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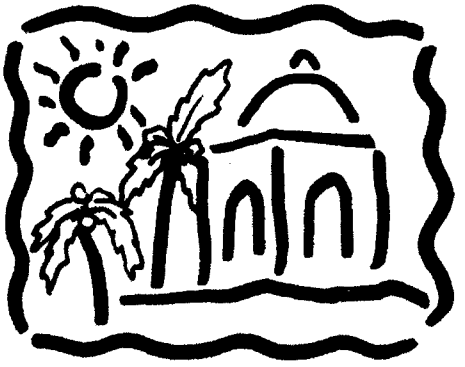


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July 29, 1992

WA: Analog Systems

WB: Multichannel Video Distribution

WC: Digital Video and Compression Techniques

WA1 STEPS TOWARD THE PRACTICAL APPLICATION OF EXTERNALLY MODULATED FIBER-OPTIC LINKS*

C.H. Cox III, L.A. Bernotas, G.E. Betts, D.R. O'Brien,
J.J. Scozzafava and A.C. Yee

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Over the past several years, the potential applications for analog fiber-optic links have increased. Our initial examination of externally modulated link models has indicated that this type of link offers several fundamental advantages over more conventional links which use direct modulation. Key among our findings were the scaling laws for link gain and noise figure with link average optical power, which are plotted in Fig. 1. These expectations were confirmed with measurements on several experimental links that demonstrated the feasibility of obtaining lossless broadband links, gain in amplifierless narrowband links, and noise figure of 5 dB, which is only 2 dB above the theoretical limit.

After a brief review of the various models and experimental results, we will present our work on some of the practical issues that must be solved so that the potential demonstrated in the laboratory can be realized in applications. Among the areas in which we have made significant progress and on which we will report are temperature-stable fiber-to-modulator attachment (see Fig. 2), automatic control of the modulator bias point, low-stress modulator mounting, and stabilization of the link gain (see Fig. 3). The techniques that are being developed in each of these areas will be reviewed. At present these methods have been implemented on a narrowband link shown in Fig. 4, and we will report experimental results on this link. The measurements demonstrate that the techniques can provide a link that operates over a temperature range of -60 to +50°C, has a modulator bias point controlled to ±0.5°, will withstand random vibration up to 3.8 gRMS, and whose gain is stable to 0.1 dB.

*This work was sponsored by the Department of the Air Force.

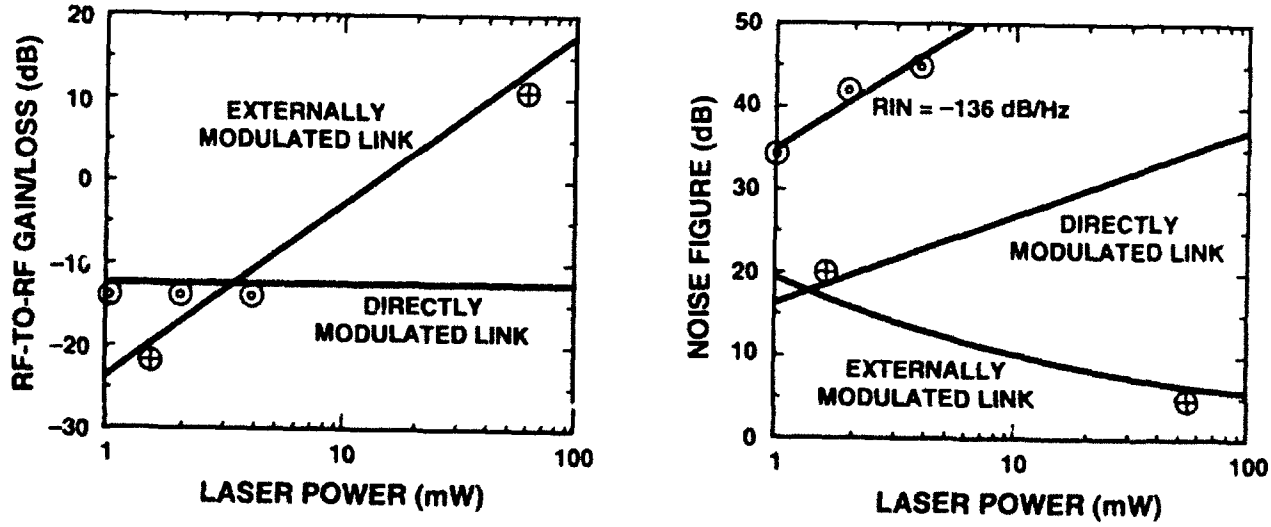


FIG. 1 RF gain and noise figure vs optical power of fiber-optic links using direct and external modulation.

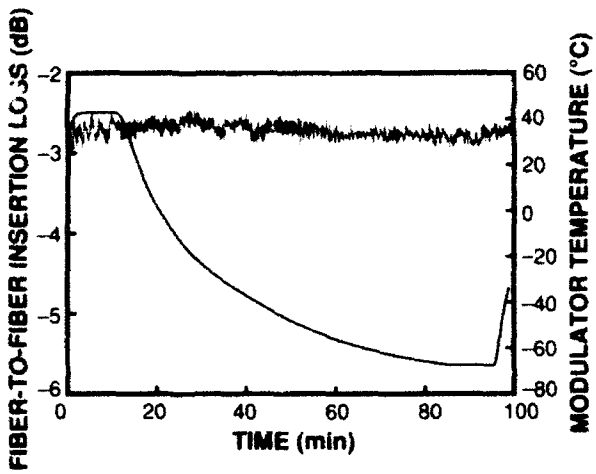


FIG. 2 Temperature (smooth curve) and integrally attached fiber-to-fiber optical loss of a Mach-Zehnder modulator.

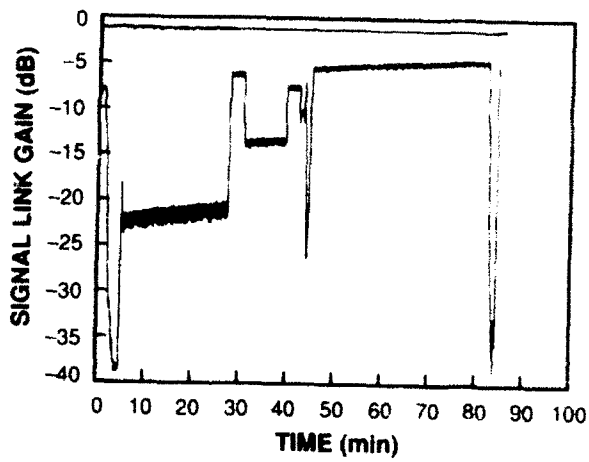


FIG. 3. Link gain vs time with (top trace) and without detector current normalization.

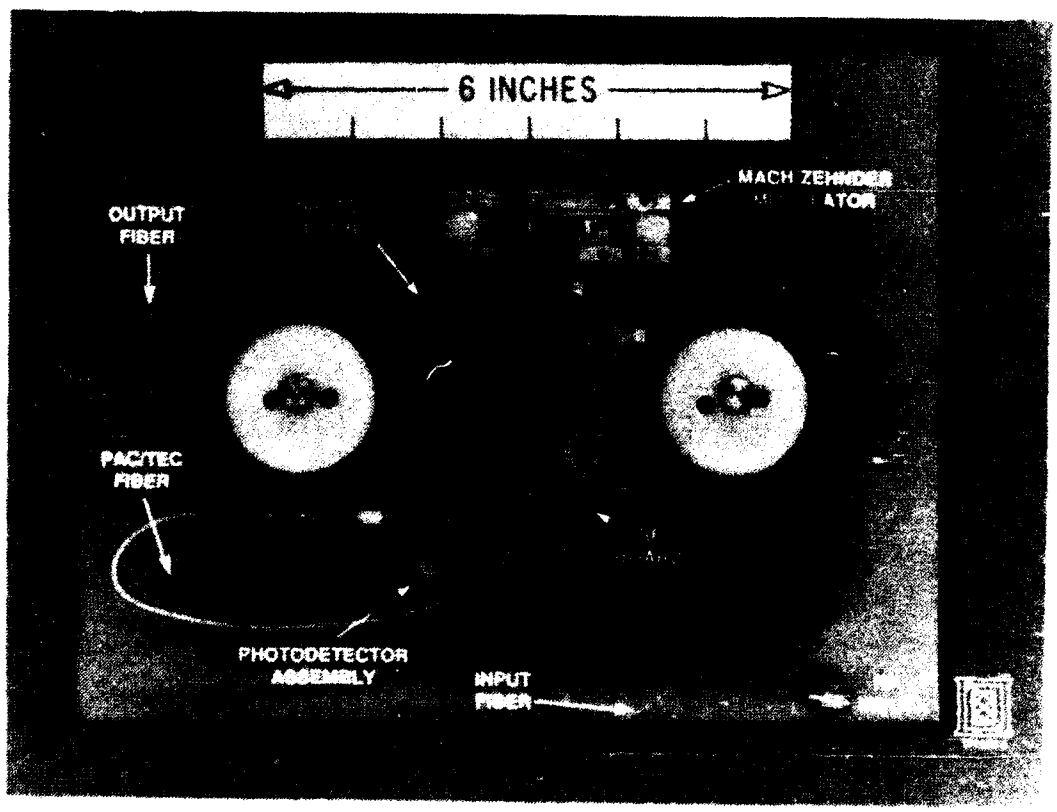


FIG. 4 Module for fiber-optic test bed.

WA2

BROADBAND DRIVE VOLTAGE MEASUREMENTS IN $LiNbO_3$ TRAVELING WAVE MODULATORS

G. K. Gopalakrishnan*, R. D. Esman, C. H. Bulmer, and W. K. Burns

Naval Research Laboratory
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Washington DC 20375

Summary

Recently the use of device structures which provide a near optical-microwave phase velocity match has led to significant improvements in broadband traveling wave $LiNbO_3$ modulators. One popular way to achieve a phase matched structure is to use a thick electrode and buffer layer(1-3). This allows adjustment of the microwave effective index to the value of the optical index. Aside from bandwidth the other important parameter for these devices is drive voltage. Usually the phase match condition is achieved somewhat to the detriment of low frequency drive voltage, but, with phase match, device length can be increased to reduce drive voltage. High frequency drive voltage is then directly related to the optical response. This paper reports on measurements of the high frequency drive voltage of the device of ref.2.

The device structure is shown in cross-section in Fig.1. A coplanar waveguide(CPW) electrode structure is electroplated on a Mach Zehnder interferometer on z-$LiNbO_3$, with an intervening SiO_2 layer. The center strip width was 8μm, gap widths were 15μm, and the buffer layer thickness was 0.9μm. The electrode thickness varied from 15-18μm on a variety of devices, but was ~18μm on the best device. The device electrode length was 2.4cm. Measurements were made at 1.3μm. Low frequency V_π's varied from 4.2-5.0V. Considering the voltage drop across the buffer layer and the asymmetry of the electrode structure with respect to the interferometer, the resulting optical-electrical overlap integral was δ=0.77-0.65. High frequency V_π can be obtained from the optical response by using

$$V_\pi(f)=V_\pi(0)\ \exp(-OR/20)\ \left[\frac{(Z_L+Z_O)}{2Z_L}\right]$$

where OR is the optical response(in dBele) and Z_L and Z_O are the device(~35Ω) and input(50Ω) impedances. The impedance term is inserted to account for the impedance mismatch at high frequency. Using the optical response from (2), this result is plotted in fig.2, showing that V_π varies from 5 to 13 volts over the 40 GHz band of the device. We expect to confirm this result by direct measurement using a two-tone distortion technique, and will report the results at the meeting.

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1. M. Seino, et al, ECOC, ThG1-5, 1990.
2. G. K. Gopalakrishnan, et al, Electron. Lett.28, p.826 (1992).
3. D. W. Dolfi and T. R. Ranganath, IPR'92, PD-2, 1992.

* Maryland Advanced Development Laboratory, Greenbelt MD 20770

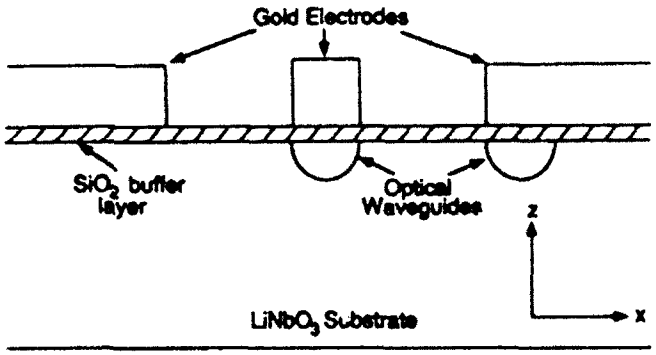


Fig.1
Cross-section of traveling wave modulator.

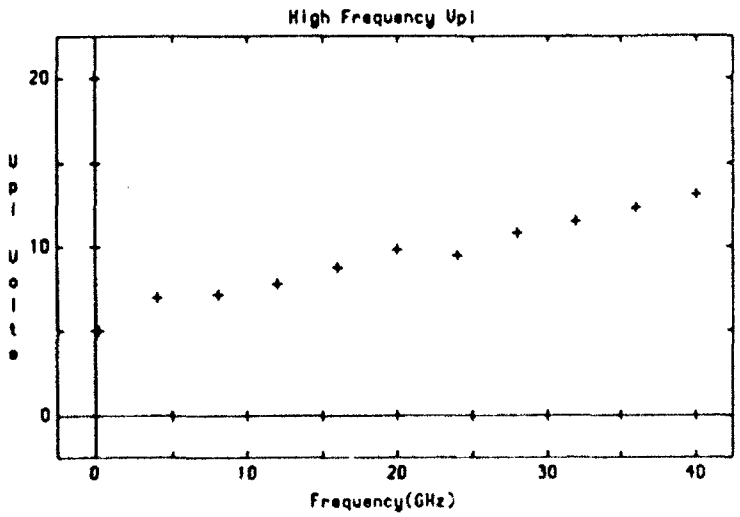


Fig.2
High frequency drive voltage.

where OR is the optical response(in dBele) and Z_L and Z_o are the device(~35Ω) and input(50Ω) impedances. The impedance term is inserted to account for the impedance mismatch at high frequency. Using the optical response from (2), this result is plotted in fig.2, showing that V_π varies from 5 to 13 volts over the 40 GHz band of the device. We expect to confirm this result by direct measurement using a two-tone distortion technique, and will report the results at the meeting.

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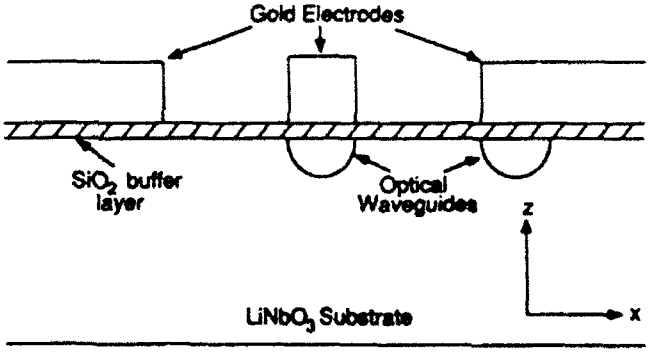


Fig.1
Cross-section of traveling wave modulator.

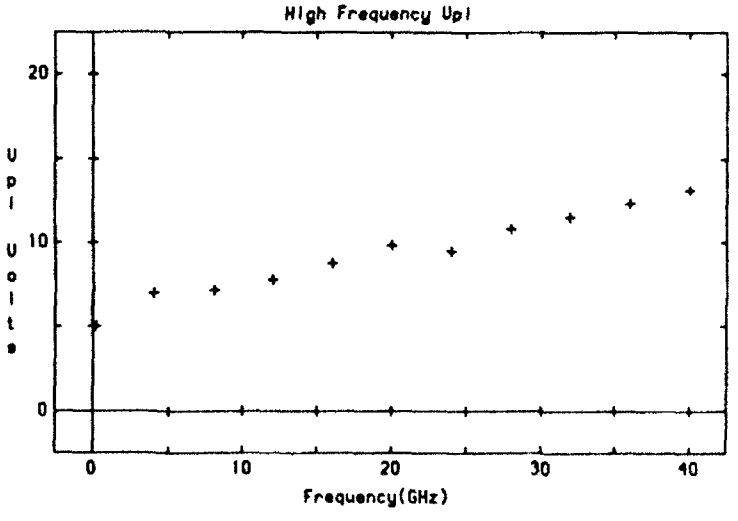


Fig.2
High frequency drive voltage.

WA3 A DIRECTIONAL COUPLER MODULATOR WITH IMPROVED LINEARITY (OPERATING UP TO 1GHz)

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External modulation of laser light is attractive because of the spectral stability, low noise, and large power available with CW solid state lasers. The potential of operating the external modulator at high microwave frequencies is particularly attractive. There is, however, a need for external modulators with linearity much better than that of the conventional Mach-Zehnder or directional coupler. Such a modulator should have a design that is practical and a linearized response that is tolerant to variances in fabrication. Researchers at UCSD have reported such a device, a conventional directional coupler modified by two passive feed-forward electrodes as shown in the figure [1], [2]. Two-tone testing with an early prototype device at audio frequencies has demonstrated a suppression in intermodulation of over 35dB for an optical modulation of 30% per tone. Presented here will be new results that address the viability of the linearized directional coupler at frequencies up to 1 GHz.

The bandwidth limits for such a modulator come from two causes: (1) drive power loss from electronic parasitics (i.e. electrode capacitance) and (2) signal distortion due to the finite transit time of the optical wavefront across the lumped active electrode. The effect of (1) can be "factored out" by considering it as a low-pass filter prior to modulation. Electrode fabrication and packaging techniques can be used to eliminate the significance of this effect for frequencies at or below 1 GHz. The effect of (2) has been viewed in the past only in terms of the reduction in fundamental signal strength. But since a linear response is desired, we consider here the bandwidth limitation provided by the spurious signal levels. Within the bandwidth where the spurious signals are well below the fundamentals (i.e. a linear response), the fundamental signal reduction will be small. Therefore, the spurious signals will ultimately impose the limit on the bandwidth.

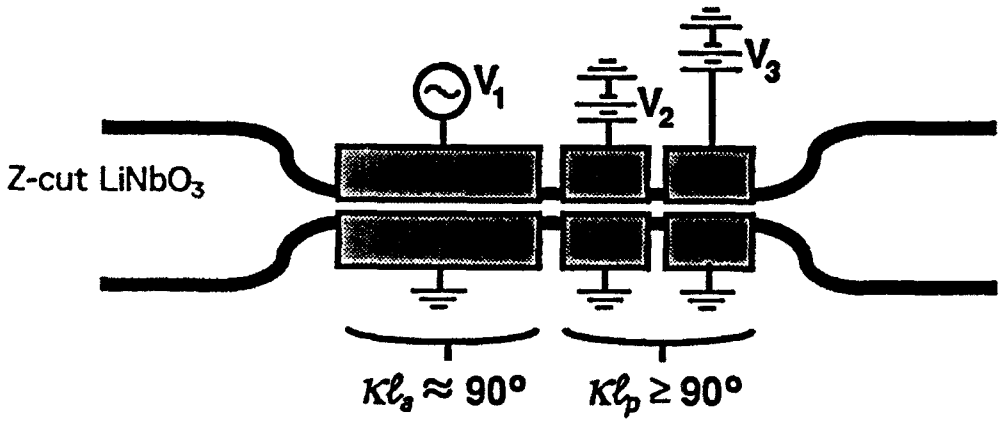
In order to experimentally investigate this frequency limitation for the linearized directional coupler, a new device has been fabricated with reduced electrode capacitance. As before, the modulator was fabricated with waveguides donated by AT&T Bell Laboratories and has the same basic design as in the figure (active electrode length is apx 1 cm). The measured capacitance of apx 5pf, however, has allowed the device to be operated at frequencies up to 1 GHz with moderate drive power resulting in significant modulation depths. This device has been placed in a test link that uses two microwave signal generators in parallel followed by an amplifier and a narrow-band filter to provide a linear two-tone input. A CW NdYAG laser at 1.3 microns is end-fired for optical input and the detected output is sent to a spectrum analyzer (HP-8566B). The preliminary results of two-tone tests at 500 MHz and 1 GHz indicate that intermodulation suppression is possible at both frequencies. But currently, extraneous spurious signals from the test link are denying a precise analysis. Test results for the fundamental and intermodulation signal levels as a function of modulation depth will be reported as available.

In addition, the computer program used to simulate the low frequency performance of the linearized directional coupler has been enhanced to account for the electro-optical phase mismatch resulting from the finite transit time of the optical wave. We are now able to calculate fundamental and spurious signal levels as a function of both modulation depth and frequency for any device composed of a cascade of coupling sections. These include conventional directional couplers ("1x2" or "2x2"), Mach-Zehnders, foreshortened directional couplers, and various versions of the linearized directional coupler discussed here. The program also allows for the simulation of transition coupling, Y-branch imperfections, coupling length variations, and bias voltage mistuning. In this way, various tolerance issues are being investigated theoretically. Results from this computer program will be presented in order establish theoretical and practical limits on linear modulation at high frequencies.

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The Linearized Directional Coupler



Only the first coupling section is modulated. The second and third sections are passive. These two passive sections provide the nonlinear compensation.

WA4 80-CHANNEL AM-VSB CATV TRANSMITTERS UTILIZING EXTERNAL MODULATION AND FEEDFORWARD ERROR CORRECTION

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Introduction

External modulation offers considerable advantages for AM-VSB signal transmission using optical fiber. This is due to the separation of the functions of light generation and light modulation. This allows the use of high power, low noise optical sources such as the Nd-YAG laser (1), in combination with a zero-chirp modulator such as the Mach-Zehnder waveguide modulator (2).

The combination of a narrow linewidth source and a chirp-free modulator avoids the problems associated with direct modulation of distributed feedback (d.f.b.) lasers such as: interferometric intensity noise from fiber backscatter and reflections (3); cavity induced CSO distortion from reflections (4); dispersion induced CSO (5); and, optical amplifier gain slope induced CSO (6). In addition, considerably higher output powers are available than from present d.f.b. lasers.

In this paper we describe the design, performance and application of externally modulated transmitters that utilize optical feedforward to correct for modulator distortion. Transmitter output powers in excess of 48 mW are achieved, distributed to four output fibers. Transmitter bandwidth (+/- 0.5 dB) is 40 - 550 MHz. Greater than 25 dB of error correction is achieved over this bandwidth, giving CTB and CSO values better than -65 dB for 80 c.w. carriers at a modulation depth of 2.8%/ channel.

Statement Of Problem

For a typical AM-VSB 40 channel system using d.f.b. lasers, a modulation depth/ channel of 4% is used, with Composite Triple Beat (CTB) of -65 dBc. State of the art systems approach the theoretical limit of approximately 5.5% (7). In general, d.f.b. distortion increases rapidly with frequency. In the absence of this frequency dependence, 4% modulation for 40 channels would correspond to ~2.8% modulation for 80 channel operation. In practice, to achieve 80 channel operation with d.f.b.s it is often necessary to use two lasers in a split-band system.

At 2.8% per channel, 80 channels, a Mach-Zehnder modulator biased for minimum composite second order (CSO) distortion, will show a CTB of -40 dB. It is therefore necessary to reduce this distortion by ~25 dB, without compromising CSO or carrier to noise (CNR).

Optical Feedforward Transmitter Design

Optical feedforward (e.g. 9, 10, 11) is a straightforward analog of electrical feedforward (8). The design of the transmitter is shown in Fig.1. The main optical source is a Nd-YAG laser (1). This is modulated by a balanced-bridge lithium niobate interferometric modulator (e.g. 12). An error signal is derived by splitting off a small fraction of this modulated light onto a photodetector and comparing this with a sample of the electrical input signal. This error signal is amplified and delayed, and then converted to an optical signal by means of a d.f.b laser. This optical error signal is combined with the main signal in a 50:50 coupler in such a way that the error signal cancels the distortion in the main signal. .

Two separate feedforward correction circuits are implemented, one for each output of the modulator. This has two benefits - first, the modulator need not be symmetrical in its distortion, and second, two separate delay adjustments are available to facilitate operation at multiple receive sites.

Results and Discussion

Results of cancellation measured by disabling the electrical sample path are shown in Fig.2. Greater than 25 dB cancellation is obtained from 40 MHz to 550 MHz. This cancellation is sufficient to allow a modulation depth of 2.8%/ channel for 80 c.w. carriers with a CTB and CSO of better than 65 dB. Measured results of distortion under these conditions are shown in Fig.3. These results are for a transmitter with four outputs, each of 12 mW. Similar results are obtained on all four outputs.

A feature of feedforward is that the error signal is a small proportion of the total signal. Therefore it can show high optical noise without significantly contributing to the overall carrier:noise. Similarly, the distortion of the error signal represents distortion of the distortion, and is a secondary effect. For these reasons, low grade

d.f.b. lasers can be used as the error correction source without the noise and distortion limitations mentioned above for systems using d.f.b.s only.

Finally, it should be noted that because, uniquely, feedforward cancels distortions of every order and indeterminate phase, it can if required be readily combined with any electrical or optical predistortion techniques to provide further enhanced performance.

Conclusion

Externally modulated transmitters utilizing high power Nd-YAG lasers, lithium niobate modulators, and feedforward error correction, show better than 25 dB distortion improvement over a standard Mach-Zehnder interferometer from 40 - 550 MHz, and total fiber coupled output powers of greater than 48 mW. This results in CTB and CSO values of better than -65 dB for 80 c.w. carriers at 2.8% modulation/carrier. Such transmitters are suitable for AM-VSB CATV distribution.

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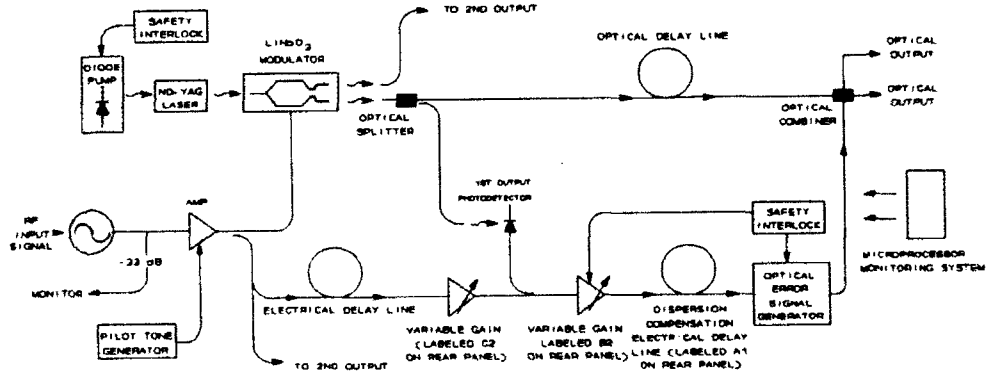


Figure 1. Block Diagram Of Transmitter.

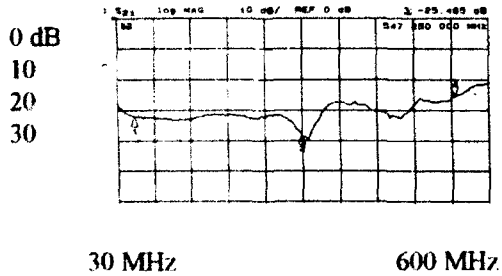


Figure 2. Cancellation

	55.25 MHz	313.25 MHz	547.25 MHz
CTB (dB)	-72.5 dB	-70.8 dB	-69.0 dB
CSO (dB)	-73.2 dB	-69.6 dB	-69.8 dB

Figure 3. Measured CSO, CTB , 80 c.w. carriers, 2.8% modulation.

WA5 EXTERNALLY MODULATED 80 CHANNEL AM CATV FIBER-TO-FEEDER DISTRIBUTION SYSTEM OVER 2X30 Km TOTAL FIBER SPAN

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ABSTRACT

Progress in predistortion linearization and the introduction of parametric feedback loops and balanced bridge electro-optic modulators yield a significant boost in analog CATV transmitter performance up to 80 NTSC channels.

Background

A feasible alternative to overcoming the difficulties associated with direct laser modulation for CATV fiber optic distribution is the use of high CW power diode-pumped solid state lasers such as Nd:YAG lasers, in conjunction with $LiNbO_3$ intensity modulators. The advantages of such approach are in the high power and low RIN (Relative Intensity Noise) of the laser source. Furthermore, an external modulator offers a bias point where the CSO (Composite Second Order) distortion is nulled out. However, the CTB (Composite Triple Beat) third-order nonlinear distortion remains to be contended with [1]. The feasibility of electronically reducing the modulator CTB was demonstrated in the pioneering work of Childs et al [2] by incorporating in the modulator driver a broadband nonlinear electronic circuit - the linearizer.

Unfortunately, the modulation depth and the number of broadcast channels achievable with the predistortion systems described to date have not yet attained the practical specifications of the CATV industry. Another problem is that modulator drift may offset the retardation away from the desirable quadrature point of null CSO distortion. Likewise, CTB distortion cancellation is generally susceptible to degradation due to variations in the electronic bias of the linearizer circuitry.

Transmitter

In the system described in this paper (Fig. 1), novel circuitry for predistortion linearization leading to enhanced modulation depth, the incorporation of parametric feedback control loops to stabilize the drifts in the external modulator and electronics, spectral and noise control of Nd:YAG high power laser sources such as RIN reduction feedback circuitry and the utilization of balanced bridge interferometer modulators to double the optical throughput, concurred to yield a practical external modulation system capable of broadcasting 80 CATV channels with CATV industry specifications for carrier to noise ratio and intermodulation distortion and with enhanced fan-out capabilities suitable for the FTF (Fiber-To-Feeder) multiple splitting CATV fiber distribution architecture covering 60 Km total fiber span (sum of all fiber segments) and meeting industry specifications of CSO, CTB, CNR (Carrier to Noise Ratio).

Experiment

The experimental set-up is described in Fig. 2. Fiber output #1 of the transmitter is connected to a spool of 30 Km single-mode fiber followed by a variable optical attenuator that feeds into the input of an optical receiver. Fiber output #2 of the transmitter is split three ways by means of 3-dB optical couplers to feed three fiber spools with the lengths of 20 Km, 10Km, 5 Km. Three optical receivers are connected to the ends of these three fiber links. The RF outputs of these receivers are displayed on three TV monitors. The output of receiver #1 is bandpass filtered using a tunable filter, preamplified and displayed on a spectrum analyzer.

The transmitter RF input is connected to a multichannel generator for an unmodulated carriers test on the spectrum analyzer. Alternatively, two of the 60 unmodulated carriers are replaced by two channels of modulated video (character generator and laser disc player) in order to assess picture quality by switching between the fiber input and a coax bypass provided with each one of the receivers .

The receiver is based on a PIN photodiode with typical responsivity 0.85, and noise equivalent current $8pA/\sqrt{Hz}$. The CSO and CTB contributions of the receiver are negligible for detected optical power less than 0 dBm.

The variable optical attenuator was set to achieve a total loss of 12 dB for link #1. The optical power on transmitter output fiber #1 was 9.8 mW and the received optical power was 0.63 mW. The laser optical spectrum measured with a spectrophotometer exhibits single wavelength operation at 1319 nm with several longitudinal modes present. A REN measurement was performed yielding -162.8 dBc.

The RF spectrum at the receiver output at 439.25 MHz (channel 60) displays a CSO contribution at a frequency 1.25 MHz to the right of the carrier at a level of -70.6 dBc. The spectral displays exhibit no heterodyned noise around the carriers, indicating a negligible value of baseband RIN. The CTB measurement for channel 32 indicates a CTB = -65.8 dBc. The corresponding CNR measurement indicates a CNR of -118 dBc/Hz, i.e. in the 4 MHz equivalent noise bandwidth of an NTSC channel CNR = 52 dBc.

Upon measuring 80 unmodulated NTSC channels, the input RF signal level to the transmitter is readjusted about 2 dB lower than the 60 channel case to maintain a reasonable balance between CTB and CNR such that CTB<-65 dBc, resulting in CNR>50 dBc throughout the band.

The modulation index for the 60 NTSC channel case was measured to be 3.6% using a two-tone method. An alternative method of verifying the modulation depth is to use the CNR equation for an AM fiber link, assuming 10 mW transmitted power, 3.6% peak modulation depth per channel, $8\,pA/\sqrt{Hz}$ receiver equivalent noise current, REN=-163 dB/Hz. At 12 dB link loss the CNR predicted by this equation is 52.5 dBc, vs. the value of 52 dBc experimentally measured.

In order to assess the impact of reflections from the multiple connectors present in the system, fiber #2 was disconnected while observing the CTB, CSO and CNR spectrum analyzer displays. No change was observed in the measurements spectral displays due to the fiber disconnection and subsequent reconnection. Conversely, with two of the unmodulated carriers replaced by two channels of modulated video, no variation in picture quality was observed on the TV monitors as fiber #1 was disconnected and reconnected.

Conclusion

In experiments using the new transmission system, distribution over 2 fibers of 30 Km each, wherein each fiber carries 80 NTSC channels, is now routinely achieved with a CNR > 50 dBc and a CTB < -65 dBc, and CSO typically -70 dBc. As the number of channels broadcast over each fiber is reduced from 80 to 60, CNR increases to 52 dBc. The fiber links served by the system under test each have 12 dB link budget, and include 4 connectors per fiber, with no degradation observed in one link when the connectors were opened on the other link.

To compare these results to previous work in predistortion linearization, a CTB suppression of about 17 dB for 50 modulated carriers at modulation index of 3.2% yielding a CTB of -60 dBc was previously reported [2]. Work on 60 or 80 channel external modulation transmission is not available for comparison. Our experiment achieved in excess of 26 dB CTB linearization suppression with 60 unmodulated carriers and 3.6% modulation index (suppression of the initial unlinearized modulator CTB at -39 dBc to better than -65 dBc after linearization).

Our results on 80 channels correspond to 2.8% modulation index for -65 dBc CTB.

The 80 channel transmission capabilities correspond to the largest number of channels broadcast via a single fiber as reported to date. Furthermore the transmitter fan-out is doubled by having two output fibers.

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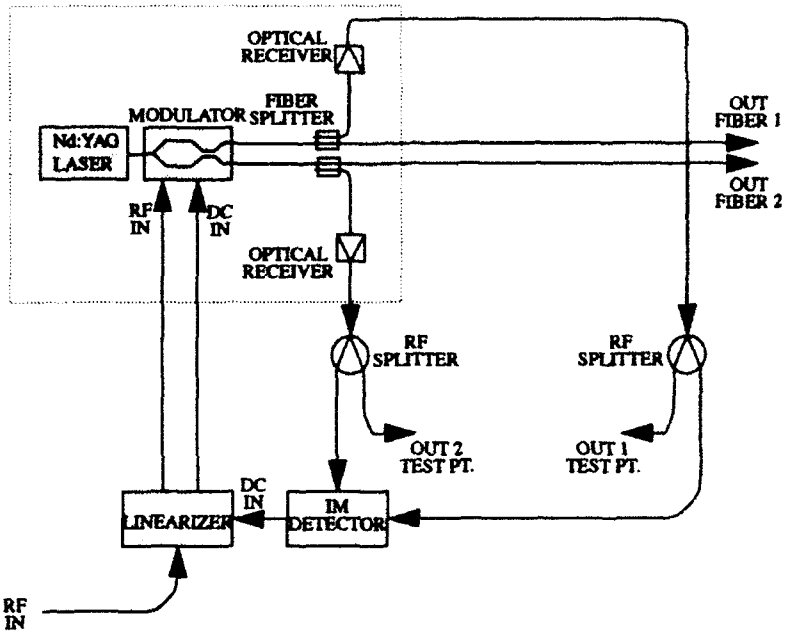


Fig. 1: External modulation transmitter with predistortion linearization and parametric control

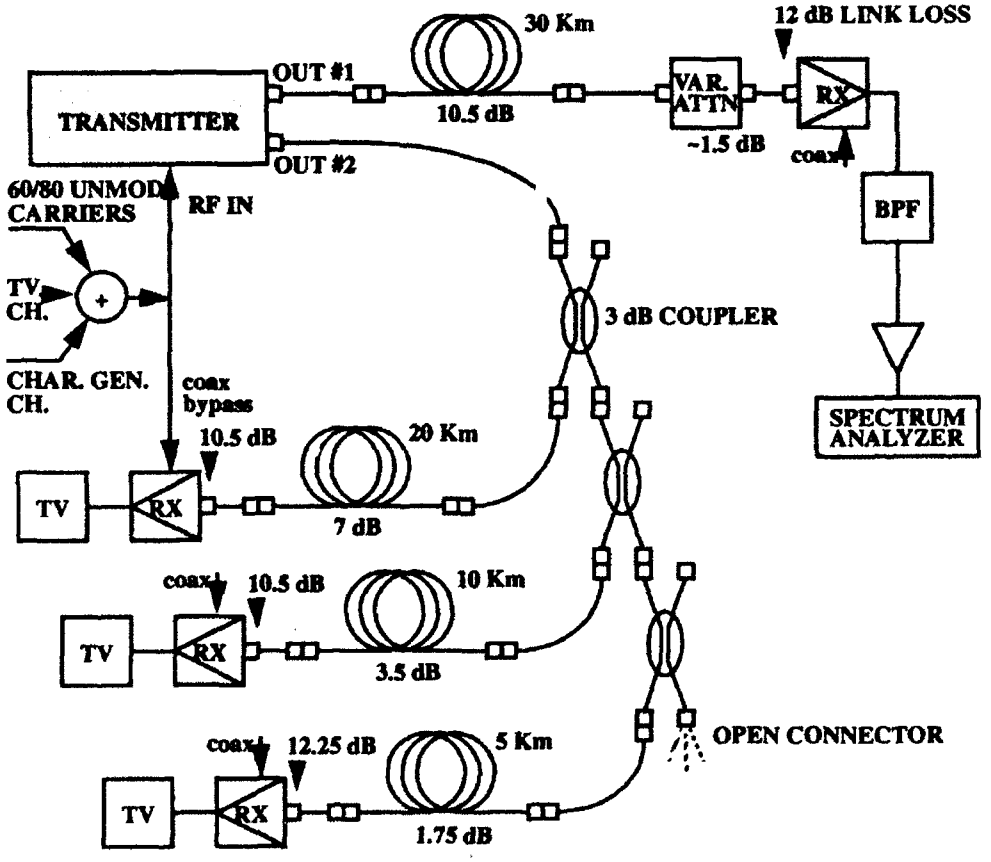


FIG. 2: Experimental set-up for testing the transmitter of Fig. 1, spanning a total of 65 Km of fiber and a multitude of connectors

WB1 TECHNOLOGY ADVANCES FOR LIGHTWAVE CATV TRANSMISSION

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As deployment of analog lightwave technology accelerates throughout the cable television industry, the broadband potential of the resultant architecture is inspiring creative new opportunities. Numerous variations of the fiber-trunk/coax-distribution architecture promise bandwidths near 1 GHz to groups of between 100 to 2000 subscribers per trunk. Each of these proposals shares a common limitation; that several fiber links are required to achieve 1 GHz bandwidth in the fiber trunk that feeds a 1-GHz single-coaxial cable distribution system. This apparent limitation of today's lightwave technology clearly leaves room for innovation.

The limited bandwidth capability of analog fiber systems arises from well-understood technical concerns. Nonlinearity in the laser limits the total modulation that can be applied, $m\sqrt{N}$, where m is the modulation depth per channel and N is the number of channels. Noise (ideally just shot noise) limits the CNR for a given m. Receiver nonlinearity limits the total modulated power that can be detected. These factors combine to make the availability of large numbers of low-cost single-laser 80-channel systems a formidable goal.

Given the technical limitations, there exist numerous alternatives by which operators can achieve the 1-GHz potential of their networks. The choices include increasing the load on a single laser, using multiple lasers on multiple fibers, or using wavelength-division multiplexing to increase the usable bandwidth per fiber. Increasing the load on a single laser is particularly attractive if the extended bandwidth is used for more robust digital-QAM channels, rather than additional AM-VSB channels.

For bands of 60 AM-VSB channels (55.25-433.25 MHz) and 60 64-QAM digital channels (441.25-795.25 MHz), windows of feasibility can be derived [1], as shown in Figure 1. Feasibility is limited by the standard noise and linearity limits and, in addition, by nonlinear interactions between channels in the two bands. As Figure 1 shows, for this particular ideal laser, the VSB band can be transmitted for modulation indices between 4.2 and 5.9 %, and the QAM band between 0.2 and 2.5 %. The laser is ideal in that only clipping [2] and resonance-induced distortion [3], which becomes significant as frequencies approach 1 GHz, are included. This system is feasible only because the relatively robust QAM channels can be de-emphasized to the level at which they contribute little to the overall load on the laser. For two bands of AM-VSB channels, and similar channel counts, the window is non-existent.

Given that large numbers of 60-80 channel single-laser systems are now being installed, it would be sensible if future extended-bandwidth systems could make use of these sub-500 MHz lasers. Wavelength-division multiplexing (WDM) is the most natural way to achieve this graceful growth. In considering WDM for AM-VSB transmission choices must be made between 1.3 or 1.55 μm wavelength operation, direct or external modulation, and whether the architecture should support broadcast or narrowcast services, or both. An architecture that supports broadcast distribution of 60 AM-VSB channels (55.25-439.25 MHz) and narrowcast transmission of an additional 52 AM-VSB channels (445.25-751.25 MHz), shown in Figure 2, has been demonstrated [4]. The broadcast source is at 1.55 μm wavelength, allowing for Er-doped fiber amplification, and is externally modulated to eliminate CSO distortion induced by the interaction of chirp and fiber dispersion. Narrowcast transmission at 1.3 μm takes advantage of the low cost of directly-modulated lasers.

Further increases in fiber capacity will require WDM components that allow multiple wavelengths within a given transmission window, and analog sources at precisely-specified wavelengths. Greater bandwidths can also be served if compressed digital video and QAM modulation take the place of AM-VSB, at least in the extended frequency band. Therefore, if compression technology continues to advance rapidly, 1 GHz capabilities should be possible without this next level of WDM complexity.

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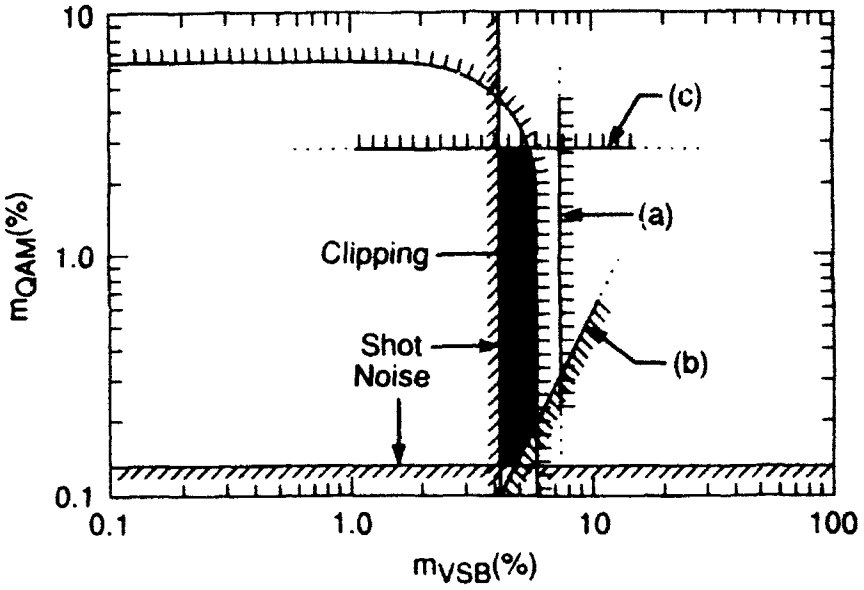


Figure 1. Window of feasibility for typical single-laser split-band transmission of 60 AM-VSB and 60 digital-QAM video channels [1]. Modulation indices (m) are bounded by shot noise, clipping, and several other nonlinear processes. (a) is the limit imposed by second-order resonance distortion (RD) within the VSB band. (b) is the limit from second-order RD from the VSB band interfering with QAM channels. (c) results from third-order RD, involving 2 QAM channels and 1 VSB channel, interfering with a VSB channel.

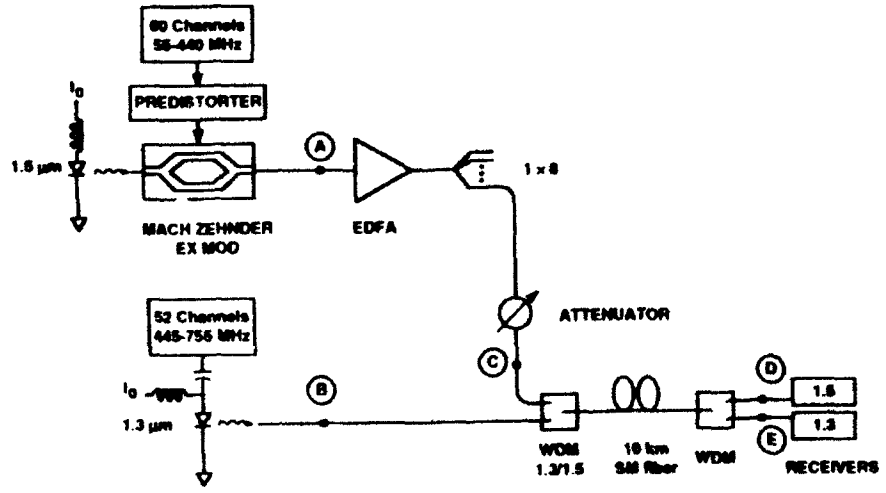


Figure 2. Split-band 112-channel WDM demonstration system [4] using broadcast externally-modulated 1.55 μm and narrowcast 1.3 μm direct modulation.

WB2 APPLICATIONS OF ERBIUM-DOPED FIBER AMPLIFIERS FOR VIDEO DISTRIBUTION SYSTEMS

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Erbium-doped fiber amplifiers (EDFAs) have made it possible to develop subcarrier multiplexed all-fiber video distribution (SCM-AFVD) systems, because their noise and distortion are low. At high pump powers, the noise figure is low while efficiency is high (Fig.1). Low noise EDFAs are characterized by small threshold noise figures, NF_{th} , and low threshold pump powers, P_{th} [1]. Reflection sites upstream of the erbium-doped fiber (EDF) degrade the noise figure more than those after the EDF (Fig. 2). The noise figure is mostly determined by the reflection loop created between the upsteam reflection site and the EDF itself. A low noise EDFA must have minimal internal reflection [2].

We have experimentally demonstrated a 4-cascade EDFA system that uses optically switched stand-by EDFAs (Fig.3). The stand-by EDFA replaces the damaged one automatically. Each EDFA is a compact size package (H200 x D280 x W15 mm). The optical switch is mechanical, and has low loss (0.36 dB for a 1x2 switch and 0.86 dB for a 1x8 switch) with high return loss (48 dB) [3].

The system simultaneous carries 11 AM-NTSC (90-220 MHz) and 50 FM-NTSC/HDTV (500 MHz-2.5 GHz) video channels. The output power from the 4-cascade EDFA system is about 14 dBm. The receiver power is down to -9 dBm for 49 dB CNR of AM video and 52 dB CNR of FM video. Low cost 50 channel FM video tuners, composed of an MMIC synthesizer, a commercial Broadcast Satellite (BS) converter, and a commercial BS tuner, were used. The compressed digital video (5-10 Mb/s) channels will be able to be multiplexed between AM and FM video chanels with a 6 MHz spacing.

The difference between light wavelength and fiber zero-dispersion wavelength causes dispersion noise and distortion, and degrades the picture quality when the direct modulation scheme is applied [4]. The application of EDFA's also incurs distortion due to their gain tilt and laser chirp [5]. When an external modulator is used, these problems can be virtually eliminated [6]. We tested the other solution of using dispersion and gain tilt equalizers. The dispersion equalizer was made of optical fiber, and its loss was quite low (1.96 dB). The gain tilt equalizer was a detuned optical bandpass filter, which had equivalent but opposite loss tilt. Measured results of the distortion improvement by these equalizers are shown in Figs. 4 and 5. The equalizers permit the extension of the optical/electrical hybrid CATV area, as well as the AFVD area.

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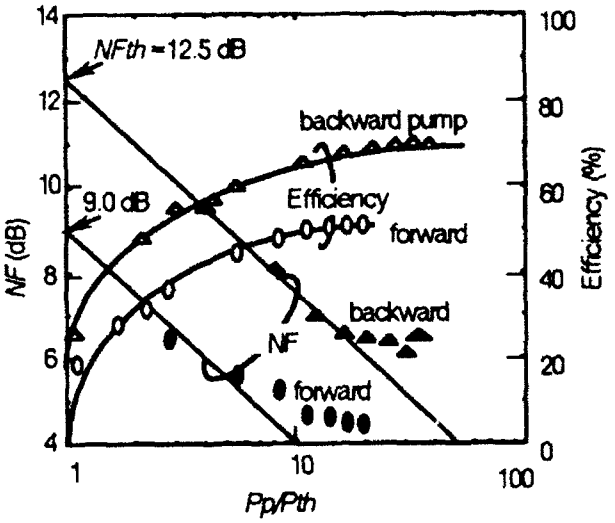


Fig. 1 NF and efficiency vs. normalized pump power characteristics of EDFA
Pth (forward)=5. 6 mW, Pth (backward)=4. 8 mW

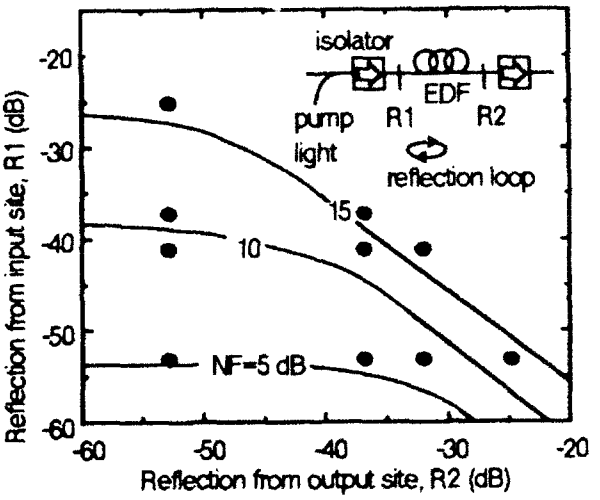


Fig.2 Noise figure degradation of EDFA due to reflection light

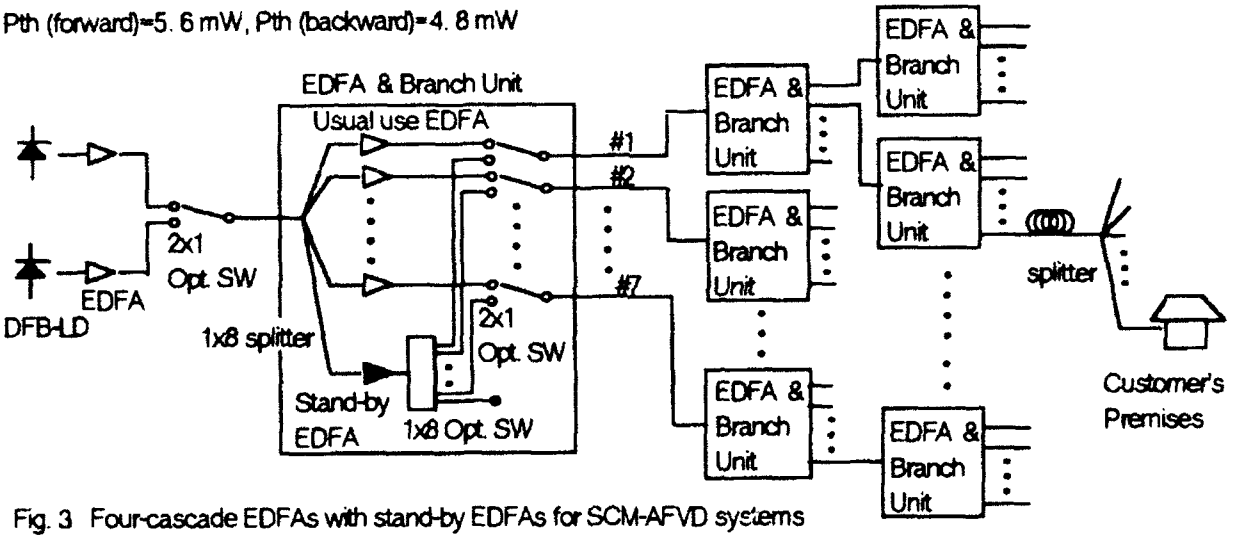


Fig. 3 Four-cascade EDFAs with stand-by EDFAs for SCM-AFVD systems

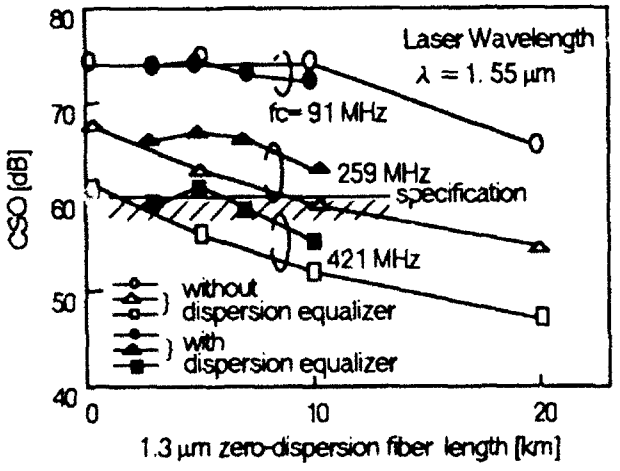


Fig. 4 CSO improvement with dispersion equalizer. Total AM-TV channels is 40. Modulation depth is 4%/ch.

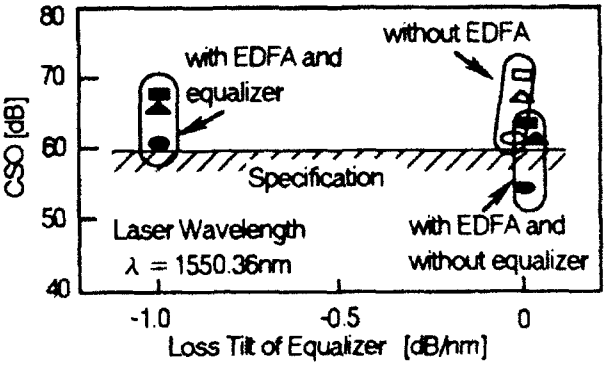


Fig. 5 CSO improvement with gain tilt equalizer. The square plots are for the 91 MHz channel. The triangle plots are for the 259 MHz channel. The circle plots are for the 421 MHz channel. Total AM-TV channels is 40. Modulation depth is 4%/ch.

WB3 A COMPARISON OF OPTOELECTRONIC REPEATERS AND OPTICAL AMPLIFIERS FOR VIDEO DISTRIBUTION SYSTEMS

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Summary

Many CATV systems employ point to point fiber optic links to transport multichannel AM video signals from the headend to the neighborhood. These point to point links can transmit completely different channels to each neighborhood to support such services as video on demand. If all that is needed is to transmit identical programming to all neighborhoods, then an optical tree and branch architecture is generally more favorable economically than a point to point architecture. Branching in an optical network is readily achieved using optical splitters.

Erbium doped fiber amplifiers (EDFA) operating at 1550 nm have been proposed to boost the signal at the branch points prior to splitting the signal. There are several significant problems with EDFA based AM systems which remain to be solved. If DFB lasers are used, then laser chirp results in CSO degradation due to the gain slope of the EDFA. Laser chirp along with fiber dispersion results in severe CSO degradation when 1310 nm zero dispersion fiber is used. External modulation suffers from very poor CTB from the basic modulators requiring extremely precise distortion compensation. In addition, stimulated Brillouin scattering, resulting from the narrow linewidth of the cw lasers used with the external modulators, limits the amount of power that can be launched into the fiber to approximately 4 mW. Finally, optical amplifiers have a theoretical minimum noise figure of 3 dB which in practice is even higher.

An alternative to the optical amplifier is the optoelectronic repeater. In the case of the optoelectronic repeater, the signal at each branch point is first detected and electronically amplified and then regenerated using one or more lasers. The entire system can be constructed using 1310 nm DFB lasers and conventional singlemode fiber. The output power of the optoelectronic repeater depends on the output power of each individual DFB laser and on the number of lasers that are used. Optoelectronic repeaters and optical amplifiers can thus have comparable output powers.

We have constructed EDFAs and optoelectronic repeaters and measured their performance. The noise figures of the two types of signal regenerators are shown in Figure 1. The optoelectronic repeater used a photodiode having 90% quantum efficiency, an amplifier with 6 $pA/Hz^{1/2}$ input noise and a laser with a RIN of -160 dB/Hz. The EDFA was pumped at 980 nm in the forward direction and at 1480 nm in the reverse direction.

Because of the lower noise figure, less optical power is needed at the secondary receiver of a repeater based system than is required at the receiver of an EDFA based system. Performance comparisons for a variety of system configurations have been analyzed and will be presented.

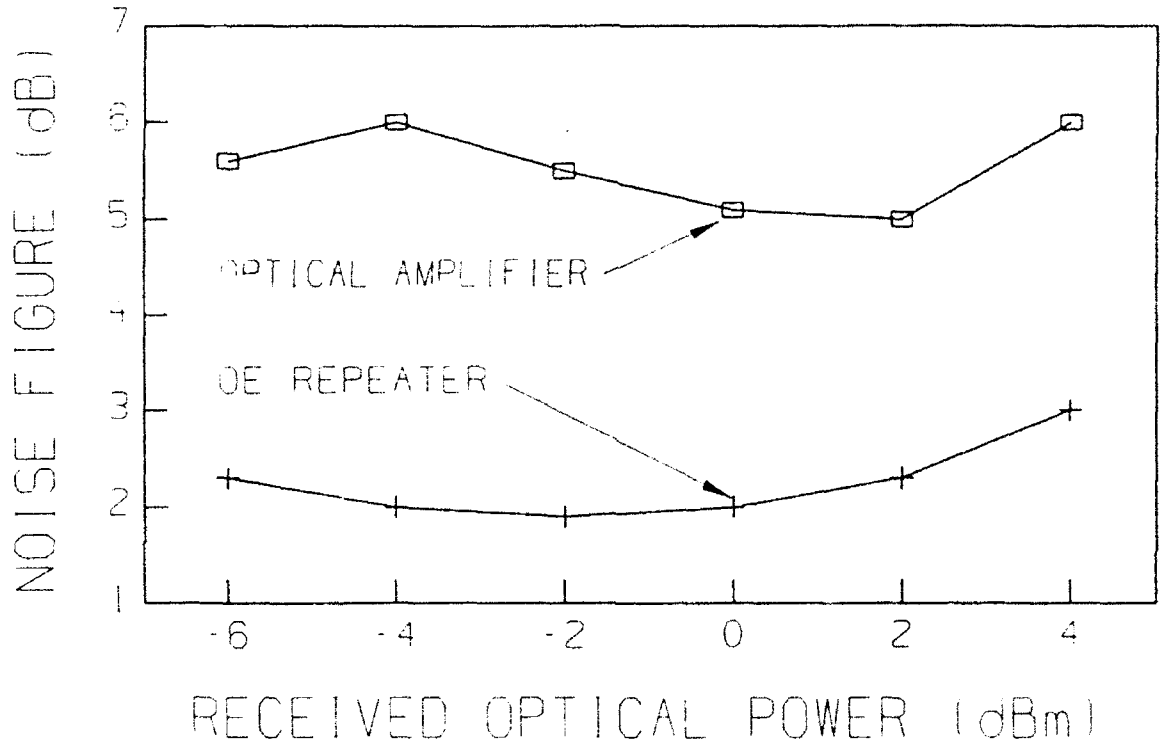


Figure 1. Noise figure of an optical amplifier and an optoelectronic repeater vs. received optical power.

WB4 **MULTICHANNEL M-QAM FOR CATV DISTRIBUTION**

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There is growing interest in augmenting the subcarrier multiplexed analog AM-VSB CATV channels with digitally modulated ones using spectrally efficient, M-ary Quadrature Amplitude Modulation (M-QAM) in the 500MHz-1GHz band. The advantage is that digital signals are more robust with respect to noise, channel imperfections and nonlinearities. Even with this heated interest, answers are not yet known to simple questions such as: *How many channels can be offered? At what bit rate and error probability? How much laser power is needed? What is the loss budget? etc...* We will set the framework within which we can address these and other issues.

Signal Power: The digital RF signal consists of N subcarrier multiplexed, independently modulated, M-QAM signals. Assume square-wave baseband shaping, consider one of these signals, and assume that during the i^{th} symbol interval, the in-phase and quadrature coordinates of the transmitted point are a_i and b_i, where $a_i, b_i \in \{\pm 1, \pm 3, ..., \pm \sqrt{M}-1\}$. Note that a_i and b_i are normalized. The symbol-dependent received signal power is $d^2 I_0^2 r_i^2$ where d (scaling parameter) is the horizontal/vertical (H/V) distance between constellation points at the receiver, I_0 is the received average photocurrent, and $r_i^2 = a_i^2 + b_i^2$ is the radius of the i^{th} symbol point. As mentioned above, the received signal power depends on the transmitted symbol. We average over all symbols to obtain the average received signal power $\overline{P_{rec}} = d^2 I_0^2 (M-1)/3$. Note that we can think of the digitally modulated optical signal as an amplitude-modulated one with an effective modulation index given by $\bar{m} = d\sqrt{2(M-1)/3}$.

Shot Noise: The shot noise power at the receiver is given by $2eI_0B$, where e is the electron charge and B is the receiver bandwidth. The minimum required bandwidth per channel is $B = 2R/\log_2 M$, where R is the bit rate. In practice, a larger bandwidth will be used to reduce interference between channels.

Laser Clipping: It can be shown that the nonlinear clipping-induced distortion is the same as that of an AM-VSB system, but with an rms modulation index given by $\mu^2 = Nd^2(M-1)/3 = N\bar{m}^2/2$,

SNR: The average signal-to-noise ratio, $\overline{\gamma_s}$, is given by

$$\overline{\gamma_s} = \frac{d^2 I_0^2 (M-1)}{3\left[2eI_0B + NLD\, I_{\{d>d'\}}\right]} = \frac{I_0^2 \bar{m}^2}{2\left[2eI_0B + NLD\, I_{\{d>d'\}}\right]} \qquad (1)$$

where, the nonlinear distortion power, $NLD = I_0^6 \mu^5 exp(-1/2\mu^2)/(\sqrt{2\pi}(1+6\mu^2)N)$, and $d' = 1/(.5\sqrt{2}(\sqrt{M}-1))$ is the H/V distance below which clipping does not occur. d' is found by assuming that each channel is sending one of its corner points and requiring that the composite RF current remains larger than the threshold current. $I_{\{d>d'\}}$ is the indicator function; $I=0$ for $d \leq d'$, and $I=1$ for $d > d'$.

It is instructive to find out the system capabilities at $d = d'$ (see Figure 1), that is, with the modulation index chosen such that clipping does not occur, so that the system is shot-noise limited. Using (1), we obtain

$$I_0/N = \overline{\gamma_s} \cdot \frac{24e(\sqrt{M}-1)}{(\sqrt{M}+1)\log_2 M} \cdot RN \qquad (2)$$

where I_0/N is the received photocurrent per channel, and RN is the total system throughput (bit rate per channel $\times$ number of channels). For 64-QAM and a symbol error probability of 10^{-9} ($SNR = 28.92$ *dB*), $I_0/N\ (mA) = 3.89 \times 10^{-13}\ RN$. Thus, assuming a laser output power of 0 *dBm* and a photoresponsivity of 0.8, we can deliver 100 channels at 10 Mbits each (total throughput = 1 Gbits) at a symbol error probability of 10^{-9}, *and still have about 13 dB of loss margin*. This is a tremendous achievement in contrast to AM-VSB, which cannot offer a comparable number of channels at these power levels as the carrier-to-noise ratio is not high enough. Note that the QAM system's performance improves when driven slightly into the clipping region (Figure 2).

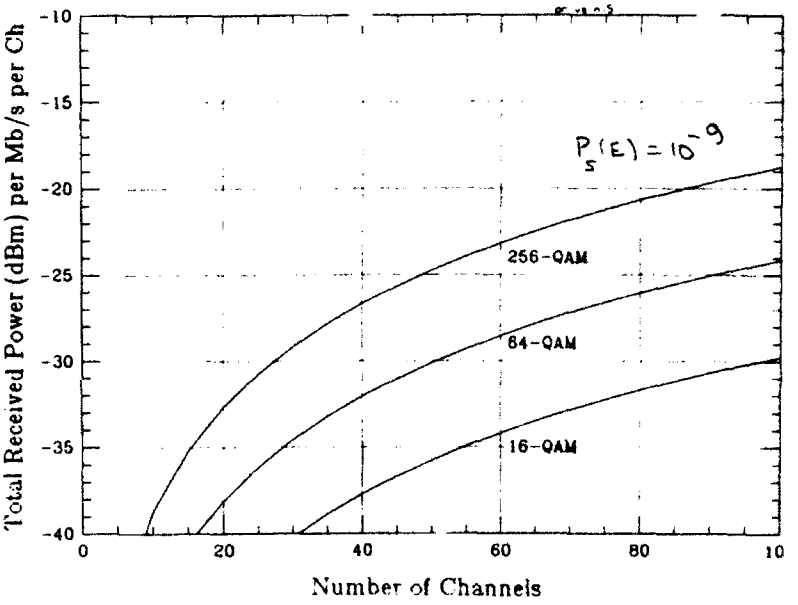


Figure 1 The required total received power per (Mb/s per channel) versus the number of channels where $d = d'$ (no clipping), and where the per-rail symbol error probability is 10^{-9}($SNR = 28.92$ *dB*). For example, with 64-QAM, we can have a 100-channel system operating at 10Mb/s per channel (1Gb/s total throughput) with a total received power of -14 *dBm* and using a minimum bandwidth of 333 *MHz*.

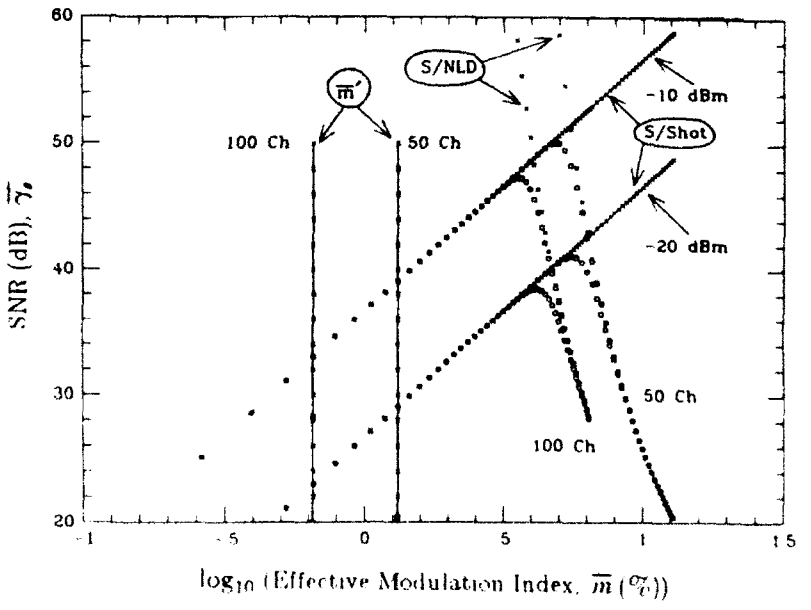


Figure 2 64-QAM, 10Mb/s/ch: The effect of increasing d beyond d' ($\overline{m}$ beyond $\overline{m}'$) which marks the onset of clipping. Initially, the clipping is negligible resulting in an improvement in SNR until larger values of d are reached where clipping dominates and drives the SNR down. The vertical lines show the value of $\overline{m}'$ for a 50-channel and a 100-channel system. We see that we can have an appreciable gain by over driving the system into the clipping region (to the right of the vertical lines).

WB5

DESIGN TRADEOFFS FOR VERY SHORT CASCADE SYSTEMS FOR CATV

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Over the past three years the cable television industry has developed and implemented AM fiberoptic technology with ever increasing intensity. At present that adoption has become so commonplace that essentially no new-builds or significant rebuilds are done without substantial fiber content. This rapid conversion to the new technology has been accompanied by a remarkable shift in the basic distribution system architectures. In fact it may be more appropriate to say that the conversion was made possible by the industry's readiness to change its whole way of thinking about system designs. This paper will give the reasons for these fundamental changes of architecture and will discuss the design implications.

Background

The feature of fiberoptic technology that is most attractive for uses in CATV is fiber's low attenuation of high bandwidth signals. This feature has been used to achieve a number of operational benefits by allowing relatively long unrepeatered transmission spans from the cable headend to neighborhoods of customers. Initially this allowed operators to break up existing long coaxial cable trunks in order to improve picture quality and to reduce service outage group size. Generally, however, there was a cost penalty for this application, which had to be justified by the service benefits.

Two years ago -- after the industry leaders had convinced themselves that the AM fiber components were "real" -- new ways for applying these pieces were first proposed. The key conceptual jump was the realization that if fiber allowed the CATV signals to be delivered to neighborhoods with the best "trunk-like" distortion and noise levels, then the trunk could be dispensed with entirely. One could say that the system architecture went from trunk-and-branch to "floating branches." This was accomplished by designing with multi-output fiber node amplifiers feeding cascades of approximately four line-extenders, all operated at relatively high levels, thus allowing the branches to reach large groups of subscribers. Excellent end-of-line distortion performance could be achieved despite the high amplifier output levels because the cascades were so short.

This fiber-to-the-feeder (FTF) architecture was immediately accepted by a large segment of the industry because it allowed them to gain the many performance and service advantages of fiberoptic delivery <u>at no additional cost per subscriber</u> when compared with conventional trunk-and-branch system designs. Indeed the cost of the fiberoptic components was decreasing dramatically, but the more significant determining factor (on a cost per

subscriber basis) was the ability of the FTF architecture to reach large numbers of subscribers from a single fiber node. Thus one year ago five-amplifier cascades became the norm for new system designs.

Very Short Cascades

During the past year, however, the key operating premise of the industry has changed dramatically. The emphasis for many operators has shifted toward ensuring their ability to deliver new services, such as specialized program delivery and telephony. This implies, in turn, that the number of subscribers fed from any one node must be reduced. Thus the architecture is moving toward three, two and even one-amplifier (fiber-to-the-pedestal) designs, with the additional equipment cost per subscriber being offset by expected additional revenue opportunities.

Additionally, these new service opportunities give rise to needs for increased bandwidth-delivery capability. Short amplifier cascades make these requirements somewhat easier to achieve, since the greater distortions from each amplifier will be compounded fewer times.

These new service requirements and the architectures that they mandate present the system designer with a completely different set of design elements. The designer must apply these elements to achieve not just performance and cost objectives as in the past, but now service group size goals, as well. Table 1 gives an indication of the complexity of the task: it shows the variety of design possibilities for a constant end-of-line performance goal. In particular, the table indicates that small node group sizes can be achieved at lower numbers of amplifiers/mile by deploying cascades of one or two distribution amplifiers (DAs) from the node.

Table 1. Fiber-to-the-feeder distribution alternatives

Distribution	Back-feed	Cas-cade	Tap type	Reach (mi)	System miles	Total ampls	Ampls per mi	Homes pass
Single DA	Y	2	NPP	0.49	3.8	9	2.4	605
DA split feeder	Y	5	NPP	1.45	5.3	21	3.9	854
Two DA	Y	3	NPP	0.72	5.9	17	2.9	949
Express feeder	Y	5	PP	1.51	6.1	17	2.8	974
Std five-ampl	N	5	PP	0.98	8.0	53	6.6	1285
Std five-ampl	Y	5	PP	1.18	10.4	53	5.1	1659

Backfeed: "Y" indicates that extensive dual cable is used
Cascade = max no. of amplifiers to a subscriber, incl fiber node
Tap type: "NPP" indicates that AC power is not passed thru taps
Reach = cable distance from headend to farthest subscriber
System miles = cable miles serving homes from a single fiber node
Homes passed: calculated at 160 homes per mile

Note: standard five-amplifier models use 3 line-extenders/branch

WC1

INTRODUCTION TO DIGITAL VIDEO

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A video signal such as television is traditionally processed in the analog domain. Due to recent advances in digital electronics and signal processing algorithms, video signals are now being processed almost exclusively in the digital domain. Two most outstanding characteristics of digital video are flexibility and robustness. Because of these, a video signal can be processed and compressed for various applications. In this talk, a brief description of several important aspects of digital video will be presented.

WC2

A HIGH PERFORMANCE VIDEO CODEC

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Summary

A high quality digital video codec has been developed for the Zenith/AT&T HDTV system which adaptively selects between two transmission modes with differing rates and robustness. The codec works on an image progressively scanned with 1575 scan lines every 1/30th of a second and achieves a compression ratio of between 50 and 100 to 1. The high compression ratio facilitates robust transmission of the compressed HDTV signal within an NTSC taboo channel. Transparent image quality is achieved using motion compensated transform coding coupled with a perceptual criterion to determine the quantization accuracy required for each transform coefficient. The codec has been designed to minimize complexity and memory in the receiver.

The video encoder is shown in Figure 1. Motion compensated transform coding exploits both the temporal and spatial redundancy present in the HDTV signal. Hierarchical block matching is used to remove temporal redundancy from one frame to the next. Using the motion vectors, a displaced frame difference (DFD) is computed and transformed using the discrete cosine transform (DCT) to remove the spatial redundancy. Each new frame of DFD is analyzed prior to coding to determine its rate versus perceptual distortion characteristics and the dynamic range of each coefficient. Quantization of the DCT coefficients is performed based on the perceptual importance of each coefficient, the precomputed dynamic range of the coefficients and the rate versus distortion characteristics. The perceptual criterion uses a model of the human visual system in order to determine the sensitivity to color, brightness and spatial frequency. This information is used to equalize and minimize the perception of coding artifacts. Parameters of the coder are optimized to handle scene changes that occur frequently in entertainment/sports events and channel changes made by the viewer. The distortion level is controlled by anticipating scene changes and monitoring the fullness of the coded video buffer.

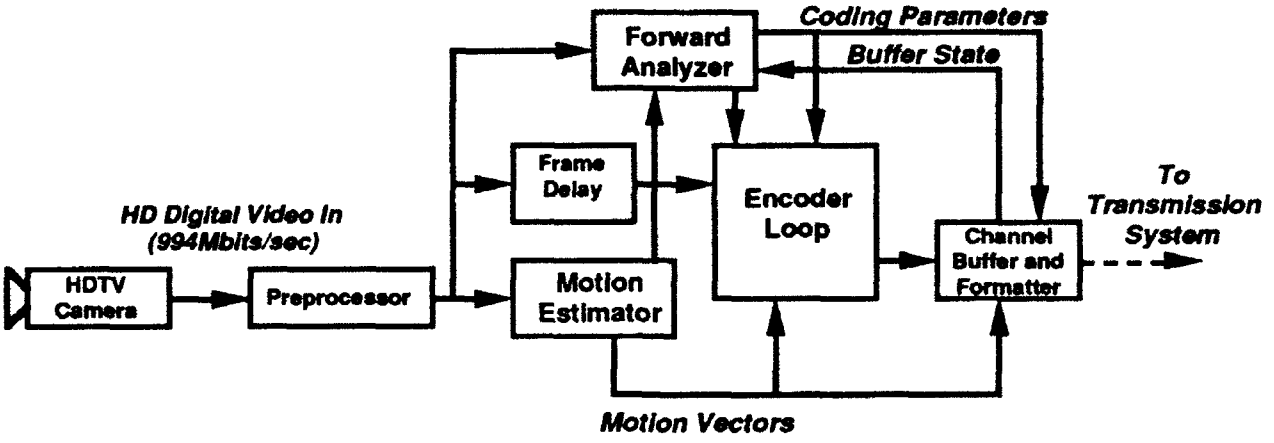


Figure 1. Video Encoder

The motion vectors, compressed DCT coefficients and other coding overhead information are buffered and packed into a format which is highly immune to transmission errors. The importance of each packet is computed and the most important packets are transmitted using a more robust mode subject to encoder buffer constraints. In case of transmission errors, the decoder uses a set of recovery techniques which mask the errors. A usable picture is always obtained even if all of the packets which were transmitted using the less robust mode are lost. If complete loss of signal is detected or the channel is changed the decoder switches to a special mode which quickly builds the picture to full quality after signal recovery.

The video decoder is shown in Figure 2. The vast majority of the codec complexity resides only in the encoder. The motion estimator, forward analyzer, perceptual quantizer selector and DFD encoder are encoder only subsystems. The decoder is realizable in a small number of VLSI chips. Transparent image quality is achieved while memory and complexity in the receiver are minimized.

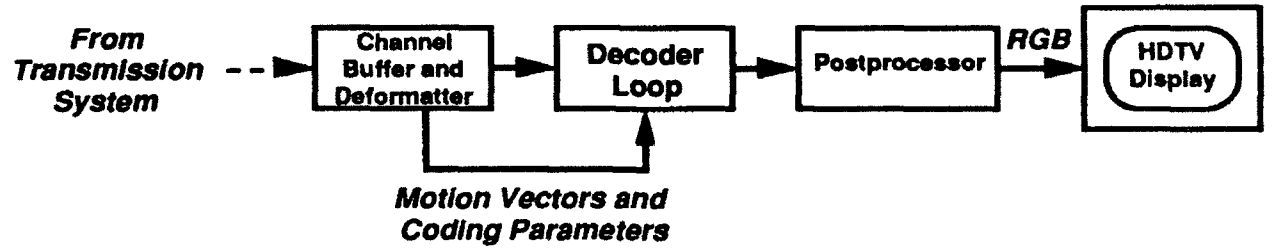


Figure 2. Video Decoder

Thursday

July 30, 1992

ThA: Digital Transmission Technology

ThB: Analog Systems II

ThC: Linearization & Harmonic Distortion

ThA1 COMPRESSED DIGITAL VIDEO FOR PASSIVE OPTICAL NETWORKS

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The Motion Picture Experts Group (MPEG) is presently developing at least two standards for full-motion compressed digital video [1]. MPEG1 aims at a 1.5 Mb/s data rate which is compatible with DS1 transmission as well as CD-ROM and DAT transfer rates and provides "VCR quality" video. A second standard (MPEG2) is targeting for a data rate of 4-5 Mb/s and an image which will be equivalent to "high quality CATV." This paper addresses the design of a video overlay network for a PON/FTTC architecture which uses MPEG2 to deliver both broadcast and switched video services on a single optical carrier.

Transmission Experiment: Experiments have been carried out [2] using a conventional 1.3 μm Fabry-Perot lasers and PIN/50 ohm receiver to transmit 94 unmodulated subcarriers having 6 MHz channel spacings and a CNR of 20 dB. Results [2] show that a receiver sensitivity of -23 dBm can be achieved with no degradation from either RIN or intermodulation products. A CNR of 20 dB is sufficient for transmitting either two or four MPEG2 video channels per subcarrier if QPSK or 16-QAM, respectively, is used. This experiment demonstrates the feasibility of transmitting 200-400 MPEG2 video channels using low-cost opto-electronic components. The ONU, consisting of a photodiode, amplifier, and electrical splitter, is as simple as possible for a video network. The transmission will be very robust against transmission impairments because of the low CNR requirements.

MPEG2 Overlay for PON/FTTC: The 23-26 dB link budget is sufficient for PONs with a 1x16 splitting ratio. With a FTTC architecture, 64 to 128 subscribers can be provisioned on each "fiber loop". To prevent theft of services and to improve operational efficiency the MPEG video should be encrypted. The decryption

keys can be transmitted directly in real-time to the subscribers set-top box in response to service requests or program orders. In addition to low-cost transmission, this approach offers a number of significant economies.

(1) Broadcast and switched services are transmitted on a single optical carrier. (2) By transmitting all signals to all subscribers, remote service provisioning can be achieved by transmitting appropriate decryption keys to the subscriber's set-top units, whenever service changes are requested. (3) The switched video access line can be shared on a statistical basis to achieve "video line concentration".

Video Line Concentration: In most previous proposals for switched video services, a fixed number (typically 2-4) of switched access lines are dedicated to each subscriber. By allocating video access lines in real-time as program orders are received, the number of access lines installed can be matched to the peak usage. Thus for a 25% peak usage rate, only 32 access lines to are needed on a fiber lop serving 128 customers. In the conventional approach of provisioning dedicated access lines 128- 256 lines might be required. As usage of switched video service increase, the number of access lines provisioned on each line can be easily increased by adding additional subcarrier frequencies at the video central office.

An MPEG2 video overlay for PON/FTTC architectures thus offers considerable advantages over previous proposals using AM-VSB, FM or more conventional baseband digital transmission systems.

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(2) G. Joyce and R. Olshansky, Photonics Tech. Letts., 665-667, June 1992.

ThA2

NOVEL CLOCK AND CARRIER-RECOVERY CIRCUITS FOR MULTIGIGABIT/sec LIGHTWAVE SYSTEMS

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The carrier reference and LO laser AFC are often derived from a residual optical carrier [1] while clock recovery techniques often depend on sufficient transitions to isolate the clock and use PLL [2] or special filters [3]. One expedient clock recovery method employed a clock pilot-tone transmitted with the data and then extracts the clock at the receiver [4]. In this paper we describe a novel technique that was used to simultaneously recover the reference carrier for n-PSK synchronous detection, a pattern-independent clock, and the heterodyne detection LO laser AFC reference, from a transmitted clock pilot-tone in two very different multigigabit/sec heterodyne detection systems. The technique to simultaneously extract the three processing signals was used in a 8 Gb/s subcarrier multiplexing (SCM) QPSK heterodyne detection system [5] and in a 4 Gb/s baseband BPSK polarization division multiplexing (PDM) heterodyne detection system [6]. This is the first detailed description of the technique.

The clock at the transmitter originates from a crystal-locked 2 GHz source. The clock is used at the pattern generators and either power combined with the modulated subcarriers in SCM case or combined directly with the PDM baseband data with a novel directional coupler. The directional coupler uses two asymmetric coupled microstrip transmission lines and two frequency selective transformers in the coupled ports. The coupling section consists of a low impedance quarter-wave transmission line and is connected at both ends to tapered microstrip transformers. The main line of the coupler is a 50 Ω microstrip transmission line. The received power spectra are shown in Fig. 1b and 2b, for the SCM and PDM cases respectively.

In the SCM case, the optical beat and the pilot-tone are mixed to recover the clock reference. The clock reference is used to phase-lock a VCO operating at the clock frequency. A 6 GHz reference subcarrier is recovered by doubling the clock and mixing the result with the clock (x3), and then mixing the x3 signal with the optical beat (IF). The IF is locked by comparing to an external standard and using the result to phase-lock the receiver LO laser.

In the case of baseband BPSK, the IF is suppressed. Mixing the two received pilot-tone signals, resulted in a term at twice the transmitted clock or 4 GHz. A frequency-divider recovered the 2 GHz data clock thus eliminating the need for a conventional clock recovery circuit. The 10 GHz IF for BPSK demodulation was determined by mixing the recovered 2 GHz clock with the 8 GHz external standard. The LO laser was phase-locked by comparing the received 8 GHz pilot-tone to the 8 GHz external standard.

The output of the AFC first-order loop filter was sent to the receiver LO laser controller resulting in ±20 Hz of IF stability for both the SCM and baseband cases. The degree of stability is a function of the loop filter parameters and the quality of the external standard. The IF stability established the stability of both the clock and the carrier reference. Since the clock is sent as a pilot-tone, the ability to recover the clock does not depend on the data pattern. The receiver sensitivity results for both the SCM and baseband cases were identical to data taken using a clock tapped from the transmitter.

A novel technique to simultaneously extract the reference carrier, a pattern-independent clock, and the AFC reference, from a transmitted clock pilot-tone has been used in a 8 Gb/s SCM-QPSK and similarly in a 4 Gb/s baseband BPSK-PDM heterodyne detection systems. This work has been partially funded by the Office of Naval Technology Program on ElectroOptics through the Naval Research Laboratory.

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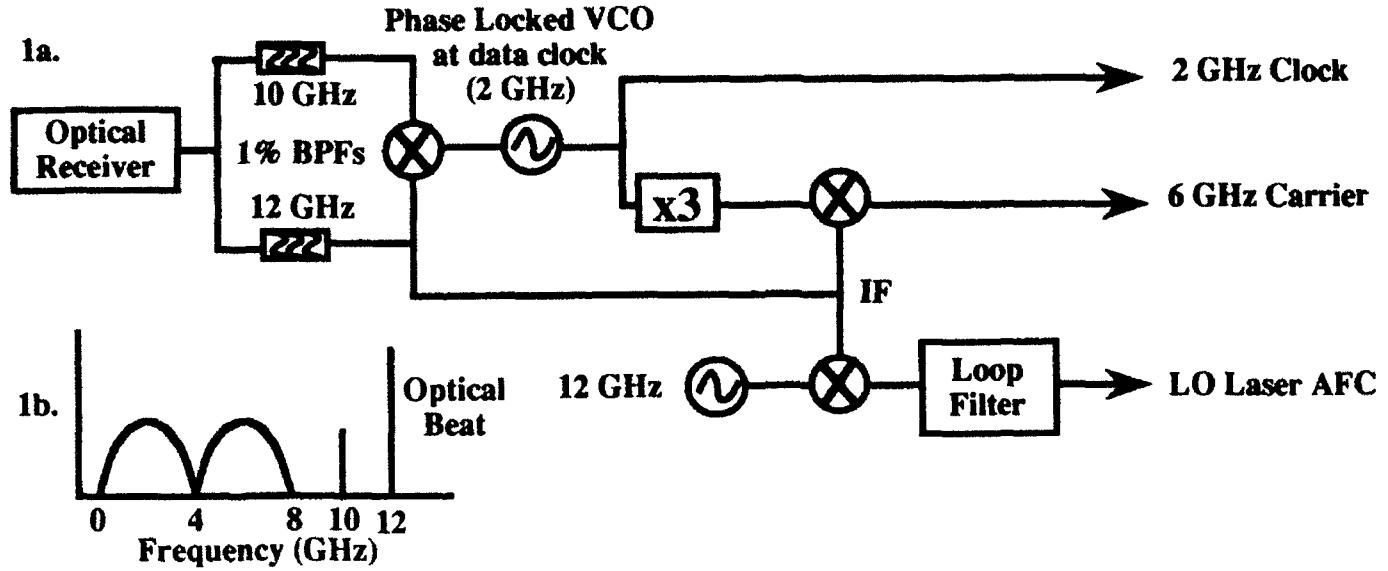


Fig. 1 a. Block diagram of circuit to extract AFC, demodulation reference, and clock for a 8 Gb/s QPSK-SCM system. b. RF spectra showing two 4 Gb/s QPSK channels, received clock pilot-tone at 10 GHz, and 12 GHz optical beat frequency.

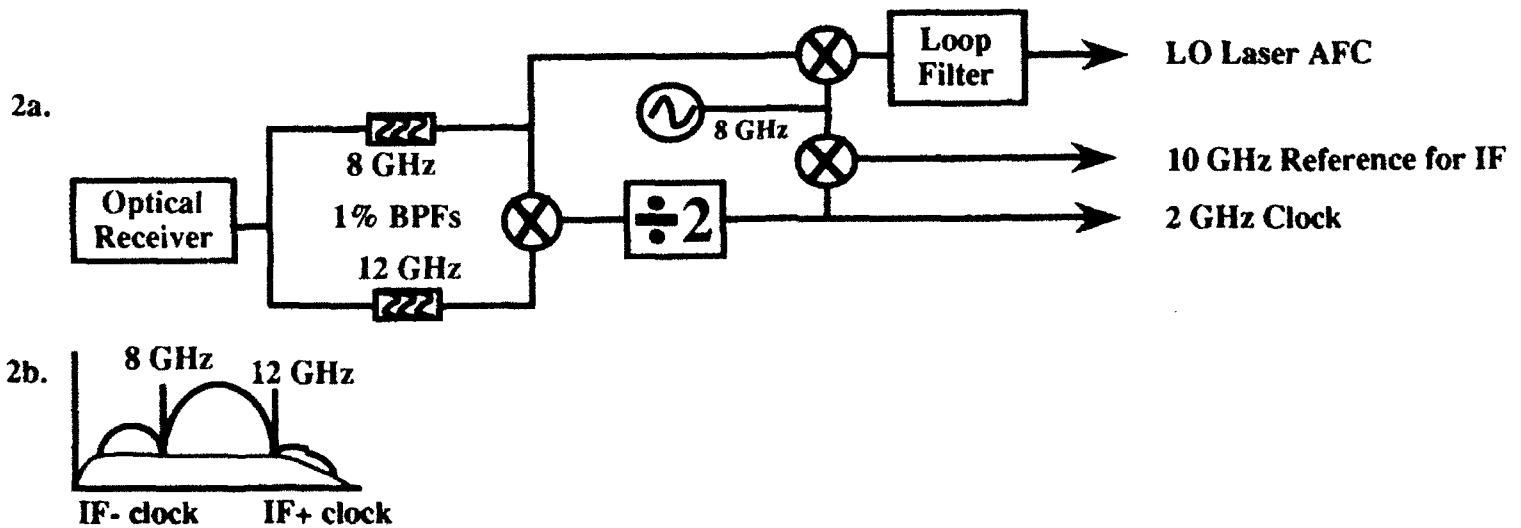


Fig. 2 a. Block diagram of circuit to extract AFC, demodulation reference, and clock for a 2x2 Gb/s polarization division multiplexing system. b. RF spectra showing 2 Gb/s baseband BPSK and received clock pilot-tone at {IF±clock}.

ThA3 EQUIPMENT DESIGN CONSIDERATIONS FOR HIGH SPEED DATA AND DIGITAL VIDEO TRANSMISSION

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Abstract

With the enormous bandwidth and low loss of fiber, why is it necessary to use anything more complex than simple on/off keying, or frequency shift keying for data transfer? The answer in most cases is because the fiber is only a portion of the system. Linear Amplitude Modulation is one of the most difficult transmission techniques for fiber but is used in cable T.V. because T. V. receivers accept AM signals. Any other signal format would require conversion hardware for every TV set on the system.

A modulator - demodulator pair (MODEM) to do a specific job could be designed in any number of ways. How do we select the best one? If the justification for the design is singular and cost is no problem, one design may be selected, but usually that is not the case and a design is only justified if the usage will be wide spread. Cost is usually a factor as well.

Given a specific task to perform, usually more than one solution presents itself. For example, a television picture can be reproduced exactly by sampling at 14.3 Mhz. with 8 Bit resolution generating about 115 Megabits per second. Equal or slightly better performance can be obtained by sampling at 10.7 Mhz with 9 Bit resolution. This results in a data rate of 97 Mb/s.

Knowing the bandwidth and characteristics of the transmission channel and the desired data rate, a transmission method may be selected. Channel bandwidth and data rate establish the minimum complexity of the system. A power limited satellite channel will typically support 24 Mhz BW and better than 8.4 db C/N with a reasonable size dish. From the chart in Fig. 1 BPSK would yield an expected Bit Error Rate (BER) of 1×10^{-4} BPSK supports about 0.8 Bits per Hertz or 19 Mb/s in a 24 Mhz. bandwidth. If a higher data rate is needed, QPSK can double the data rate but a 3db greater C/N is required. The same amount of data could be sent down a 6 MHz. wide channel in a CATV system but we would need a better C/N and we must use a more complex signaling structure.

System design trade-offs are selected using various criteria.(1) The decision process must take into consideration the desired (required) data rate, the channel characteristics, the acceptable bit error rate, the acceptable complexity, the permitted cost and, to some extent, the system designers experience. The channel characteristics include gain response, loss based on available transmission power, bandwidth, frequency dependent time delay, modulator, amplifier

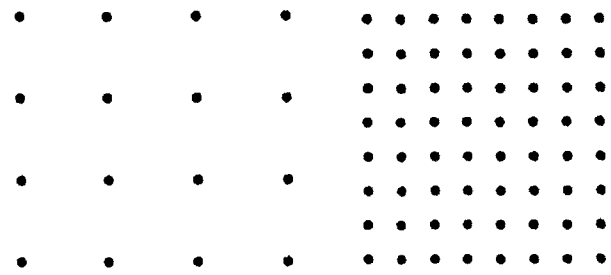
and detector distortion. The acceptable BER is the net result of noise and distortion in the channel and error detection and correction capability. It is possible to improve a 10^{-3} BER to 10^{-9} BER in a consumer priced system. The data rate penalty is about 1/4 loss of the total bit rate. The channel capacity is a complexity and power issue. QPSK works well in power limited satellite systems where the transponders operate with some signal amplitude compression.(2) A QPSK detector can be as simple as a delay line phase detector which compares the present incoming carrier phase with that of the signal delayed by 90°. The integrated result is the data output. Unfortunately the satellite signal is far too noisy to use this technique directly and complex phase lock loops (PLL's) are necessary to create a good phase reference for demodulation and sampling of the incoming data. Decision directed carrier recovery loops and the Costas loop are classic PLL's used for this purpose. (3) Bandwidth limited systems in which adequate power can be transmitted with linear response enables the use of modulation techniques using both multiple phase and amplitude levels. 16 QAM has 4 possible amplitude levels on each of 2 carrier phases. This permits sending twice the data of QPSK in the same channel or conversely the same data in half the bandwidth. This is because the four levels are represented by 2 data bits. The next level is 3 data bits (8 levels per phase) for 64 QAM. This in only half again the data etc but 4 data bits per phase yielding 256 QAM would double the 16QAM rate. The constellation patterns of Fig.2 show possible data locations. Remember that each location is the instantaneous amplitude and phase of a analog wave form. The distance between these locations, known as the Euclidean distance, is the resolution necessary for correct detection in the presence of noise and distortions. There is a class of coding, which produces what are known as cross-constellations, Fig. 3. This uses memory and extra data overhead but can well be worth the effort. So-called Trellis coding can be used to create cross constellations such as 32 QAM. Optimum detection is usually achieved via a Viterbi decoder to detect the most likely data value. Another help in detecting the most likely data value is to use a gray code in the Analog to Digital (A/D) process since this changes a maximum of one bit for the minimum detectable amplitude change. In a similar manner, the data bits are often differentially encoded to prevent interchanging the I and Q channel data during demodulation.

In order to recover data from QAM signals we must first lock to the carrier with a carrier recovery PLL. We must then lock to the data symbols to digitize them. Assuming that this is accomplished, we must determine which of the quadrature phases are which, and to complicate the issue, there is usually 50/50 chance that the data is inverted. In some systems in which the data is sent on both phases of the carrier, it is possible to have earlier bits arrive later at the decoder.

In systems using block error codes, it is necessary to detect a synchronize code to know where to start and to separate data and Forward Error Correction (FEC) bits. If this isn't complex enough, consider that a long string of zeros or ones might cause the clock recovery PLL's not to operate properly because the PLL does not see a regular sequence of phase or amplitude changes. To minimize this we generally incorporate a scrambler. This bit mixer is not to be confused with the bit mixing resulting from the intentional encryption necessary for data intelligence security.

	C/N for 10^{-4} BER	BITS/Hz
on/off	12	0.8
BPSK	8.4	0.8
QPSK	11.6	1.8
16QAM	18.6	3.1
64QAM	25.0	5.0

Fig. 1

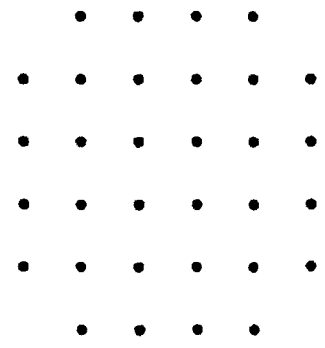


16 QAM 64 QAM

Fig. 2

Conclusion

This paper has presented some of the design considerations for high speed data transmission. The data associated with digital television is so compressed in that upwards of 120 MB/s is often compressed to less than 2 MB/s. This means that a single uncorrected bit error can create disastrous results. The good news is that FEC and adaptive equalizers are realizable at nominal expense to make even consumer digital T.V. viable.



32 QAM

Fig. 3

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ThA4 BROADBAND ISDN DELIVERY SYSTEMS AND TECHNOLOGIES

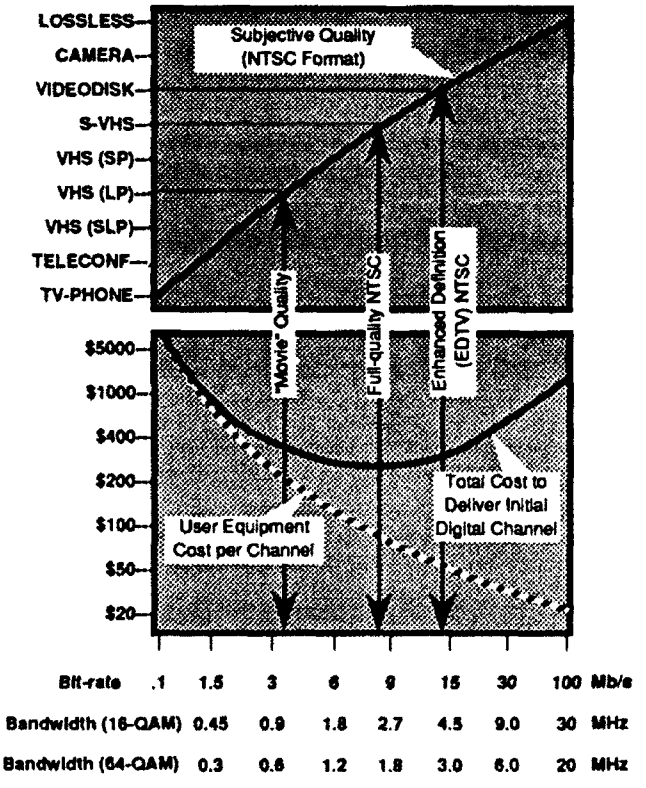
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BISDN Driving Forces

Switched on-demand video is expected to become the major bandwidth driver of BISDN. Two-way video telecommuting, televisiting and tele-education services could together represent a further and substantial multimedia bandwidth demand. High Speed Data, such as FDDI between locations, or the remote operation of a single CAD terminal, are also likely new applications for BISDN. Graphics images such as X-ray or CAT-scan in the medical field or high resolution color imaging in the printing and publishing business both need extremely high bit-rates. However it is future digital video which is the dominant BISDN network driving force, particularly for on-demand entertainment services, but also for interactive visual services in both residential and business applications.

Digital Video Compression

The bit-rates needed to achieve a range of subjective video qualities is shown in the graph below. The dotted cost curve in the lower portion of the graph shows estimated user equipment (digital video tuner/decoder) cost per channel for different bit-rates. The solid cost curve shows that to deliver digital video and audio to the television set, (including transmission and user equipment, in fiber-fed co-ax or twisted pair delivery systems), a bit-rate of around 8 Mb/s gives the lowest cost and offers at least S-VHS quality (no "ghosts", "echoes", "snow" or interference patterns.

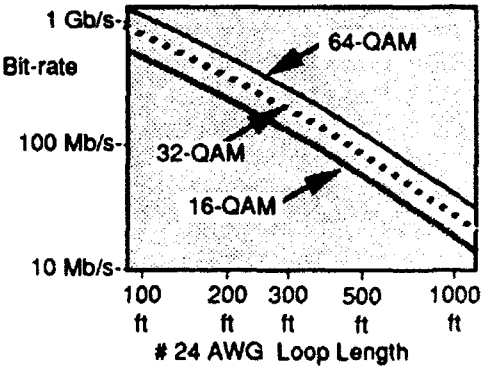


Digital Modulation

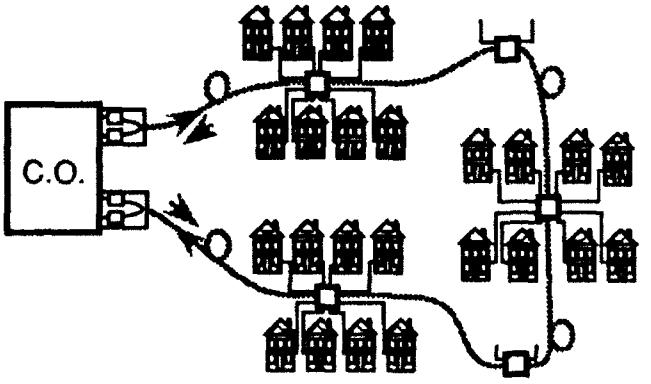
Quadrature Amplitude Modulation (QAM) is an efficient, spectrally compatible and popular modulation scheme for digital delivery on media having limited bandwidth, such as co-ax or twisted pair cables and wireless. QAM using a full matrix of modulation states and practical filters provides a spectral efficiency of about 0.84*Log2(n) bits/sec/Hz, where n is the number of possible modulation states for a single symbol. For example a 4 bits/symbol signal having 16 possible states (16-QAM) has a spectral efficiency of approximately 3.36 bits/sec/Hz. A more optimum arrangement uses a sub-set of possible matrix points, usually in a more circular rather than rectangular grouping. For example, 32-QAM provides around 4.2 bits/sec/Hz and requires a transmission performance very little more than that needed for 16-QAM.

Short Twisted Pair BISDN Delivery

Telco-provided twisted pair drops and home telephone wiring have considerable digital capabilities using QAM if their lengths are kept short. The diagram below shows potential capacity vs. length.



BISDN services can be more easily provided on a separate twisted pair per home. However where a second pair does not exist, it is possible to combine existing telephone and BISDN within a single pair. The diagram below shows a fiber ring system used to deliver large volumes of highly reliable service to the twisted pair drops.



In this system signals flow unidirectionally, with idle or "dark" timeslots provided for "upstream" traffic or control. In the event of fiber damage, two-way transmission can be maintained in each part of the separated ring using time-compression multiplexing techniques.

At least three high quality digital TV channels (or as many as seven movie quality channels) per loop can be achieved using 32-QAM at a maximum loop length of 800 feet. At this loop length in typical suburban home densities at least twenty-four such loops can be served by each fiber ring fed opto-electronic curbside module.

Co-ax Cable BISDN Delivery

The North American Cable-TV industry is very aware of the tremendous bandwidth potential of its imbedded, now almost ubiquitous, co-ax cable distribution systems. Moreover, the now digital direction of HDTV has alerted the Cable-TV industry to the potential digital capabilities of its co-ax, not just for television channel capacity, but also for data, voice and telemetry services. Digitally extended bandwidth NTSC (or PAL) television transmission offers many of the attributes of HDTV but at much lower cost and with existing TV set and studio system compatibility. This approach could defer, potentially, the need and thus expense of HDTV for some time while, at the same time, providing a smoother path for its eventual introduction.

Analog fiber optic transmission systems are already being deployed rapidly and universally by Cable-TV operators in their local feeder and trunk distribution networks to reduce service outages, decrease maintenance costs and to increase video performance. Fiber feeder cables already being deployed and planned by Cable-TV operators typically contain a large proportion of spare fiber strands. Some of these strands may be used to increase video channel capacity or to provide upstream paths for two-way services. Other fiber strands may be utilized, at very low cost using lasers carrying only QAM digital signals, to provide BISDN and even greater digital TV channel capacity within a configuration such as that shown in the diagram below.

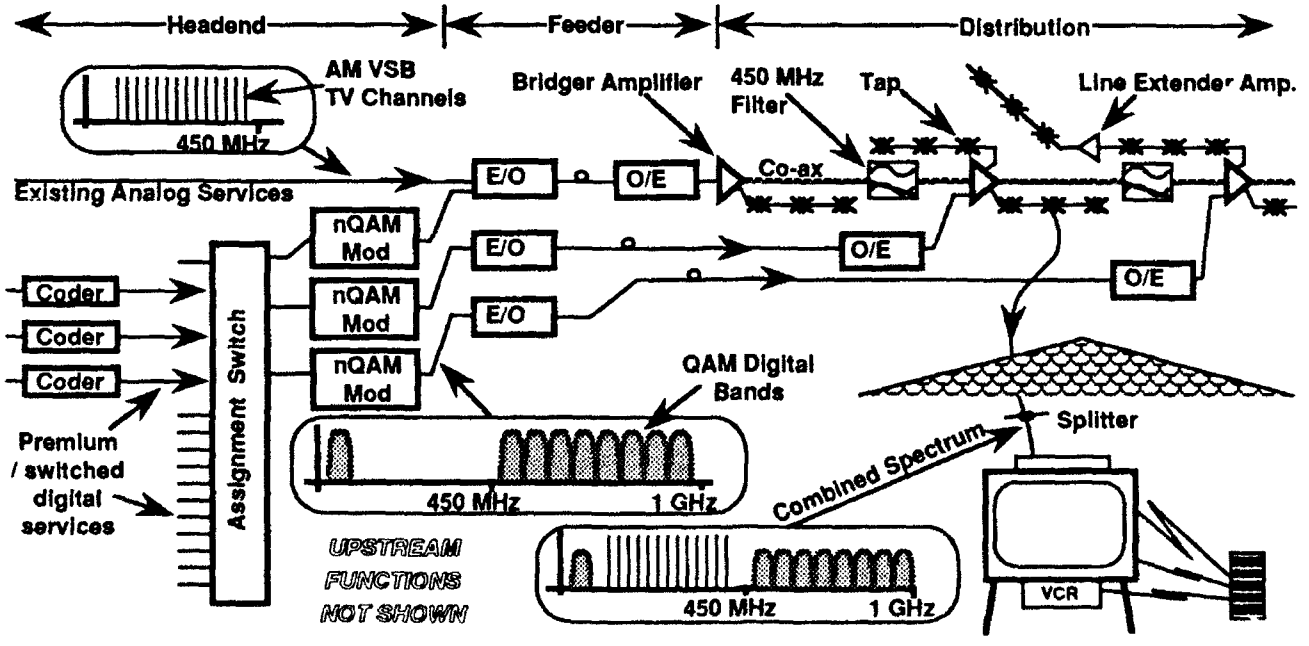
Future digital television sets will require single QAM and video compression standards, regardless of who delivers the services. Digital set-top converter technologies will migrate into television sets, VCRs, PCs, etc. Eventually, as is now happening during todays analog Cable-TV era, digital set-top converters will themselves become redundant.

Some Observations

Fiber-fed Cable-TV co-ax and Telco-provided, fiber-fed, short twisted pairs both offer potential BISDN capabilities. Both serve or pass at least 95% of North American TV homes and both have the potential to provide an abundance of switched digital video and other BISDN services.

Cable-TV operators have advantages in time, economics and entertainment service infrastructure. Cable-TV fiber feeders are already being deployed universally as a means of reducing cost and improving quality for existing services. This fiber deployment has the potential to provide an "already paid for" base for future BISDN capabilities. In contrast, the Telcos must fund deployment of new fiber and BISDN loop interfaces entirely from future new service revenues. However the Telcos have the advantage of existing network infrastructures needed for "dial-tone video" services, particularly in areas of signaling, numbering plan, built-in operations and maintenance facilities and message accounting.

The two likely BISDN delivery network operators thus have a set of complementary business, technical and imbedded-base capabilities. Their future collaboration could be the key to rapid, effective and economic deployment of BISDN, particularly for on-demand video.



A digitally overlaid Cable-TV distribution system

ThA5 TRANSPORT OF DIGITAL VIDEO ON TELEPHONE SUBSCRIBER LINES

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1. Introduction

If wire pairs can be used to provide wideband access capabilities, "broadband services" may be introduced long before the full penetration of optical fiber in the loop plant. Asymmetrical Digital Subscriber Line (ADSL) is an emerging technology for providing high bit-rate channels to the residence, and is the focus of this paper.

2. ADSL: A New Wideband Access Capability

ADSL (Fig.1) consists of a pair of copper wires from either the central office (CO) or the remote terminal (RT) to the subscriber, together with the necessary interface equipment. Initial ADSL systems are projected to contain: 1) A 1.5 Mb/s one-way channel going from the CO/RT site to the subscriber; 2) A two-way, low-speed data channel; 3) A bidirectional POTS (Plain Old Telephone Service) channel or possible an ISDN Basic Rate Access (BRA) channel.

3. Candidate Technologies For ADSL

The technologies for ADSL are based on passband pulse amplitude modulation (PAM) and adaptive equalization. Adaptive equalization allows different loop characteristics to be accommodated without manual adjustment. Passband modulation allows frequency multiplexing of the POTS, the low-speed data channel, and the high-speed channel. An example of spectrum allocation puts the POTS channel in the <4 KHz baseband, followed by about 40 KHz of bandwidth for the BRA ISDN channel and the upstream control channel, and places the downstream high-speed channel (time-division multiplex of the 1.5 Mb/s channel and the low-speed control channel) above 50 KHz.

For passband modulation of the high-speed channel, a well-known technique is Quadrature Amplitude Modulation (QAM), which uses a sinusoidal carrier to modulate the digital information signal into the desired passband. Because of the spectral compatibility requirements, the peak signal level at the transmitter is limited (e.g. 3 volts). Given the constraint in the signal amplitude (and thus energy), other parameters considered in QAM are the bandwidth (W) and the number of signaling levels (L). Generally, a larger L increases the bit rate at the expense of the probability of symbol error. On the other hand, increasing the bandwidth does not increase the capacity proportionally due to the channel attenuation and noise effect. Thus there is a tradeoff between W and L. The optimal values depend on specific loop characteristics. However, L=16,32, and 64, have been shown to perform close to optimal for a bit error ratio of 10^{-7}. The corresponding bandwidths will then be about 400 KHz, 300 KHz, and 267 KHz respectively.

A typical ADSL system using an L-level QAM is shown in Fig.2. Referring to Fig.2(a), the input binary digits are first split into two bit-streams. The binary digits in both streams are grouped into $\log_2 L$ bits which are then coded into two L-level amplitude symbol sequences a_n and b_n with a symbol period of T seconds. The pulse-amplitude sequences are then shaped by transmitter lowpass filters before modulated to a passband signal centered at a carrier frequency of f_c. The modulated signal is then launched onto the loop wire, which is modeled as a linear dispersive channel with impulse response $h_c(t)$. A commonly used model for the wire pair has the characteristic that the attenuation ($H_c(f)$) varies according to the length of the loop (l) and the square root of frequency (f) given by, $|H_c(f)|^2 = e^{-K_c l\sqrt{f}}$, where K_c is a constant. For ADSL, the noise model is made up of three parts: self-Far-End CrossTalk (FEXT), impulse noise, and Additive White Gaussian Noise (AWGN). The power spectral density of FEXT can be modeled as: $S_{FEXT}(f) = P_s K_F l f^2 |H(f)|^2$, where P_s is the total power spectral density of the interfering signals belonging to the same binder group (with 50 wire pairs) and $H(f)$ is the frequency response of the equivalent baseband channel, and K_F is a constant. Impulse noise causes burst errors which can last up to milliseconds and thus may need forward error correction to reduce degradation.

At the receiver, the incoming signal is first demodulated into the baseband in-phase and quadrature components. The lowpass filters in the demodulator are used to reject the double frequency component caused by the shifting of the passband signal to baseband. After demodulation, the baseband signal is processed by the receiver filter $r(t)$ and the adaptive equalizer. As shown in Fig.2(b), the receiver filter can be considered to be made up of two parts: A noise whitening filter that makes the FEXT look like a white noise; and a matched filter that optimally filters out the noise. After the receiver filter, the signals are sampled at interval of T seconds (baud-rate) to obtain the discrete time signals, which are then equalized by a Decision Feedback Equalizer (DFE) for reducing the effect of intersymbol interference (ISI) resulting from the dispersive wire channel. The DFE attempts to remove the ISI with a combination of a linear feedforward filter (FFF) and the feedback filter (FBF). Because the ISI may be caused by both the in-phase and quadrature components, both the FFF and the FBF can be considered to have complex coefficients. The forward filter reduces the precursor ISI which is the result of the interference from future symbols. Due to its non-causal nature, the forward filtering requires signal delay for implementation. The feedback filter attempts to correct the postcursor ISI (interference from past symbols) based on the detected symbols. The DFE usually outperforms the linear equalizer since the feedback section is free from noise (assuming no undetected errors).

The ADSL system is capable of adapting itself for different loop characteristics by adjusting the coefficients of the linear FFF and FBF of the adaptive equalizer. The adjustment can be done in real time and is based on the error signal e_n and the symbol estimates $\{a_n, b_n\}$ according to the minimization of the minimum mean square error. Further improvement in performance can be achieved by using a sampling rate higher than the symbol rate. The resulting structure is called a Fractional Spaced Equalizer (FSE). For implementation convenience, an integral multiple of the nyquist rate is usually used. The FSE can perform both the functions of the receiver filter and the forward filter portion of the DFE. In addition, it is less sensitive to the receiver sampling

phase and alleviates the effect of aliasing as a result of the baud-rate sampling of the received signal.

4. A Possible Evolving scenario For The Access Network

The evolution from a copper loop to an all-fiber access network will probably involve a combination of two important technologies: Advanced digital subscriber loop (DSL) and Fiber-to-the-home. A possible evolution scenario is depicted in Fig.3. Initially, conventional analog copper loops carrying services such as POTS and data on modems will start to migrate to digital subscriber loops using the same wire pairs to provide ISDN (2B+D) services. Basic rate ISDN provides a bit rate of 128 Kb/s with 16 Kb/s signaling capabilities. At this rate, visual communication service using H.261 (p=2) becomes a reality. The next cornerstone is the introduction of the ADSL technology around 1993-1994. ADSL would allow the offering of many "modern age" services which cannot be supported with the conventional copper loop. The introduction of these new services will give residential subscribers a "taste" of what an advanced communication network can offer and subsequently stimulate the demand for more advanced services.

As the technology for ADSL matures and the service demand increases, it will be possible to provide upgraded services such as bidirectional high-speed services, high quality videophone, and NTSC-quality videos, over a shorter loop distance (e.g.<9Kft). One way to shorten the copper loop distance is to deploy fiber from the CO to a remote location, from where Very High-speed ADSL (VHDSL) technology that can support a variety of bit rates may be used.

While ADSL technology is used for the early introduction of new services, fiber will be deployed up to the pedestal (FTTC). Early FTTC deployment will mainly be focused in new construction areas or for the rehabilitation of old copper loops, and it will be likely to be driven by POTS and/or Basic rate ISDN services.

As advanced services proliferate, it become more economical to migrate the ADSL network to a fiber-based network. The experience gained from earlier FTTC deployment will make this migration easier. Similarly, the POTS-driven FTTC will be upgraded to support higher rate services. The last phase of the evolution involves the conversion of the last drop from wire pair (or coax) to fiber. This provides the largest capacity and is able to support digital HDTV as well as Broadband ISDN services eventually.

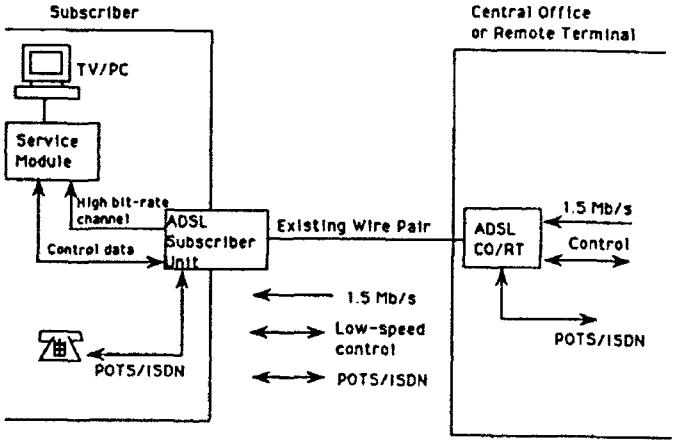


Fig. 1 ADSL System

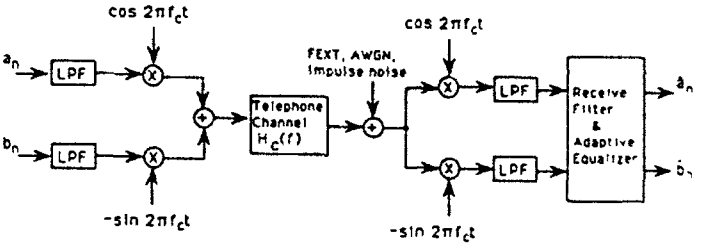


Fig. 2 (a) ADSL using QAM

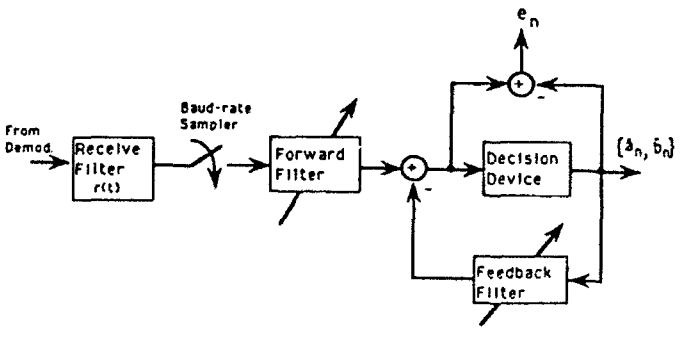


Fig. 2(b) Receive Filter and Adaptive Equalizer

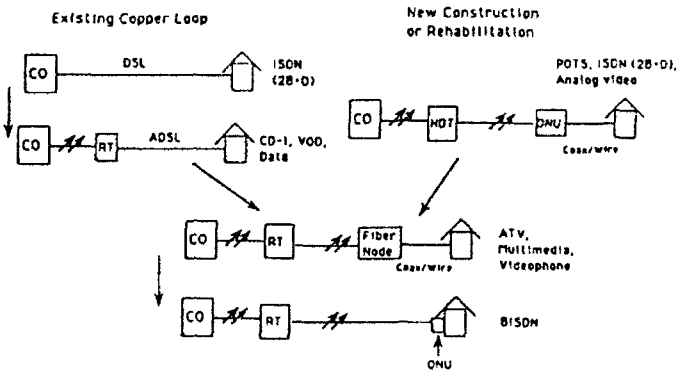


Fig. 3 An Access Network Evoultion Scenario

ThB1

SYSTEM ENGINEERING FOR EXTERNALLY MODULATED, ANALOG, FIBER-OFTIC LINKS

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To achieve optimal performance from a fiber-optic link, interactions with other components in a system must be considered. This paper will address three examples of system engineering for the analog fiber-optic link: (1) cascade calculations for RF gain, noise figure and dynamic range; (2) budgeting for heat loads and volume constraints; (3) reliability modeling. Each of these examples illustrates trade offs among component specifications...

An optical link itself will typically have a noise figure greater than that available in a good receiver. Therefore a low noise preamplifier is required to preserve the sensitivity of a receiver where a fiber optic link is connected to the antenna. The performance of this two-stage cascade (preamplifier plus fiber-optic link) is analyzed by combining gains, noise figures and intermodulation intercepts to determine total noise figure and third order intercept for the cascade. The dynamic range of the cascade is then determined by the total noise figure and intercept. The system noise figure can be made very low (practically equal to that of the receiver) if arbitrarily high gain is inserted before the fiber-optic link. Unfortunately, front end gain also lowers the total input intercept of the cascade (thus lowering system dynamic range) so a compromise must be made in selecting preamplifier gain. In any case, the dynamic range of the cascade cannot exceed that of the preamplifier and the noise figure of the cascade cannot be less than that of he preamplifier. Therefore, there is little value in improving the dynamic range of the fiber-optic link beyond that provided by electronic preamplifiers (typically between 100 and 120 $dB/Hz^{2/3}$.)

The mechanical design includes the laser, modulator, rf circuits, power and control electronics in a compact, outdoor, pole-mounted, weatherproof enclosure. The thermal design must maintain the laser heat sink at a temperature between 25 and 50 C and maintain the junction temperatures of the electronics below 110 C in an ambient ranging from -25 C to 50 C. This is accomplished by passive cooling via external heat exchanger fins for the electronics and a dual TE cooler cascade for the laser.

The failure rate of the analog link is modeled as the sum of the failure rates of the component parts. The major elements of this model are the pump laser, the lithium niobate modulator, the hybrid electro-optic assembly, rf electronics, and power supplies. There is no valid data for the modulator so its failure rate was estimated with data for SAW devices. The failure rate of the complete link is thus estimated to be at least 20 failures per million hours or an mean time to failure (MTTF) of 50,000 hours. A sensitivity analysis determines the significance of the laser and lithium niobate modulator. In this analysis the failure rate of the link electronics and packaging, without the laser and modulator, is estimated to be 4.4 failures per million hours. This number sets a rational goal for the reliability of the laser and electro-optic modulator since improvements to these components would not significantly improve the system failure rate.

This work was sponsored in part by the USAF Rome Laboratory.

ThB2 TWO SECTION OPTICAL FILTER WITH A 4 GHZ OPTICAL BANDWIDTH REALIZED WITH IN-FIBER BRAGG GRATINGS

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ABSTRACT

We present the measured data from a narrow bandwith optical filter that has a 4 GHz transmission bandpass. The filter is realized by cascading one reflection filter and one transmission filter. Both the transmission and reflection filters are based on in-fiber Bragg gratings.

SUMMARY

A two section optical filter was constructed as shown in figure 1. The in-fiber Bragg gratings[1,2,3] are induced by the photo refractive effect. Filter R_1 is a Bragg grating reflector with a 3 dB optical bandwidth of 70 pm. The reflection of this filter is R_1=0.37. The excess loss of the filter is less than 0.05 dB. The reflection spectra from filter R_1 is shown in figure 2. Filter T_2 is a Bragg grating with a 3 dB optical bandpass of 4 GHz. The excess insertion loss of this filter in the filter bandpass is measured to be 2.7 dB. The transmission spectra from filter T_2 is shown in figure 3. The fiber splitter converts the reflection function of grating R_1 to the transmission mode. The transmission spectra from the cascaded filter is shown in figure 4.

CONCLUSION

We have realized an optical filter with a very narrow optical bandpass. This filter can be used to remove excess spontaneous emission from optical amplifiers and the filter design can be

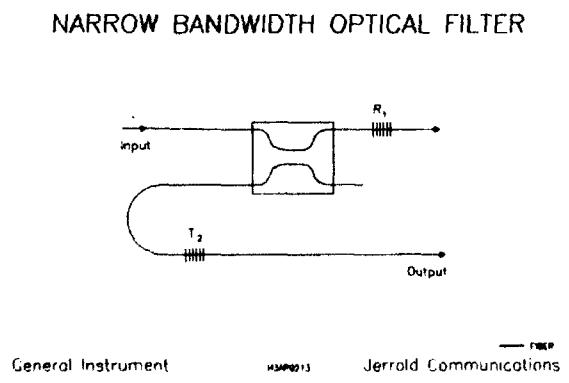


Figure 1. Optical Filter Configuration

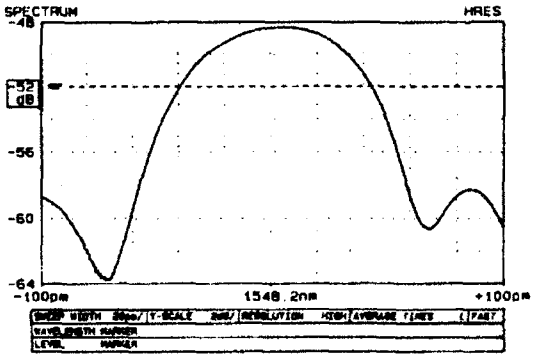


Figure 2. Reflection Characteristics of Grating R_1

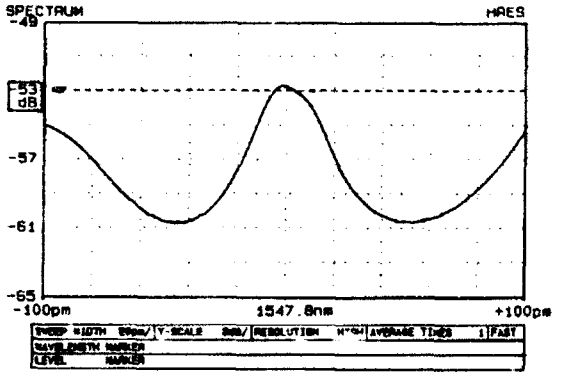


Figure 3. Transmission Characteristic of Grating T_1

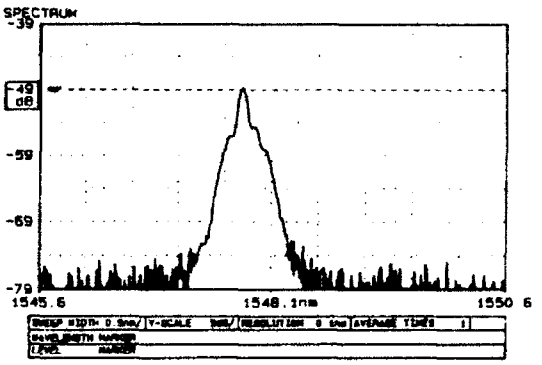


Figure 4. Transmission Characteristic of Composite Filter

readily adapted to wavelength division multiplexing. These filters will have general use in optical sensor and communication systems[4] that require narrow optical bandwidth filters. System applications will require temperature stabilization of the grating since the temperature coeffient is 13 pm/°C.

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ThB3 APPLICATIONS OF FIBER OPTIC RF AND MICROWAVE ANALOG LINKS TO ANTENNA REMOTING

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This paper will discuss applications of fiber optics to antenna remoting systems. Performance requirements/issues will be addressed in light of the application. Status of the technology and its ability to meet system performance will be addressed.

Paper not available at time of print.

ThB4 A BROADBAND VARIABLE TIME DELAY SYSTEM FOR TRANSVERSAL FILTERING AND PHASED ARRAY RECEIVE APPLICATIONS

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SUMMARY

A new optical implementation for a reconfigurable transversal filter is presented. One important application is for the control of a dynamic broadband phased array receive system. The system is illustrated in figure 1, where it is seen that a segmented mirror SLM is used as a means for steering light into a delay line array. Such an approach has several distinct advantages. The number of elements in a SMD can be quite large with the same number of filter/antenna elements (one for each SMD element) used. Despite its inherent simplicity, the system presented here has several advantages over other types of switched fiber delay line configurations that employ electro-optic switches as a means to select a particular delay. These switches tend to be quite lossy and inefficient requiring high power budgets. This has made extremely large order systems impractical since inefficient switching matrices are required. The present system provides a practical low loss variable delay line implementation for wideband (i.e. pulsed and chirped radar, spread spectrum, dual frequency, etc.) signal processing [1].

From figure 1 it is further seen that the RF signal is amplified and used to modulate light with any variety of modulation methods. The light is fiber coupled and sent to a collimating lens (a graded index or GRIN rod collimator is shown in the figure.) The light is polarized at the source such that it is reflected by a polarizing cube and directed onto the SMD. The modulated signal then reflects off the SMD elements where it makes a second pass through a quarter-wave plate. This configuration results in rotation of the polarization by 90 degrees. The light is now transmitted by the cube and sent to a lensing system. The SMD beamsteerer in essence directs the light at a particular angle (spatial frequency). The Fourier transforming property of the lens system produces a spatial impulse (focused beam) whose spatial position varies linearly along the x-axis as a function of the steer angle. An array of fibers, each fiber a different length (delay), is placed along the x-axis. The output of the fiber delay lines are summed and direct detected. In this way a (quantized) variable delay is obtained.

A single element proof-of-concept system was constructed on an optical bench. A linear array of eight multimode fibers were fixtured in a v-groove assembly. This provides a variable delay line system with 3 bit resolution. The fibers were cut to differential lengths of 2 feet to obtain about 3 nanoseconds of differential delay between adjacent fibers. A pulse generator was used to modulate a diode laser. Figure 2 shows the step response of the system for each of the eight delay lines (each trace has been vertically displaced one division for clarity) on a digitizing oscilloscope. For a typical phased array application, the ability to steer an aperture ±60 degrees in half degree increments requires 240 steps of delay which is approximately 8 bits of resolution. Lenses l_1, l_2, and l_3 are used to provide this resolution by magnifying the mirror tilt angle as well as to focus the reflected light from each mirror element onto a linear fiber array. Note that all time delay elements share the same set of delay lines.

Examining some typical numbers we find that if 256 50-micron diameter fibers constitute the linear fiber array (resulting in approximately a 1.25 millimeter width) then for a typical SMD displacement of 4 microns, using F_1 = 6.25 centimeters, F_3 = 5 centimeters, and F_2 = .5 centimeters would result in the 8 bit delay resolution required. In effect, the ratio F_1/F_2 provides the necessary demagnification and assures that the light focused into the fiber by F_3 is within its numerical aperture.

In conclusion, perhaps the single most important characteristic of the system discussed is its wide electrical bandwidth. In the phased array applications this eliminates the dispersive

beampointing error associated with narrowband systems known as squint. The SMD based system eliminates the large loss usually associated with switched fiber systems and allows for a practical implementation of a phased array antenna receive system with a large number of elements.

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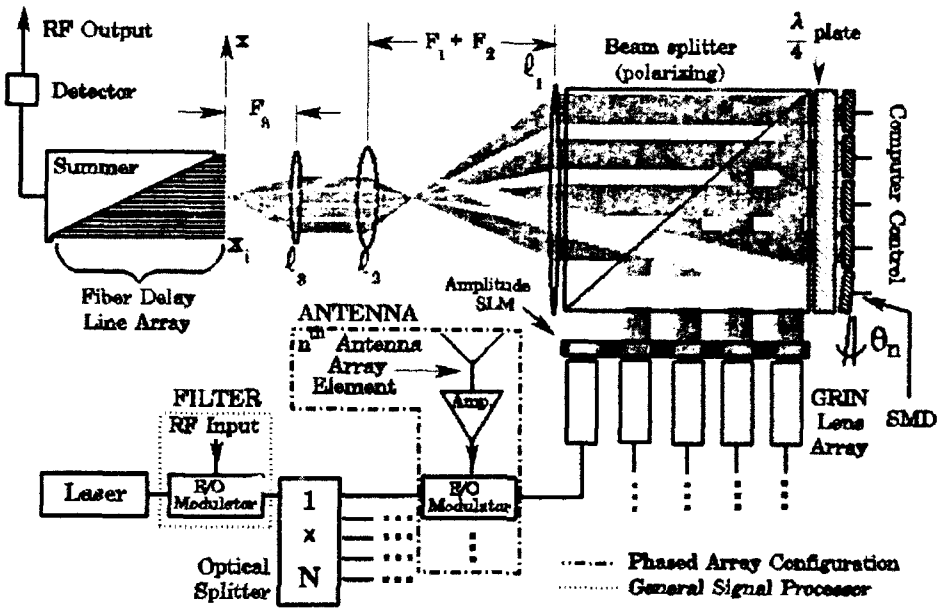


Figure 1: Wideband phased array receive system.

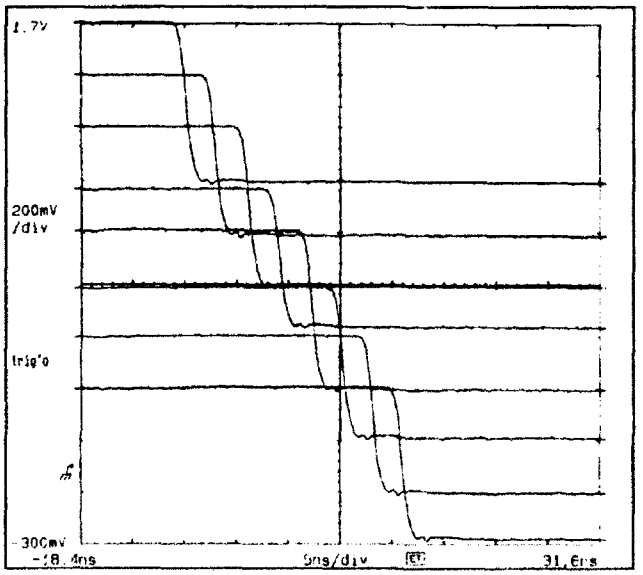


Figure 2: Step response for a 3-bit delay line.

ThB5 **HIGH-BANDWIDTH, HIGH-DYNAMIC-RANGE, ANALOG OPTICAL GUIDED-WAVE SYSTEMS FOR PHYSICS INSTRUMENTATION**

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Introduction

We have developed two remote measurement systems that efficiently exploit the information transmission capacity of optical guided-wave technology. The first system, which operates at 820 nm, was developed for nuclear weapons measurements and emphasizes high-bandwidth high-dynamic range information transmission. The second system was developed for the detector readout at the Super-Conducting Super Collider (SSC); this system emphasizes high charge sensitivity measurement transmission and operates at 1320 nm. Most of the component design (including modeling), fabrication, packaging, characterization, and system integration was done at LLNL specifically for these specialized physics measurements applications.

The Nuclear Weapons Diagnostic System—EXMOD

Our EXMOD (EXternal MODulation) system consists of a laser diode carrier source operating at ~820 nm, a high-bandwidth Mach-Zehnder (or Y-branch balanced-bridge) modulator, a ~1 km run of single-mode optical fiber, and a high-bandwidth streak camera recorder. This system is diagrammed in Fig. 1. The physics measurement requirements for the nuclear testing mission require very high bandwidth and high-dynamic range (the physical quantity being measured is the logarithmic derivative of the observable, this places severe stress on the dynamic range requirement). To achieve the current overall system bandwidth of ~6 GHz (transmitted real-time over a km of fiber) each component must be capable of high bandwidth operation: the modulators[1] are capable of over 20 GHz with V_π ~ 14 volts and the streak camera is capable of about 15 GHz response. However, the current streak camera readout, a Photometrics CCD camera, has only 576 samples in the time direction; this limited sampling and a desire to record

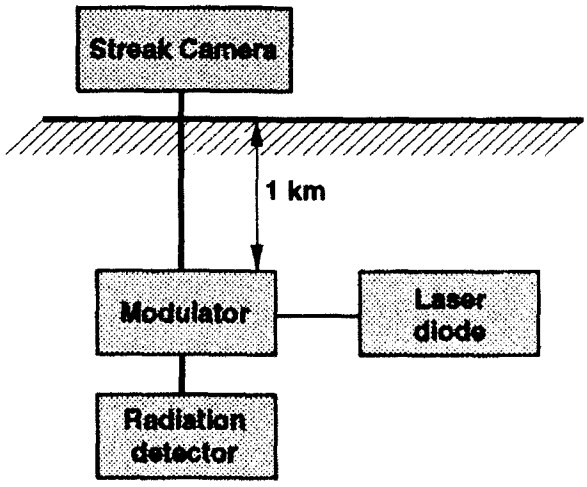


Figure 1. Block diagram of the EXMOD system.

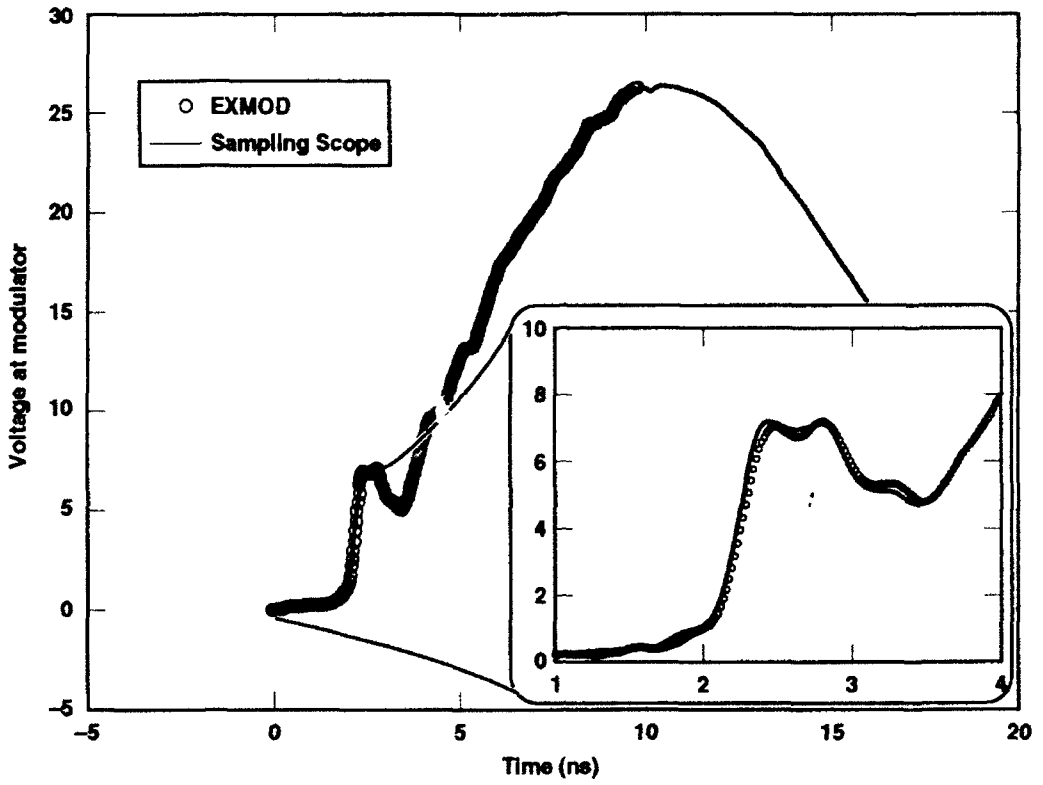


Figure 2. Comparison of sampling scope and EXMOD measurements

these single-transient events over as long a time a possible usually limits the effective streak camera bandwidth to ~ 10 GHz. Due to the rather severe chromatic dispersion in the silica single-mode fiber at 800 nm (100ps/nm-km), and the nearly transform-limited spectral broadening from the modulation, the fiber transmission is limited to an effective bandwidth of ~ 15 GHz (over this 1-km link with no dispersion compensation). The bandwidth of the transmission and recording system exceeds the bandwidth of our ionizing radiation detector in our current system.

We take advantage of the "excess bandwidth" (excess over the ionizing radiation detector bandwidth) to drive the modulators over many fringes. This multiplies the frequency content of the transmitted and recorded signal; however, it also effectively multiplies the dynamic range of the streak camera, ~40, times the number of fringes crossed, yielding increased system dynamic range.

The optical power present on the streak camera photocathode is generally limited to approximately 1 mW to ameliorate the bandwidth degradation from space-charge effects. To limit photorefractive damage effects we generally pulse the laser on for several microseconds before and after the signal to be measured is present.

Both the bandwidth and dynamic range are illustrated in Fig. 2. This figure compares the voltage signal from a calibration pulser measured in two ways. Before the diagnostic canister is buried for the event, we measure the time history of the calibration pulser—that measurement is the solid line in fig. 2. After the canister is buried very deeply in preparation for the nuclear event, the measurement system is exercised by the calibration pulser. The open circles depict the EXMOD system's remote measurement of the calibration pulser. It should also be emphasized that the EXMOD system's measurement is a single-transient measurement

while the sampling scope technique enjoys the freedom to average many pulses (in this case 1000). It is clear that the EXMOD system reproduces the pulse shape with extremely good fidelity; as the inset shows, some of the finer structure of the pulse appears more pronounced in the EXMOD measurement. The dynamic range is clearly over 100. *Thus, the EXMOD system demonstrates a (bandwidth) x (dynamic-range) product of over 600 GHz for each information channel.* It appears that the EXMOD measurement is higher fidelity than the sampling scope, even though it is single-shot, and remote.

The High-Sensitivity SSC System

Our instrumentation development work includes a system at 1320 nm for measurements at the Super-Conducting Super Collider (SSC). Here we use a YAG laser as our carrier source and rely upon the small capacitance of the Mach-Zehnder modulator, and high optical power to directly read the electrical charge output of high-energy physics detectors. The huge detector arrays envisaged to perform high energy physics (HEP) experiments at the SSC will have nearly 10^6 independent data channels that must operate in a hostile radiation environment that will be severely cramped—limiting the efficacy of cooling built-in electronics. Thus, approaches that minimize the presence of active electronic components are advantageous. Typically, these HEP detectors require electronic preamplification that allows their relatively weak charge signals to effectively drive metallic signal cables. Our approach may potentially eliminate the need for active electronics and radiation-scattering metallic cables among other advantages[2].

The block diagram of the SSC system appears in fig. 3. Here we operate the Mach-Zehnder modulators in the linear region of the transfer function. And drive the electrodes directly with the charge output of the HEP detector. By using the 1320 nm YAG laser we are able to achieve an extremely low-noise optical carrier in the frequency regions beyond the relaxation oscillation frequency[3]. We use a high-pass filter to eliminate any residual laser noise. Virtually the only remaining noise source in this system is statistical shot noise; we minimize this by operating at the highest possible optical power. However, due to saturation of the photodiode in the low-noise optical receiver we are limited to an optical power of 5.5 mW. The system bandwidth is determined by the modulator's bandwidth and the bandwidth of the optical receiver.

For these experiments we used our own in-house modulator (20 GHz traveling-wave electrode structure). Even though this short-electrode structure has a higher V_π than other modulators that were available, it is readily seen that for charge detection the length of the

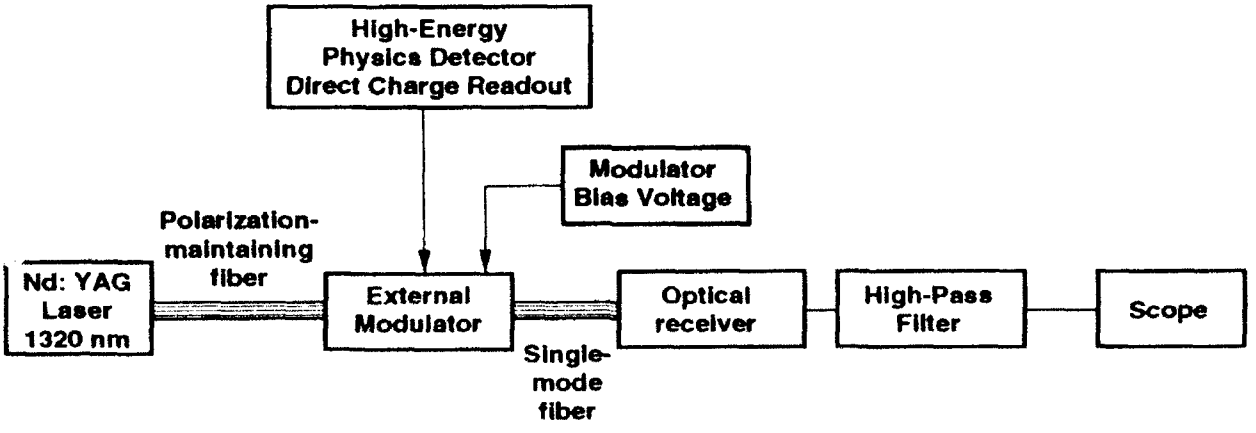


Figure 3. Block diagram of the high-sensitivity SSC data link.

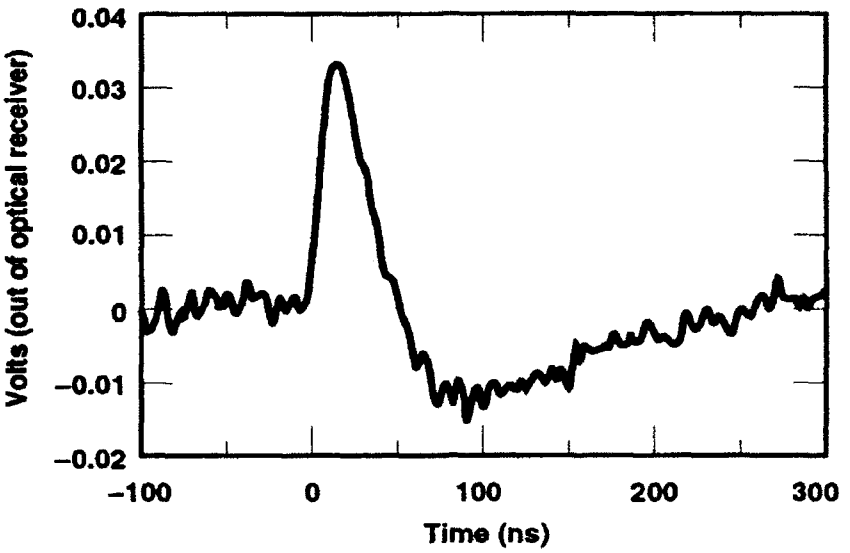


Figure 4. Response of the 100 MHz SSC link to a charge pulse from an ionization chamber detector.

electrode is irrelevant[4]. However, by altering our traveling-wave package we were able to terminate the modulator external to the package and experiment with optimum termination impedances. This optimum termination impedance is driven by the desire for high-bandwidth (low impedance for low RC time constant) on the one hand and the desire to minimize the rate at which charge is dissipated across the resistor (and therefore lost to effective modulation) on the other hand. A more complete description of these issues and the setup may be found in a forthcoming publication[5].

Figure 4 is typical data obtained from this high-sensitivity optical link. Here we are directly reading out a charge pulse from an ionization-chamber detector. The integrated charge from the detector was independently estimated to be 4×10^{-13} Coul. We measure the s/n ratio of this signal to be 23. Thus, we estimate the noise-floor of the charge measurement[6] is 17 femtocoulombs (fC). The termination impedance was 400 ohms, and the recording bandwidth (which determines the noise floor) was 100 MHz.

We have also evaluated the performance of this system by replacing the HEP detector with a voltage pulser and using a long-electrode modulator[7] which was terminated in a 50 ohm load. We also upgraded the receiver to one with a 220 MHz bandwidth. Typical results appear in fig. 5. Here we see the output of the optical receiver when the modulator is driven with a 1.9 mV-peak signal. The peak receiver output is 150 mV. We find the signal-to-noise ratio (snr) to be 8.5 at this recording bandwidth of 220 MHz. Thus the lowest signal that we could record at the modulator would be 0.22 mV. The shot-noise limited noise floor that we calculate is 0.203 mV (at the modulator) for this optical power of 5.5 mW and modulator V_π of 2.68 volts. *Therefore, we have demonstrated a shot-noise limited 220 MHz optical data link with 0.22 mV sensitivity.*

Conclusions / Future Work

We have presented results from two state-of-the-art optical data links. These systems have both been "field-tested" and fulfill some unique measurement roles. In the future we will be exploring new modulator designs and materials, new detection schemes, and new optical

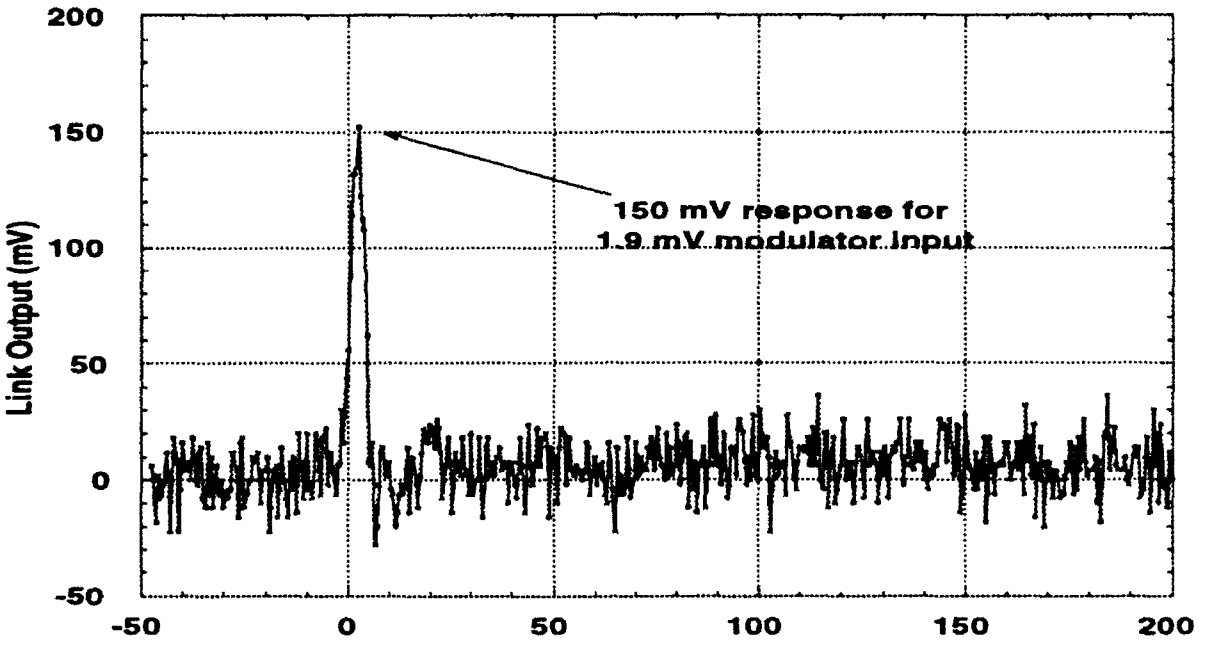


Figure 5. Shot-noise limited response of a 220 MHz SSC link to a 1.9 mV voltage pulse.

sources that we hope will enable us to further push the limits of system bandwidth, sensitivity, and dynamic range.

We further hope to apply this capability to digital applications ranging from computer interconnects to networks, and other analog applications such as antenna remoting.

Acknowledgments

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[3] This can vary depending on the particular laser geometry and power control features. The Amoco laser noise peaks around 150 kHz while the Lightwave laser noise peaks around 500 kHz.

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[6] We note that in some previous conferences we had incorrectly put this measured noise floor at less than one fC. This incorrect value was due to an erroneous calibration measurement. The authors regret the error.

[7] This modulator was a commercial unit from United Technologies Photonics.

ThC1

LINEARIZATION TECHNIQUES FOR WIDEBAND ANALOG TRANSMITTERS

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Transmitter linearity is an important consideration in the design of wideband transmitters for analog lightwave transmission systems. System requirements for applications such as analog microwave systems and multichannel amplitude-modulated (AM) vestigial-sideband (VSB) CATV systems generally impose limitations on allowable nonlinearities in the transmitter. This paper presents an overview of techniques for improving the linearlity performance of directly modulated lasers and external modulators.

In directly modulated semiconductor laser transmitters, the primary source of distortion is the intrinsic nonlinearities of the semiconductor laser. These nonlinearities arise from the carrier-photon dynamics in the active region [1] and nonlinear leakage current effects [2]. Laser nonlinearities can be minimised by careful design of the device to maximise the relaxation oscillation resonance frequency [2], minimize leakage currents [2,3], and optimize other parameters such as the coupling between the grating in the active region in DFB lasers [3].

In externally modulated transmitters, distortion components arise from the intrinsic nonlinear attenuation versus drive voltage transfer characteristic of the modulator [4]. Little can be done to alter the transfer characteristic of a single modulator device, but composite device structures based on polarization effects and/or cascaded devices [5-7] show some promise for improved performance. External modulators can be biased to produce second order distortion that is lower than in directly modulated semiconductor lasers. Third-order distortion in modulators may be larger than in semiconductor lasers, depending on the modulation frequency [8].

In applications requiring high linearity, a variety of techniques can be used to reduce transmitter distortion to values below that produced by an intrinsic laser or external modulator. These techniques can generally be classified into four main categories: (a) predistortion techniques [2,10,11], (b) optoelectronic feedback [12,13], (c) techniques using cascaded and parallel composite devices, and quasi-feedforward methods [5-7,9,14], and (d) feedforward techniques [15-17]. Most of these techniques apply to either directly modulated lasers or external modulators, but hybrid approaches using both directly modulated lasers and external modulators in the same transmitter are possible [8].

Predistortion compensation is the simplest and perhaps most straightforward of the various linearization techniques. It is useful only when the laser or external modulator is memoryless, i.e. when the device has an input-output transfer characteristic that is independent of time. This is a reasonable approximation for practical semiconductor lasers and modulators at frequencies below a few hundred MHz but is invalid in semiconductor lasers operating above this frequency. The high-frequency performance of predistortion circuits can become difficult to predict at frequencies above a few hundred MHz due to parasitic capacitances and inductances associated with the junction diodes in the nonlinear elements used in these circuits. Nevertheless, predistortion compensation has been shown to be very effective in some applications.

Optoelectronic feedback [12,13] can reduce distortion in the same way that electronic feedback can reduce distortion in electronic amplifiers. The main limitation of this approach is that the time delay associated with the feedback loop ultimately limits the stability of the circuit and determines the maximum frequency of operation. With hybrid circuit construction this maximum frequency would generally be in the order of a few hundred MHz. Future progress on monolithic integration of this type of circuit may lead to feedback circuits that can operate well into the GHz region.

Quasi-feedforward compensation or static feedforward compensation [9,14] operates on the principle that distortion produced by one nonlinear device (i.e. a semiconductor laser or external modulator) can be compensated by cancelling that distortion with an opposite distortion component produced by another identical [14] or known [9] device. The devices generally operate in parallel, and the cancellation occurs in the optical domain at the point where the outputs from the two devices is combined. If the devices are nominally identical then this technique may be effective even if they exhibit memory effects and have a time-dependent transfer characteristic. The technique can be extended to included non-identical devices [9] and with this approach a variety of design compromises can be effected. It should be noted, however, that with non-identical devices quasi-feedforward compensation will generally not be effective if the lasers or external modulators show memory effects. The linearization of modulators based on cascaded devices [6,7] is closely related to quasi-feedforward compensation.

Like quasi-feedforward, full feedforward compensation [15,17] requires two devices (lasers or modulators). However, feedforward compensation allows distortion to be reduced in devices with or without memory. An advantage of full feedforward compensation is that the two devices do not need to be identical and the distortion characteristics of the devices do not need to be known. Full feedforward compensation methods will generally be effective even if the distortion characteristics of the device to be linearized are functions of external parameters such as temperature or external reflections. Feedforward compensation circuits may be too complicated for some applications, but have the advantage that, like feedback circuits, they can also be used to reduce laser noise [17].

The choice of an optimum linearization technique for a particular directly modulated or externally modulated transmitter will depend upon a number of factors including frequency range, the distortion performance required, and the acceptable complexity of the linearization circuitry.

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ThC2 CIRCUIT MODEL FOR HARMONIC DISTORTION CHARACTERIZATION IN DISTRIBUTED FEEDBACK LASER DIODES

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It is well known that the spatial hole burning (SHB) and the leakage current (LC) effects are responsible for intensity modulation harmonic distortion in DFB laser diodes at lower modulation frequencies (10MHz-1GHz) [1,2] . Because this frequency range is of interest to analog AM-CATV applications where DFB laser diodes play a major role as optical transmitters,it is important to be able to datermine the SHB and LC contributions to the overall harmonic distortion characteristics of device [3,4].

In this paper we propose an equivalent circuit model approach for harmonic distortion characterization in DFB lasers. The proposed model which is shown in Fig.1 takes into account both SHB and LC nonlinearities of the device. The active region of the device is represented in Fig.1 by the branch consisting of diodes D_1 and D_2 and the resistor R_1. The LC branch has the diode D_2 in series with the resistor R_2. The resistor R_3 in the third branch is intended to model SHB which is induced by a nonuniform longitudinal carrier distribution. In our previous work [4] the R_3 resistor has been assumed to be linear, thus allowing for the LC modeling only. Reasonable agreement between the calculated and measured second harmonic distortion over a limited range of bias currents has been obtained . The model components shown in Fig.1 are related to easily measurable quantities such as L-I, dL/dI , and its derivative characteristics. Also, the device dc optical spectra below and above the threshold current are required to establish the κL and optical powers at both facets of the device. An example of the relationship between the differential efficiency and the model elements is shown in Fig.2. The resistors R_α and R_β shown in Fig.2 are related to R_1,R_2, and R_3 resistors as follows $R_\alpha=R_1R_2/(R_1+R_2)$, and $R_\beta=R_2+R_\alpha$.

The analysis underlying the proposed circuit model is based on the well known current-voltage relationship for a p-n junction and the

single-mode rate equations to derive the leakage current and the SHB compression factor from a simple computer program.

The model has been verified using several commercial InGaAsP DFB devices for the second harmonic distortion to carrier (2HD/C) characteristics. Reasonable agreement between the modeled and measured characteristics has been obtained. Because of its relative simplicity and easy determination of its elements, the proposed model is in our opinion,well suited for optoelectronic CAD applications.

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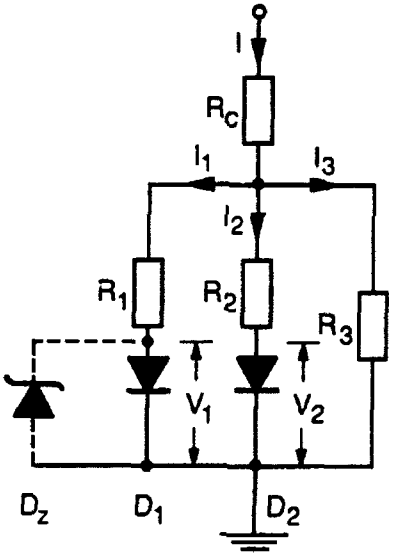


Fig.1

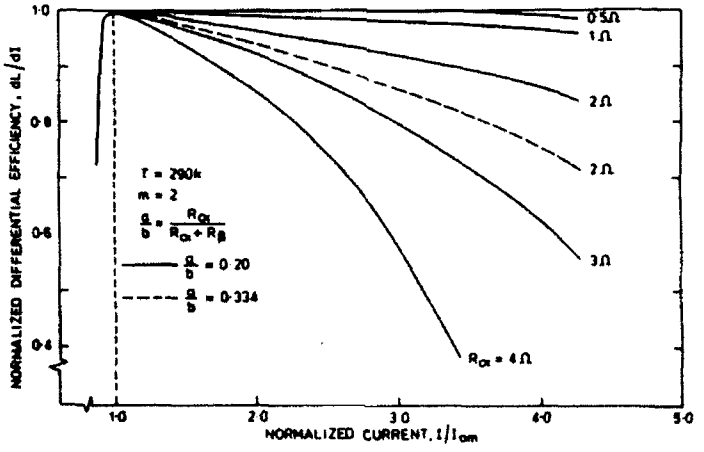


Fig.2

ThC3

HIGH-CONTRAST SELF-LINEARIZED OPTICAL MODULATION OF A SEED BASED ON A NORMALLY-ON ASYMMETRIC FABRY-PEROT MODULATOR WITH RECORD COMBINED CHARACTERISTICS

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Recently, asymmetric Fabry-Perot (ASFP) structure with a pair of unequal grating mirrors to enhance the electroabsorption of light within the active medium, consisting of III-V semiconductor quantum wells (QWs) and/or superlattices (SLs) has attracted attention for potential applications such as two-dimensional arrays for optical interconnection of integrated circuits and optical processing. In particular, normally-on operation achieved by modulation of the cavity absorption to balance the initially impedance-unmatched resonator, through the quantum-confined Stark effect (QCSE) in QWs, has been demonstrated to exhibit simultaneously very low insertion loss, high contrast and low drive voltage[1]. This can be attributed to the relatively large field-induced absorption coefficient (α_{high}) and absorption coefficient ratio f (= $\alpha_{high}/\alpha_{low}$, where α_{low} is the residual loss) at photon energies below the low-field (or zero field) QW excitonic absorption edge.

Recently, using appropriate positive optoelectronic feedback, self-electro-optic effect device (SEED) based on high-contrast normally-off ASFP, operated as a modulator and detector simultaneously, has been demonstrated to exhibit optical bistability with very high on/off ratio[2]. For various potential application in optical information processing, it is desirable for a surface normal optical modulator to exhibit both high contrast ratio, for maximizing the device's fan-in, and low insertion loss, for maximizing its fan-out. Moreover, this should be achieved at low voltage swing for lower electrical switching energy. In addition, in analog signal-processing applications, it is advantageous that the optical output depends linearly on the control input, be it electrical or optical. It is well known that the modulated optical output with respect to drive voltage of neither a simple QW non-Fabry-Perot modulator nor an ASFP is linear. To improve the linearity of the optical output signal of the modulator and the input control signal, in this work, we operate a QW-ASFP with simultaneously very low insertion loss, high contrast and low drive voltage as a SEED, where current biasing of the ASFP is used[3]. The optical modulation of the ASFP is expected to vary linearly with drive current and exhibit similar high performance with low switching energy.

The ASFP device structure contains top and bottom quarter-wave stacks respectively of 5 periods p-doped and 20.5 periods n-doped alternating 725Å AlAs and 625Å $Al_{0.2}Ga_{0.8}As$ layers. The active region inside the Fabry-Perot (FP) cavity is composed of 25.5 pairs 100Å GaAs QWs confined by 45Å AlAs-GaAs short-period SLs[1]. In contrast to that of the optically bistable SEED, the internal optoelectronic feedback in this present case is negative[3] because the operating photon energy is at the FP mode of the normally-on ASFP where the photocurrent increases with increasing reverse-bias voltage, due to increasing absorption caused by the red-shift of the QW exciton[4]. As shown in Fig. 1, a voltage-control current source is connected to the ASFP in reverse bias. When the current I_c from the current source is larger (smaller) than the photocurrent I_{ph} generated by the ASFP, then it will charge up (discharge) due to the current difference. This in turn adjusts the voltage across the ASFP to yield increased (decreased) absorption and hence increases (decreases) I_{ph} until the stable equilibrium point $I_c = I_{ph}$ is reached. At this point, if

the internal quantum efficiency of the ASFP is unity, then the absorbed optical power P_A is given by $h\nu I_c/q$, where hv is the photon energy and q is the electronic charge. Since P_A is linearly dependent on the control current I_c, the reflected power P_r given by $P_r \approx P_i - P_A$ (very good approximation because the transmitted power of such ASFP is very small compared with P_i and P_A) is therefore a linearly decreasing function of I_c. Further, P_A can be expressed as AP_i where A is the fraction of light absorbed in the active cavity and is a function of the active medium absorption coefficient and the FP cavity parameters. At the FP resonance, A is virtually complementary to the FP reflectivity, and this can lead to the virtual extinction of the reflected power of the balanced ASFP with sufficient drive current.

Shown in Fig. 2 are the output powers versus drive current curves for two different optical input powers at the FP wavelength (~866nm). Except in the low current region close to $I_c \approx 0\mu A$ where the reflected power is limited by the ASFP's insertion loss (<1.6dB), the ASFP's reflected power decreases linearly with increasing current to a minimum given by its 'zero' reflectivity, yielding contrast ratio of >100:1 at the output. In the linear region, the rate of change of P_r with respect to that of I_c is given by the fundamental parameters hv/q, as evidenced by the slopes of the curves in Fig. 2.

The speed of the current device operation is dependent on the speed of charging and discharging the ASFP P-I(QW)-N diode by the I_c and I_{ph} difference. The current demonstrated SEED can also be in other configurations where the ASFP is integrated with electronic components to extend the device versatility and increase potential applications. In this paper, additional results will be presented. Finally, possible scheme of monolithic integration of such ASFPs with photonic and electronic devices will be discussed.

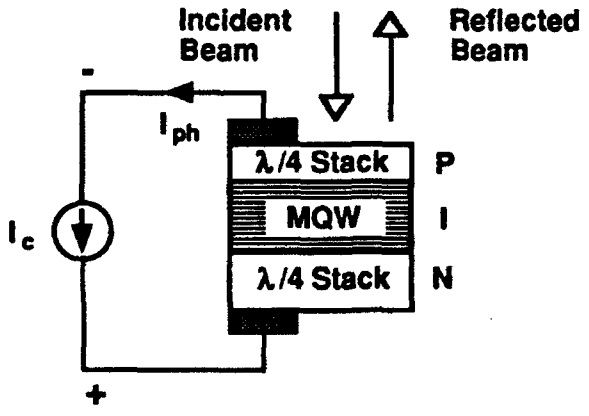


Fig. 1. Schematic diagram of the SEED consisting of a current source connected to reverse bias the normally-on ASFP.

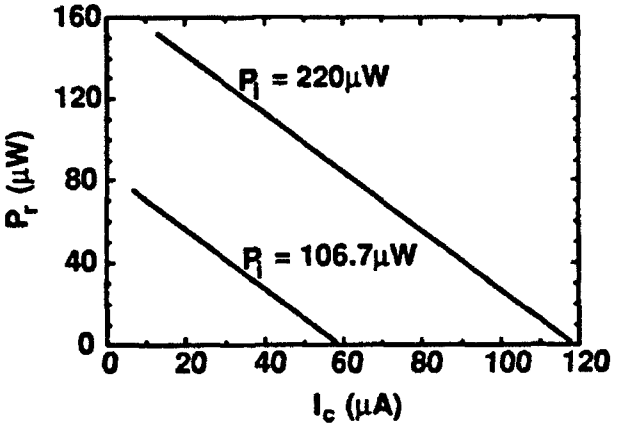


Fig. 2. Reflected output power as a function of the drive current at the FP wavelength for two different input optical powers.

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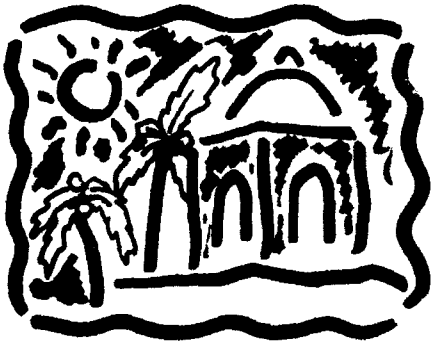
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Optical Multiple Access Networks

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MA1

NETWORK ISSUES IN THE BROADBAND ERA

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The bandwidth for data communications has been growing steadily and dramatically over the last twenty years. Some of us remember the early days of data modems at 10 characters per second (cps) in the late 1960's. When 300 baud speeds became available (providing 30 cps), we thought of it as a major improvement (and it was).

In the mid-70's, as packet-switched networks began to proliferate, we saw the standard set at 64 kilobit per second (KBPS) trunk speeds; of course, by the time one paid for the software and protocol overhead, we were happy to end up with about 10 KBPS file transfer speeds (by now, the dial-up data modem speeds had reached 2400 bits per second). The killer application which drove the penetration of these X.25 networks was that of transaction processing.

In the 1980's we witnessed the proliferation of T1 channel speeds, providing 1.533 megabit per second (MBPS) access. Private T1 networks exploded in the 1980's because of the cost savings they provided by allowing corporations to integrate their voice and data networks into a single network. This was the killer application for T1 networks. However, the packet-switched networks still had 64 KBPS backbone speeds due largely to the complex operations the switches were required to carry out; specifically, each switch had to decode every packet up to the third layer (the network layer) of the seven layer OSI architecture.

As we entered the 1990's, we saw a grass roots development in the form of Frame Relay networks. These nets offer packet switching at T1 speeds, a significant step above the 64 KBPS packet switching nets of the 1980's. Both hardware and software developments led to these higher speed packet switched networks. On the hardware side, the widespread deployment of fiber optic communication channels by the long-haul carriers was critical. Besides having enormous bandwidths, these fiber optic channels are extremely noise-free, thereby greatly relieving the network of extensive error control. Moreover, much faster switches have been developed due to the progress in VLSI technology. These two hardware advances reversed the relative cost of switching versus transmission and has led us to architectures in which the economic as well as the performance bottleneck is now the switch. New protocols which take advantage of these hardware improvements have also been developed. In particular, the ISDN signalling channel (the D channel) uses a streamlined protocol for routing signalling packets (known as the Link Access Protocol for the D channel - LAPD); indeed, it only decodes these packets up to the second layer (the data link layer) of the seven layer

model, extracting a minimal amount of network layer information. Frame Relay uses the LAPD protocol for the data channel, thereby achieving much higher transfer speeds. Thus, by relegating as much function to hardware as possible, by moving function out of the network when possible (e.g., error control on the data packets), and by taking advantage of streamlined packet protocols, Frame Relay is able to achieve packet switching at T1 speeds. The killer application which has been the driving force behind Frame Relay is that of local area network (LAN) interconnection.

In addition, we have seen some multi-megabit data network plans, announcements and offerings. Among these are the Fiber Distributed Data Interface (FDDI) at 100 MBPS, Switched Multimegabit Data Services (SMDS) at 45 MBPS, the Distributed Queue Dual Bus access protocol at 45 and 150 MBPS, ATM switches and Broadband ISDN at 155 MBPS up to 2.4 gigabits per second (GBPS), the High Performance Parallel Interface (HIPPI) at 800 MBPS, etc. Indeed, the Synchronous Optical Network (SONET) standard has defined speeds for optical systems well into the multigigabit range.

It is clear we are moving headlong into an era of gigabit per second speeds and networks. The High Performance Act of 1991 legislates a major national effort in high performance computer and communications, one component of which is the National Research and Education Network (NREN). In support of the NREN, a number of gigabit testbeds have been established and experiments with gigabit networking are already underway.

As we move into the gigabit world, we must ask ourselves if gigabits represent just another step in an evolutionary process of greater bandwidth systems, or, if gigabits are really different? In the opinion of this author, gigabits are indeed different, and the reason for this difference has to do with the latency due to the speed of light.

In this presentation, we will comment on the fact that gigabit networks have forced us to deal with propagation delay due to the finite speed of light. Fifteen milliseconds to cross the United States is an eternity when we are talking about gigabit links and microsecond transmission times. The propagation delay across the USA is forty times smaller than the time required to transmit a one megabit file into a T1 link. At a gigabit, the situation is completely reversed, and now the propagation delay is roughly 20 times larger than the time to transmit into the link. We have moved into a new domain in which the considerations are completely reversed. We must rethink the way we design control algorithms, the way we architect our networks and the way we design our applications in this new environment. Much more research must be done before we can claim to have solved many of the problems that this new environment has exposed. We must solve these problems in the near future if we are to enjoy the benefits that fiber optics has given us in the form of enormous bandwidths.

MA2 OPTICAL FDM NETWORKS AND COMPONENTS

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It is often said that the transmission window of optical fiber provides a bandwidth of tens of teraherz (10^{12} Hz). Such a band would allow network throughputs of tens of terabit/sec, but many physical factors other than transmission loss limit network capacity. Still, throughputs approaching a Tb/s may well be physically realizable.

Just who needs this capacity and at what cost are questions well beyond my ken. And it is probably too early to ask. But the appetites of man and machine to exchange growing volumes of information (vital and trivial) seem insatiable.

Two straightforward approaches to utilizing the available band are optical time-division multiplexing (OTDM) and optical frequency-division multiplexing (OFDM). The former requires that pulse widths of less than a picosecond (10^{-12} s) from different laser sources be synchronized and time-multiplexed over wide separations. Transmission delay dispersion and limitations of high-speed electronics make the OTDM approach difficult.

Optical FDM is simpler since N optical carriers each modulated at bit-rate B and spaced by Δf can cover the available bandwidth. The bandwidth utilization b^{-1}, where

$$b = \Delta f / B \,, \tag{1}$$

is determined by crosstalk requirements and as a practical matter might be b = 10, i.e., a 10% utilization. The throughput is given by

$$T = NB \,. \tag{2}$$

The bit-rate B is limited by the cost and complexity of electronic and optoelectronic (e.g. lasers, modulators, detectors) devices. The number channels N is limited by the tuning ranges and tuning speeds of lasers and optical filters. Nonlinear optical effects in long transmission fiber spans also limit T when the product of network distances and total signal powers exceed a megameter-mW or a few Mm-mW-nm, where the total OFDM spectrum width is in nanometers [1].

For a simple passive optical star network [2], as shown in Fig. 1, the laser transmitter powers are reduced by N at the receivers. The direct detection receiver sensitivity is proportional to B and is typically $S = pB$ with $p \sim 10^{-3}$ mW/Gb/s. Then, with a transmitter power of $P \sim 1$ mW, the received power just equals the sensitivity (i.e. no margin for excess loss) when

$$\frac{P}{N} = p\,B \tag{3}$$

or $T = NB = P/p \sim 1$ Tb/s. Optical preamplifiers can improve p and T by a factor of 10 or more.

Some network users cherish the dream of an "all-optical network" (AON), whereby clear optical channels can be provided and controlled without resorting to electronic buffering, regeneration, switching and multiplexing at intermediate nodes. Thus, as the Interstate highway system and local roads allow a wide variety of vehicles to access every corner of the

US, so the AON would allow photons in a wide variety of signal formats to find their way through clear channels for local and wide area access. There are plenty of reasons why such a goal is unrealistic, even if you water down the definition of "all-optical", but it is a challenge to see how far we can get.

Optical frequency routing provides a promising approach. We can make use of a component with N fiber inputs and N outputs that routes signals according to their optical frequencies. See Fig. 2. Such a function can be realized in a clumsy way with bulk components and in an elegant way with an integrated optics version [3]. Semiconductor lasers that can hop among tens of optical frequencies separated by tens of GHz in a few nanoseconds can provide fast switching for connection-oriented or connectionless packet services [4]. Tunable filters and receivers, with limited speed, are also available, and elegant versions of other devices such as frequency translators and frequency-division switches remain to be invented. The network architecture design is strongly influenced by available component functionality and device research is strongly influenced by the needs uncovered by novel network design.

The design of a high speed OFDM network covering both local and wide areas and offering connection-oriented and connectionless services is a big job, requiring the interaction and mutual understanding of engineers with experience in many disciplines. Perhaps the toughest hurdle is the control system, incorporating the scheduling of scarce resources and the avoidance of congestion over propagation times that far exceed packet times.

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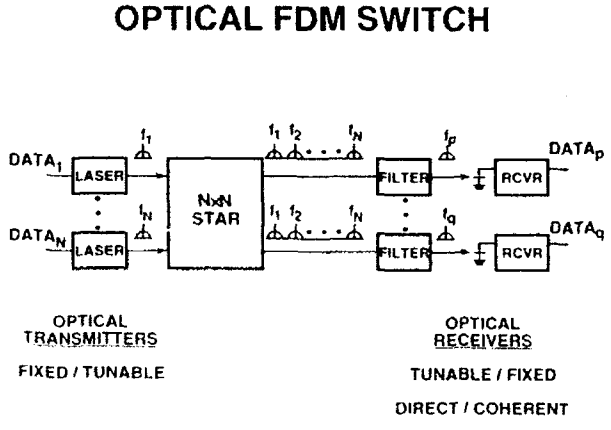


FIGURE 1

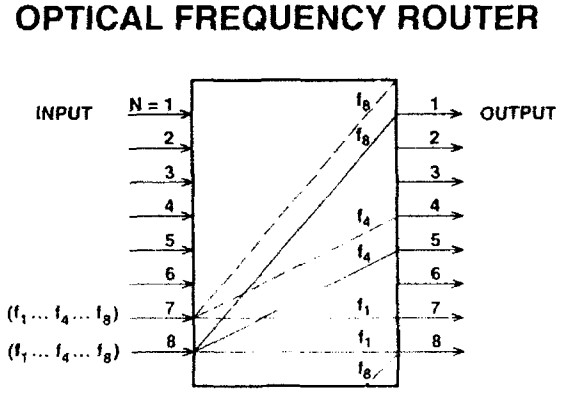


FIGURE 2

MB1 HYBRID WDM/SPACE DIVISION OPTICAL NETWORKS

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1.Introduction: Optical or Photonic technologies now offer one of the most important means of constructing broadband communication networks. Optical fiber transmission systems have already been installed world-wide as part of a broadband communication infrastructure. Photonic switching is expected to play an important role in "optical one-link" transparent networks over optical fiber transmission highways. Among the various types of photonic switching networks, photonic Space-Division (SD) and Wavelength-Division (WD) networks are attractive because of their ability to construct bit-rate independent flexible networks. One of the most important issues in driving photonic switching networks into practical use would be to find suitable applications. This paper first describes some possible applications of photonic switching in broadband networks and the recent activities of photonic switching network developments are also reviewed.

2.Broadband Network and Photonic Switching: Figure 1 shows a possible application of photonic switching in a broadband network, which includes both public subscriber and private networks. The subscriber network which consists of two layers: the transfer network and the access network[1], transmits and distributes user-signals to a particular service node, depending upon the service requirements. Signals from a service node are connected to trunk lines via a Digital Cross-connect System (DCS). In the case of private networks, a broadcasting studio[2] seems to be the most attractive near term application of photonic switching, where a demand exists for distribution and transmission of several hundreds of standard digital video signals and a switcher for at least a few tens of channels of High Definition TV (HDTV).

A broadband PBX, DCS and HDTV switcher represent good targets for implementing photonic SD switching technologies, whereas in the case of applying distributed photonic WD switching technologies, a broadband LAN or MAN and the transfer network would be more appropriate. Such distributed switching networks are practical with current technologies because they can be constructed without large scale Photonic Integrated Circuits (PICs). With the necessary PIC requirements, photonic WD switching networks have the potential for realizing large scale switching systems which can be applied to a public network service node.

3.Present Status of Photonic Switching

(1)Photonic SD switching system: A 32 line photonic SD switching system, using polarization independent $LiNbO_3$ 8x8 switch matrices has already been demonstrated[3]. However, for practical application, capacity expansion to over 100 lines would be required. Introducing optical amplifiers, especially semiconductor traveling wave optical amplifiers (TWAs), to the switching network is both effective and promising for this purpose[4]. The possibility of a 128-line photonic SD switching network has already been demonstrated[5] and novel packaging technologies for such a network have also been developed[6]. Photonic SD switching networks are also very attractive for applying to network restoration. Fig. 2 shows the structure and operation of such a restoration scheme, namely, optical DCS[7]. If all of the fibers between a pair of nodes are cut either accidentally or by a natural disaster, optical signals are re-routed to the destination node via standby optical fibers and the photonic switching networks of passing nodes, without any O-E or E-O conversion. Design considerations have shown that optical DCSs for a MAN application can be constructed using $LiNbO_3$ 8x8 switch matrices and TWAs.

(2)Photonic WD switching network: The wavelength switch (λ switch), which accomplishes wavelength interchange, is the key component in photonic WD switching networks[8]. The λ switch is composed of tunable wavelength filters and wavelength converters. An eight channel photonic WD switching system has been reported using distributed feedback (DFB) LDs as tunable wavelength filters[8]. Introduction of coherent optical detection technology has been proposed for achieving large scale photonic WD switching networks. The switching function of the coherent λ switch and its capability for a broadband MAN application with a line capacity of over 1000 has already been demonstrated[9]. Another important photonic WD switching network is the WDM

passive star network[10]. This network can be realized by simply using tunable wavelength lasers and filters. An extension to this type of technology has led to using WD/TD hybrid multiplexing[11], where more than a few hundred digital video signals can be broadcasted, even with a limited number of WD channels. Such a network which is suitable for a broadcasting studio application can be seen in Fig.3. Using Acousto-Optic (AO) filters as tunable wavelength filters, distribution/selection of 48 NTSC digital video signals has been demonstrated[12].

4. CONCLUSION: Present technologies readily allow the photonic SD and WD switching networks to be applied to certain areas in broadband networks, such as a broadcasting studio and network restoration. Application expansion requires larger scale photonic switching networks, where PIC development would be a key issue.

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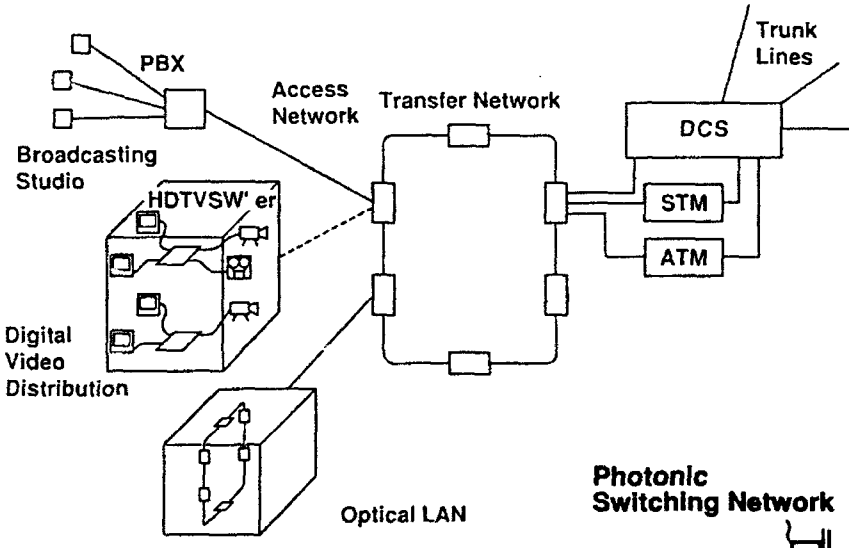


Figure 1
Possible application of photonic switching in a broadband network

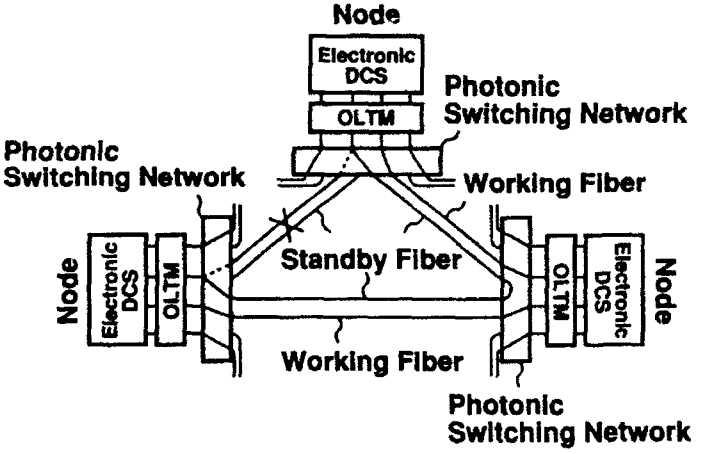


Figure 2
Optical Digital Crossconnect System (optical DCS)

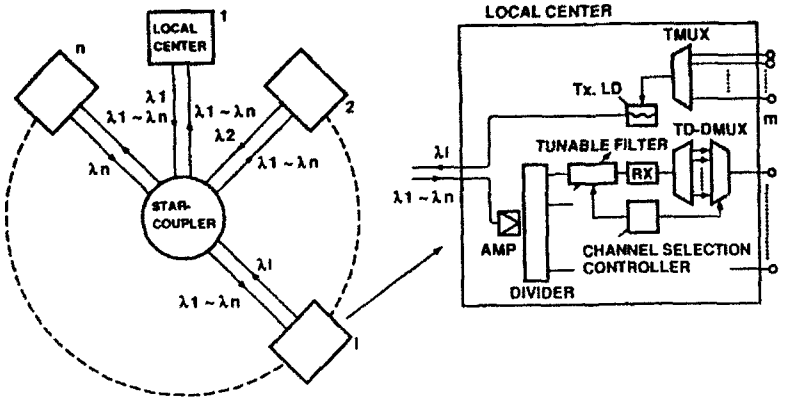


Figure 3
WD/TD passive star network for a broadcasting studio application

MB2

A NOVEL INTEGRATED-OPTIC WDM CROSS-CONNECT FOR WAVELENGTH ROUTING NETWORKS

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Introduction

Wavelength division multiplexing cross-connects play an important role in wavelength routing networks such as passive photonic loops, interoffice networks, and multihop networks [1]. Features of grating technology have been considered for many years.

Recently, we have analysed a general space-varying refractive index medium and studied some of its applications for broadcast and selective-broadcast coupling [2-3], for self routing wavelength division and for a WDM cross-connected star topology in multihop lightwave networks [4]. In this paper, using Bragg micrograting, we design a two-dimensional array capable of performing various wavelength routing functions on a single substrate.

With a deflection-type grating, wavelength selectivity is easily obtainable. Our conclusion is that we can achieve bandwidth of about $0.5A^o$ around the tuned wavelength. A wavelength separation in the order of $10A^o$ can be obtained with very little crosstalk. In other words, if we tune a Bragg cell to wavelength λ_1, by properly choosing the grating period Λ, wavelength λ_i from the coming input wave will be deflected by an angle 90^o and all other wavelengths, $\lambda_j \neq \lambda_i$ (out of its $0.5A^o$ bandwidth) will remain on their original direction. Suppose there are N wavelengths with about $10A^o$ separation and a bandwidth around $0.5A^o$. Suppose we have an input in the Z (or X) direction with N wavelengths $\lambda_1, \lambda_2, ...\lambda_N$ arriving at the single Bragg cell tuned to λ_i. Only λ_i will be deflected by 90^o and will get out in the X (or Z) direction and all other wavelengths, λ_j; j≠i will propagate out in the original Z (or X) direction. The crosstalk can be as low as -60 to -70 dB. In this paper, we assume about 1nm wavelength separation between and $0.5A^o$ bandwidth around the wavelengths. The simple single Bragg-cell can be implemented by two-wave mixing. This tuned Bragg cell can be used as a 2×2 wavelength-selective coupler with a fixed crossover wavelength. Suppose there are two inputs, one applied in the Z-direction with wavelengths λ_1^1 and λ_2^1 and the other in the X-direction with wavelengths λ_1^2 and λ_2^2, when; $\lambda_1^1 = \lambda_1^2 = \lambda_1$ and $\lambda_2^1 = \lambda_2^2 = \lambda_2$. Only $\lambda_1 = \lambda_1^1 = \lambda_1^2$ will be deflected by 90^o and $\lambda_2 = \lambda_2^1 = \lambda_2^2$ will go through in its own direction, because the Bragg-cell is tuned to λ_1. A single-tuned Bragg-cell can be considered as a 2×2 wavelength-selective coupler.

We use this simple Bragg-cell in an integrated optic form and use it for network applications discussed in the following section. Furthermore, we assume that a single-tuned Bragg-cell has the wavelength selectivity over the entire necessary bandwidth for dense WDM.

II. A Two-Dimensional Array Based on Single Bragg-Cells for Various Wavelength Routing Applications

By a proper wavelength assignment and employing enough number of single Bragg-cells with each cell tuned to a desired wavelength, a two dimensional array can be set in a matrix form which may be implemented by integrated optic. This device provides access to the vast bandwidth of single-mode fiber by enabling wavelength routing and switching in the network. We will show how such a desired network can be constructed by our proposed matrix form of integrated optic, where each element of the matrix is properly chosen to be one specific Bragg-diffraction cell. We will describe our proposed system by an example.

Example: One important application of wavelength routing is nearly fixed assignment cross-connect application, where circuit connections and capacity vary slowly and do not require active switches. The general structure for such a cross-connect is shown in [1]. The N-nodes of a cross-connect is shown in a two-sided model with the transmit side on the left and the receive side on the right. As shown in [1], each transmitted signal has unique wavelengths which correspond to the destination addresses. All the optical signals are wavelength-multiplexed and are transmitted over a single-mode fiber to the network hub. At the hub, wavelength demultiplexers separate the signals from each incoming fiber. All the channels that are intended for a given destination are then passively rearranged, and since they were allocated different wavelengths, they can be wavelength-multiplexed and sent towards the destination on a single fiber. At the receiver of each node these different channels are wavelength-demultiplexed.

We claim such a network hub can be implemented by integrated optic as shown in Fig. 1. There are $N \times N$ single Bragg-cells. The cell in the i-th row and the j-th column called (i,j) is tuned to wavelength, λ_{ij}; it means that only λ_{ij} (with a bandwidth around $0.5A^o$) will be deflected by 90^o and all other waves will go through straight. Therefore, we have N inputs each with a set of wavelengths, $\lambda_{i1}, \lambda_{i2}, \ldots, \lambda_{iN}$; $i = 1, \ldots, N$, entering the system, but only one wavelength from each point will be deflected by its own specified (tuned) Bragg cell and all other

wavelengths will go straight to find their own specified (tuned) cell. The deflected light will travel straight up through the other cells because none of these cells have been tuned to these wavelengths. Therefore, if λ_{ij}'s are independent of each other, (i.e., wavelength separation is in the order of $1nm$ with some bandwidth around $0.5A^{\circ}$) the system shown in Fig. 1 will be operating as a desired optical network hub with N inputs from left to N outputs on the top of the device.

It is observed in [1] that for N nodes, N^2 different wavelengths are required for a network with N^2 point-to-point connections. However, the wavelength allocations for the proposed multiplexing structure requires all wavelengths associated with a given transmitting node (e.g., node q) λ_{qj} and all wavelengths associated with a receiving node (e.g., node m) $\lambda_{j,m}$; $j = 1, \ldots, N$, to be distinct. This condition can be satisfied with only N different wavelengths, consequently, all the WDM multiplexers and demultiplexers in the system are identical. The number of wavelengths can be reduced.

Other applications for this technology that we have considered are $N \times N$ WDM cross-connects with N wavelengths and implementation of a shuffle network, as will be presented orally.

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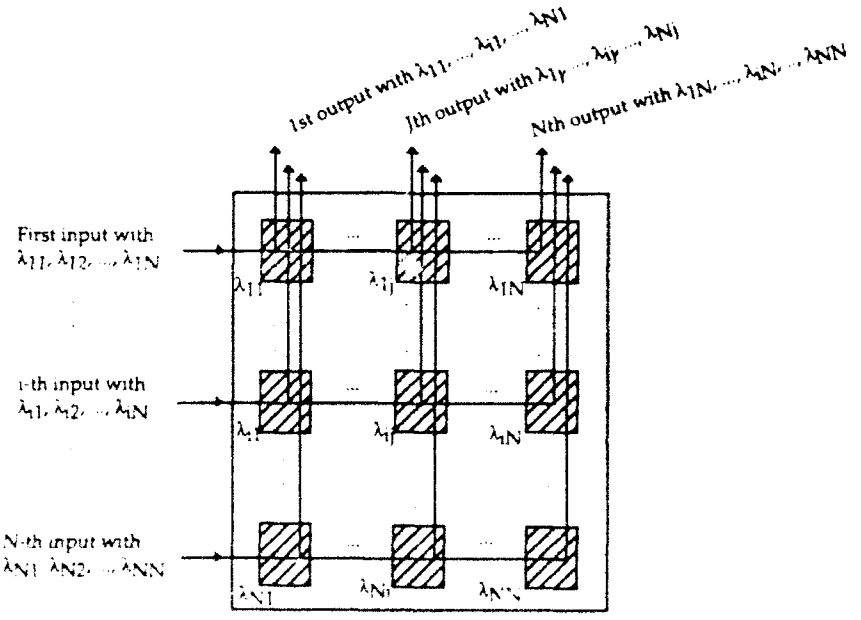


Figure 1 Proposed implementation of $N \times N$ network hub with $N \times N$ single Bragg-diffraction cells. The cell in the i-th row and the j-th column called (i,j) is tuned to λ_{ij}, i.e. only λ_{ij} will be deflected over this cell by θ_B and all other wavelengths will go through straight.

MB3

A PACKET-RATE REAL-TIME RECONFIGURABLE PHOTONIC SWITCH FOR COMPUTER INTERCONNECTS

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Multistage, multihop photonic interconnection networks with deflection routing can allow tightly coupled multiprocessor computers to scale to large number of processors over large physical areas [1]. Deflection routing handles the routing and contention functions and is well matched to flow-through photonic switches. A key component of these networks is the 2x2 photonic switch capable of self-routing packets and resolving contention for its output ports. A 2x2 photonic switch which performs deflection routing in real-time has been demonstrated [2]. The reported switch processes packets that are coded using bit per wavelength coding (BPW). An electronic EPROM lookup table was used to map all 2^6 possible control bits from the two switch inputs to a single control signal. Switch throughput was on the order of 10 Mbit/s and latency on the order of 1 μs.

Two important features are scalability to large numbers of nodes and robustness to changing traffic and network conditions. The routing control processor (RCP) is responsible for computing the switch state, and should scale as the number of nodes increases. Additionally, if network conditions change, e.g. if a link goes down, the RCP should be able to adapt. Real-time reconfigurable switches offer the potential to adapt to changing conditions. optoelectronic based processors can be used to realize real-time reconfigurable architectures with low latency and the added benefit that they scale well with increasing network size.

In this paper we discuss a novel reconfigurable switch architecture and its demonstration with improved performance over the previously reported switch in terms of latency and flexibility. We also discuss the salient features which provides reconfiguration at the packet rate. Details of an optoelectronic processor which allows the control function to be changed dynamically will be discussed. Additionally, a method to extend this technique to react to slowly varying traffic conditions will also be presented.

1.0 Switch Architecture

The overall architecture is shown in Figure 1a. Packets are coded using BPW coding. Control bits centered about $\{\lambda_c\}$ are demultiplexed from data bits centered about $\{\lambda_d\}$. Data bits are stored in a fiber delay line equivalent to the processor latency. The control bits are further demultiplexed and directed to an optoelectronic RCP, where the priority and address bits are sent to separate stages. The RCP generates a control signal for the 2X2 switch. Contention occurs when both inputs request the same switch output port. *Deflection routing* [3] uses the priority bits to determine the switch state. Under a contention condition, the packet with the higher priority bit will route to its desired output while the other input is deflected. The deflected packet will reach its destination via an alternate path in the network topology [1]. In the case where contention exists and the priority bits are equal, the switch is maintained in its prior state to promote fairness.

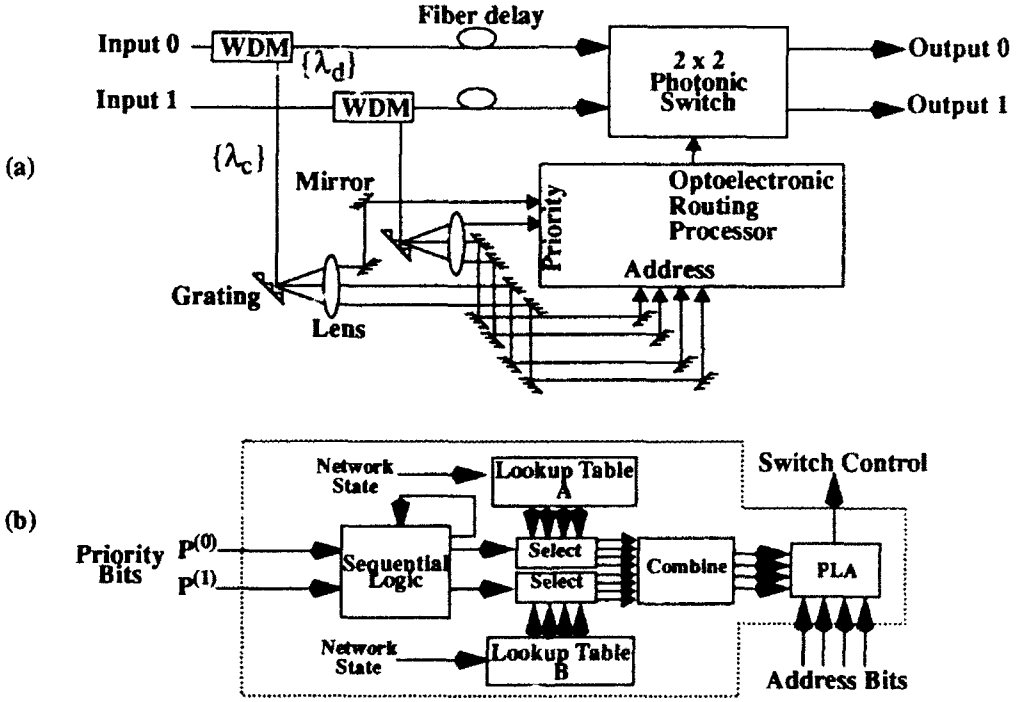
The electrooptic RCP is shown in Figure 1b. It processes the priority bits at a sequential stage in order to choose the routing function via lookup table A or B. The correct mapping is sent to a

GaAs programmable logic array (PLA) which is updatable at the packet rate and has a 2 ns access time. The PLA maps the four address bits to the correct control signal. Network state information can be used to change the lookup tables at a slower rate, providing reconfigurability on two different time scales.

2.0 Summary

We have demonstrated a novel reconfigurable photonic switch architecture which computes routing and contention resolution on the fly according to dynamically programmable lookup tables. Reconfigurability is at the word-size packet rate (> 10 Mpackets/sec) and latency is reduced to a single packet duration using GaAs technology. Details of the optoelectronic processor and resulting performance will be discussed.

FIGURE 1. Architecture of a reconfigurable photonic switch with contention resolution



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MC1

PHOTONIC ATM SWITCHING SYSTEMS

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1. Introduction

The ATM(Asynchronous Transfer Mode)-based Broadband ISDN is expected to be an infrastructure for multimedia telecommunication services in the 21st century. According to our plans, optical fiber will connect all households in Japan by 2015. This means that by then we will need ATM switching systems with a throughput of more than a tera-bit-per-second. Despite the highly-developed state of VLSI technology, the throughput of electronic ATM switching systems is limited by the operation speed of electrical circuits. Electromagnetic induction and a circuit's R-C constant distort the waveform of electrical signals transferred at high rates, and clock skew is another factor limiting the speed of synchronous systems. Photonic circuits, on the other hand, are free of these problems because the waveform of optical signals is not distorted even at transmission rates higher than gigabits per second. It is therefore reasonable to consider that the broad bandwidths attainable in photonic systems can also play an important role in increasing switching throughput in an ATM system. [1]

In this paper, we discuss how to use photonics to surpass the limitations of electronic switching technology. We propose two kinds of system architectures and we present an experimental result on optical address detection.

2. Optical components for ATM cell switching

The essential components needed for building photonic ATM cell switches are high-speed spatial switches with cell buffers, cell coder/decoders, and address detectors. Optical switching devices like $LiNbO_3$ switches and semiconductor switches have a sufficiently broad bandwidth to pass signals at transmission rates of more than terabits per second, but their switching speed is at most several gigabits per second. Fortunately, each ATM cell has a length of 53 bytes and even if it is conveyed at rates higher than 100 Gbps, subnanosecond switching transient time does not seriously reduce the transmission efficiency of the optical path (Fig. 1). Although cell buffers are also indispensable components for resolving cell contention in the ATM switch, the only available devices for the purpose is an optical fiber delay line. The contention problem in photonic ATM systems should therefore be solved by developing ingenious architecture that requires fewer buffers than do conventional ATM switch architectures. To perform such cell header processing functions as address detection and routing by using optical devices is another difficult problem because most optical devices have very limited functions. By using high-speed electronics, however, we can provide header processing functions even when cell transfer rates exceed 10 Gbps. The two-layer structure in a cell switch is useful for combining the high bandwidth of photonic devices and the high versatility of electronic devices.

3. Cell switch architectures

3.1Broadcast-and-Select (B&S) Star Network Using Ultrafast Optical Pulses

A broadcast-and-select (B&S) network using optical star couplers is a simple and useful architecture for some applications like LANs. WDM-based[2] and STM-based[3] B&S networks have been proposed but there has been no proposal for an ATM-based network. The "ULPHA(Ultrafast Photonic ATM)" switch[4] we proposed in 1990 is an n-input and n-output B&S type ATM switch (Fig.2). In the cell coder called a "cascade compressor," each 1-Gbps input cell is converted into a cell with a bit-rate of more than 100 Gbps, and at the same time a wavelength-multiplexed address header is attached to the cell. All address headers of TD-multiplexed cells are examined after WD demultiplexing from the 'body cell.' When the address coincides with the output line address, the ultrafast body cell enters an optical cell buffer and has its speed reduced in a cell decoder. The throughput of the ULPHA switch is limited by the throughput of the TD-multiplexed optical highway and the time required for address header analysis in a cell selector. The latest experimental results on the ULPHA switch are presented in this meeting.

3.2 Hypercube network consisting of optical matrix switches[5]

The hypercube network has a variety of advantages for use in a cell switch. The most significant advantage is

its capability of detour routing. The link contention problem that is almost impossible for photonics to handle can be solved by using detouring in a simple transport layer. As in the ULPHA switch, cell body and routing information are split at the input port and they travel in parallel through an optically switched network and an electronically switched network. Each input/output line is equipped with a few input buffers and output buffers. The throughput of the switch is limited by the size of the optical matrix switches, the operation speed of regeneration circuits, and - when an optical amplifier is used as the simplest regeneration circuit - the maximum number of hops within a switch.

4. All optical cell address detection

When the TD-multiplexed bit rate exceeds 100 Gbps, the address header reaches several Gbps. All-optical address detection beyond 10Gbps is proposed and its operation is examined.[6] The address signal is modulated by phase-shift keying and is detected by using silica-based waveguides and thermo-optic phase shifters. Figure 3 shows the waveform of 4-bit address detection observed when the bit rate was 4.65 Gbps.

5. Conclusion

Two kinds of photonic ATM switch architectures and an all-optical address detection circuit are presented. The combination of photonics' and electronics' technologies will provide practical high-throughput ATM switching systems by the early 21st century.

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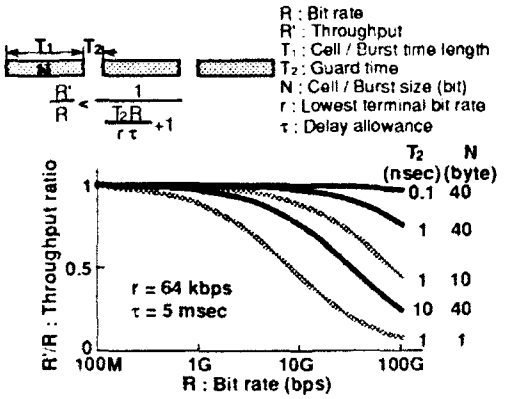


Fig.1 Transmission Efficiency of Optical Spatial Switch

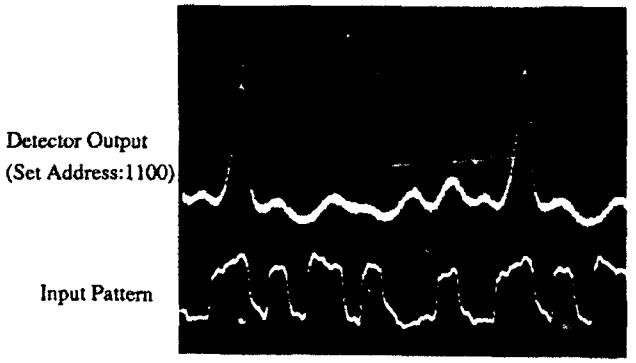


Fig.3 All-Optical Address Detection Experiment

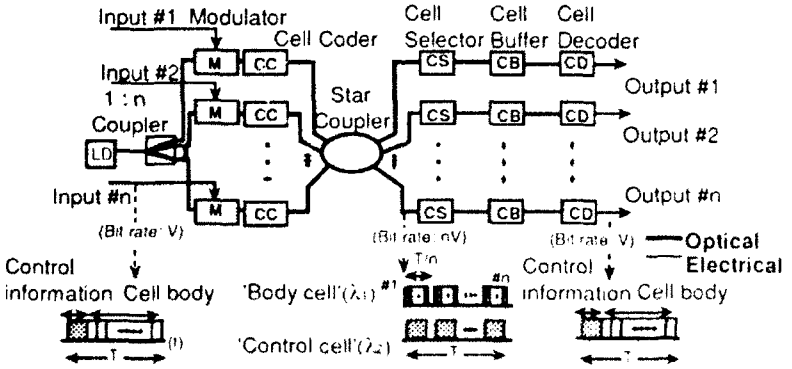


Fig.2 B&S Type Optical ATM Switch (ULPHA)

MC2

DETECTION AND SELF-ROUTING SELECTION OF 25-Gbit/s 4-bit OPTICAL CELLS IN AN ULTRAFAST PHOTONIC ATM SWITCH

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I. Introduction

An ultrafast photonic ATM (ULPHA) switch has been proposed for large capacity and various bit-rate services in future communication networks.[1] The ULPHA switch uses ultrashort optical pulses for cell signals, and can avoid cell contention by using optical output buffers. In this switch, the key technique is the detection of high-speed optical cells. This paper proposes a cell decoder consisting of 1×2 ultrafast switches, delay lines, and 2×1 couplers connected in series. The detection of 25-Gbit/s 4-bit data cells selected by WDM address signals is also presented.

II. Cell decoder configuration

The cell decoder configuration for 2^k-bit optical cells of bit-rate V and the timing chart for 4-bit optical cells are shown in Fig. 1. A time-interval-expander unit consists of a 1×2 switch, a delay line, and a 2×1 coupler. In the kth unit, the 1×2 switch, which is driven by the RF signal of frequency $V/2^k$, sends the pairs of pulses alternately to its dual ports, and then the delay line gives the pairs a relative delay of $2^k \cdot T$. Finally, optical cells of bit-rate V are converted into those of V/(1+VT). This configuration requires fewer optical switches. For example, a 512-bit optical cell requires a decoder with only nine 1×2 optical switches.

III. Experiment

The experimental setup is shown in Fig. 2.

(1) Cell coder 25-Gbit/s 4-bit data cells were generated using 14-ps optical pulses from a gain-switched DFB-LD (1.303μm). The repetition rate was 100 MHz. The "1011" pattern was generated using an optical intensity modulator.[2] The driving signal and the optical output are shown in Fig. 3. The generated data cell ("1011") monitored with a streak camera is shown in Fig. 4. The directly modulated DFB-LD (1.55μm) generated 100-Mbit/s gate signals for the address. The optical data cells and optical gate signals were wavelength multiplexed by a 2×1 coupler.

(2) Cell selector Wavelength-multiplexed data and gate signals were demultiplexed by the optical filter. Cell selection error rate was measured experimentally. At an average received power of -39 dBm, an error rate of 1×10^{-9} was achieved.

(3) Cell decoder The cell decoder for 25-Gbit/s 4-bit cells was fabricated using two 1

× 2 LN switches.[3] The frequencies of the applied driving signal for each switch were 12.5 GHz and 6.25 GHz, respectively. Using two kinds of delay line pairs, 6.25-Gbit/s and 100-Mbit/s signals were generated. Both waveforms are shown in Fig. 5. As can be seen, the 25-Gbit/s cells were successfully decoded to 6.25-Gbit/s and 100-Mbit/s signals with the correct sequence ("1011").

IV. Conclusion

A novel cell decoder to detect optical cells has been proposed. This decoder converts high-speed optical cells back into slow electrical ones with a minimal amount of hardware. The 25-Gbit/s 4-bit data cell selected by WDM gate signals were converted into 6.25-Gbit/s and 100-Mbit/s signals.

Acknowledgments

The authors wish to thank Drs. H. Terui and H. Miyazawa for providing the devices.

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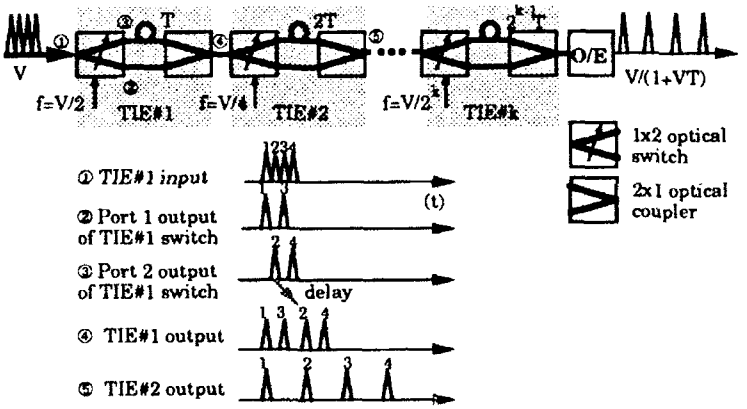


Fig. 1 Configuration of the cell decoder and timing chart to decode high-speed optical cells into slow ones an input of 4-bit optical cells.

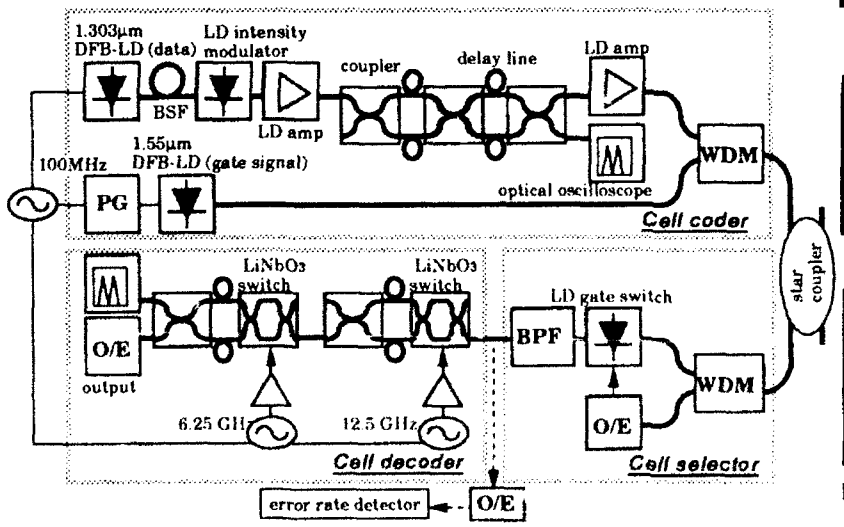


Fig. 2 Experimental configuration for detection and self-routing selection of the ultrafast optical cells. PG: pattern generator, BPF: band pass filter, WDM: wavelength division multiplexing.



Fig. 3 Electrical signal applied to the modulator (upper trace) and modulated optical pulse train (lower trace).

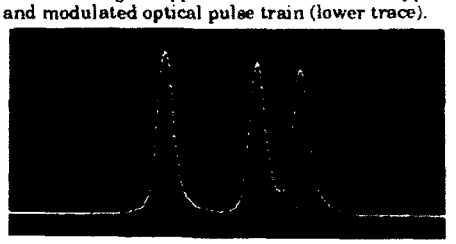


Fig. 4 4-bit ("1011") optical cells.

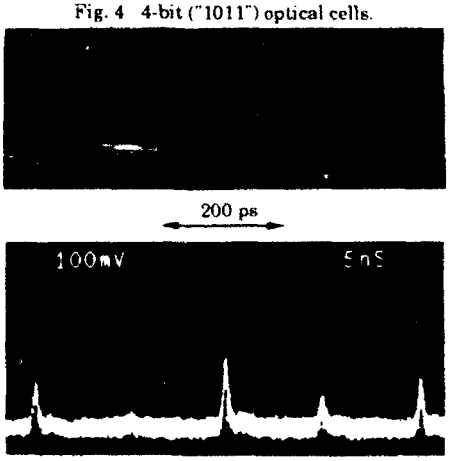


Fig. 5 Waveforms of the 6.25-Gbit/s (upper trace) and 100-Mbit/s (lower trace) 4-bit ("1011") signal at decoder output.

MC3

ON THE DESIGN OF THE 'STAGGERING SWITCH'

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In this paper, we present a novel switch architecture that employs the inherent capability of the optical fiber for storage. The switch is based on two rearrangeably non-blocking stages interconnected by delay lines with different amount of delay. Probability of loss as a function of link utilization and the size of the switch are investigated. In general, with proper setting of the number of delay lines, the switch can achieve arbitrarily low probability of loss. We've estimated that switches of 32 × 32 may easily be implemented with the ECL logic. Additional issues that are discussed are: extension of the *Staggering Switch* to the Wavelength Division Multiplexing technique, growability of the *Staggering Switch* to larger modules, and several implementation issues, such as packet synchronization at the switch inputs.

1 Features of the *Staggering Switch*

Among the salient features of the *Staggering Switch* are: its transparency, lack of recirculation, and flexibility in operation and in performance.

The *Staggering Switch* is an "all-optical" switch and thus is transparent to data bit-rate. Therefore, it may support essentially unlimited link capacity. This feature is achieved in the switch design by the use of the *field-coding* technique in which the header and the data are encoded at different bit-rate. In particular, the header is encoded at considerable lower bit-rate than the bit-rate of the (transparent to the switching operation) data field. Thus the control part of the switch operates at much slower speed, and can be implemented in inexpensive and mature technology, such as ECL, for example. Yet, this low-speed electronics controls Gbps optical switching.

The architectures of the all-optical packet switches proposed in the technical literature are mainly based on some sort of recirculation loops, to facilitate the temporary storage (buffering) of the optical information as to resolve output collisions. This recirculation carries quite a large cost penalty, since some sort of optical amplification (and possibly regeneration) is required to compensate for the optical attenuation and dispersion of optical switching elements in the recirculation loop. Our proposed architecture eliminates the need for optical amplification in the storage elements, since in our switch the optical storage devices are created from pure fiber (without switching elements).

Finally, the scheduling algorithm provides flexibility in the switch operation. In other words, different switching attributes can be created by simple adjustment of the scheduling algorithm, which is implemented in the electronic control. For example, priorities, packet reordering, and different quality of service (i.e., packet loss probability) can be easily incorporated into the switch design through simple changes in the order in which the scheduling is performed. And since changes in electronics are relatively inexpensive (compared to changes in the optical design), our design may accommodate different and differing traffic requirements. Moreover, the level of performance (packet loss) can be easily adjusted in the design process by changing the number of the delay-line elements.

2 Switch Architecture

The Staggering Switch architecture is based on two stages: the scheduling stage and the switching stage. Each one of the stages is a reconfigurably nonblocking switching fabric, implemented with electronically controlled optical devices ($LiNbO_3$, for example). The scheduling stage ($n \times m$) is connected to the switching stage

($m \times n$, where $m \leq n$) by m delay lines, d_i, $i = 1$ to m. The delay of the d_i delay line equals i packets. The energy of each one of the n input lines is split immediately after its arrival; a "small" fraction of the energy is passed to the detector, converted to an electrical signal, and forwarded to the Control. The Control reads the header bits to determine the required routing for the packet, and drives the scheduling and the switching stages of the switch.

The purpose of the scheduling stage is to distribute the packets arriving on the switch input to the delay lines in such a way that, at any time slot, no two packets arriving at the switching stage are destinated to the same output; i.e., the output collisions are resolved by delaying the colliding packets by different number of slots, so that arrivals to the switching module are collision-free. The scheduling algorithm is performed by the Control. Because of the statistical properties of the arrival process, some packets cannot be accommodated without violating the "no collisions at the switching stage" principle, resulting in some probability of packet loss. The switching stage permutes the packets from the delay-lines to the required switch output.

In its basic form, the scheduling algorithm scans the inputs sequentially and for each input packet tries to insert the packet in the lowest possible delay-line, subject to two conditions: the time slot is free and there's no other packet to the same destination in the column that the packet is to be inserted in.

To alleviate the resequencing problem, the scheduling algorithm is modified: if the last packet from input k to output j has arrived s slots ago and was placed on d_i, then a packet from the same input to the same output arriving in the current slot can be placed on d_h, where $min(1, i - s + 1) \leq h \leq m$.

The scheduling and the switching stages may be implemented as rearrangeably non-blocking networks (for example Benes networks [1]) with dilation to reduce the amount of cross-talk. 16 x 16 rearrangeably non-blocking modules were built with optical power loss of 13.4 dB per module ([2]). Thus in multi-hop environment some sort of amplification is required. A possible solution is a single stage of optical amplification or direct amplification ([3]).

We also propose an effective growability scheme both in the space domain (i.e., a way to compose large switches from smaller modules) and in the wavelength domain (i.e., in WDM networks).

3 Performance

Simulation and analytical results were obtained to investigate the probability of blocking. In general, the larger the switch size (n), the lower the loss probability for a given line utilization (ρ). Thus, for switches of 32×32, the P_{loss} at $\rho = 0.7$ is smaller than 10^{-8}.

Increasing the number of delay lines lowers the loss probability, since more "buffering" is available. This effect of increasing m is quite dramatic. For example, at $\rho = 0.8$, the P_{loss} decreases from $1.2 \cdot 10^{-3}$ to $6 \cdot 10^{-7}$ (i.e., about 4 orders of magnitude), when m increased from 16 to 32. Thus m may serve as a very effective design parameter to achieve a desirable level of performance.

The latency of the Staggering Switch depends on ρ, n, and m. In general, an increase in ρ, in n, and in m results in increase in average packet delay through the switch.

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MD1 TUNABLE OPTICAL FILTERS FOR LIGHTWAVE NETWORKS

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Introduction. In the past, wavelength multiplexed optical communication systems had not earned respectability as viable optical network strategies, due to tight system loss budgets and a limited menu of wavelength-sensitive building blocks. Recently, however, optical amplifiers have made loss a manageable device deficiency, while the evolution of tunable lasers, wavelength multiplexers, optical filters and wavelength-selective switches has made dense WDM systems technically feasible.

Role of the Tunable Optical Filter. The tunable optical filter is a key component in dense WDM systems because it can function in the transmitter, receiver and distributing areas of WDM networks: as the wavelength-selective element in a tunable laser, as the front end of a direct-detection receiver and, in the case of the acousto-optic filter, as an add/drop node in a fiber disribution network (Fig. 1). We will consider a broad class of optical filters which operate by imposing a normally forbidden transmission process but which provide a narrowband resonant and tunable means of defeating this transmission barrier.

Fabry-Perot Filters. The most familiar and most commercialized tunable optical filter is the Fabry-Perot etalon filter, in which a pair of highly reflecting mirrors become transparent on resonance. The Fabry-Perot is tuned by changing the optical path length between the mirror pairs, either by direct length adjustment (as in piezoelectrically-tuned filters) or by a change in the refractive index of a nematic liquid crystal film occupying the Fabry-Perot cavity [1]).

Mismatched Coupler-Filter. Other electronically-tuned optical filters work by grating-assisted coupling of optical waves which propagate at very different velocities. The coupler-filter is a mismatched directional coupler for which the two waveguides are evanescently coupled, but the modes in each waveguide have very different effective indices, resulting in an effective birefringence Δn. Resonant transmission between waveguides is achieved by modulating the coupling strength so that energy crosses between guides only when the contributions can add coherently. The phase matching criterion is that the modulation period Λ just equals the beat length between modes $L_{beat}=\lambda/\Delta n_{eff}$. Recently Alferness and coworkers demonstrated an InP-based vertical coupler filter in which two mismatched channel waveguides were coupled by a grating which was tunable by varying the injection current [2]. This was integrated with a gain section to produce a widely-tunable laser with over 50 nm of tuning range about 1550 nm.

Polarization Conversion Filters. Polarization conversion filters consist of crossed polarizers between which is placed a weak distributed wave plate which can rotate the polarization of incoming light. This transmission process is defeated by incorporating a highly birefringent medium with polarization beat length $L_{beat}=\lambda/\Delta n$ over which contributions to a flipped field are dephased. Resonant polarization conversion can be achieved, however, by synchronously alternating the weak induced birefringence with the beat length, either by an alternating electro-optic grating or by an alternating photoelastic coupling provided by an acoustic wave. The electro-optic tunable filter (EOF), relying on periodic electrodes, is only weakly tunable, while the acousto-optic filter (AOF) has a very wide tuning range.

Comparison of Filter Types. Table 1 compares the bandwidth, tuning range, tuning speeds and channel capacity of the resonant filters discussed above. All but the EO filter has a tuning range sufficient to cover the Er-doped fiber amplifier gain region. All filters have passbands of a nanometer or less, suitable for dense WDM. The Fabry-Perot filters are notably slow. The EO filter

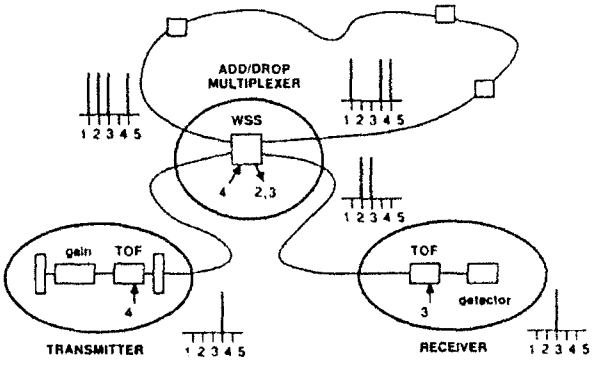


Fig. 1. System applications of tunable optical filters.

TYPE	PASSBAND	TUNING RANGE	SPEED	AVAILABLE CHANNNELS
Fabry-Perot	0.5 nm	>50 nm	ms	comb
Grating coupled	1nm	>50 nm	ns	one
Electro-optic	1nm	10 nm	ns	one
Acousto-optic	1nm	>300 nm	μs	arbitrary

Table 1. Comparison of tunable filter types and capabilities.

is only very weakly tunable. Although the Fabry-Perot filter provides a comb of passbands, all passbands move with the adjustment of the single available parameter of optical pathlength. The AO filter is the only filter capable of operating with many simultaneous and independent passbands. It is this feature which distinguishes the AOF most dramatically from the other candidates. The important applications which derive from this unique capability will occupy the rest of this discussion.

The AO Filter. The AOF uses RF-frequency surface acoustic waves (SAWs) to perform polarization conversion in the 1.3 to 1.6 μm optical communication spectrum. At a wavelength of 1550 nm, the drive frequency is 175 MHz, the drive power is 6.5 mW and the tuning range is over 300 nm, with a tuning rate of about 8 nm/MHz [3]. Fig. 2 (top) is a schematic of the integrated acousto-optic filter fabricated on $LiNbO_3$, incorporating singlemode titanium-indiffused channel guides for confining both optical beam and surface acoustic waves. Integral polarizing beamsplitters have been incorporated into the AO filter structure, resulting in a polarization-independent AO filter. Light coming into the upper input channel is decomposed into horizontal and vertical components which are separately filtered in waveguides sharing a common SAW beam, and then the processed light is recombined in another polarization splitter/combiner. Selected wavelength channels, for which horizontal and vertical polarization components were interchanged, recombine in the lower output port. Unselected wavelengths recombine in the upper output port, resulting in polarization-independent spatial separation of filtered and unfiltered light. This AO filter/switch can act as a wavelength channel interchange which allows two input fibers to exchange any number of wavelength channels by selection of the RF drives corresponding to the wavelengths to be exchanged.

Wavelength Crossconnects. There are numerous applications of the AO filter/switch. The use of the 2 × 2 AO filter as an add/drop node in a fiber ring was recently demonstrated, including the feature of self-routing by incorporating a node-specific pilot tone in the data spectrum of the wavelength to be dropped [4]. Fig. 2 (bottom) shows the connection of six 2 × 2 filters in a Benes network which acts as a 4 × 4 wavelength crossconnect. Each input fiber port can be connected to any fiber port, and the crossconnect setting can be simultaneously and independently configured for each wavelength channel, by the simultaneous application of RF drives of the appropriate frequency to the appropriate nodes.

Other Applications. The AO filter has been shown capable of acting as a wavelength-dependent active loss element (capable of servocontrol), for use in compensating for the nonuniformity of the Er-doped fiber amplifier gain. The AOF provides a controllable amount of loss in each wavelength channel by exploiting the analog nature of the AO filter switching characteristic [5].

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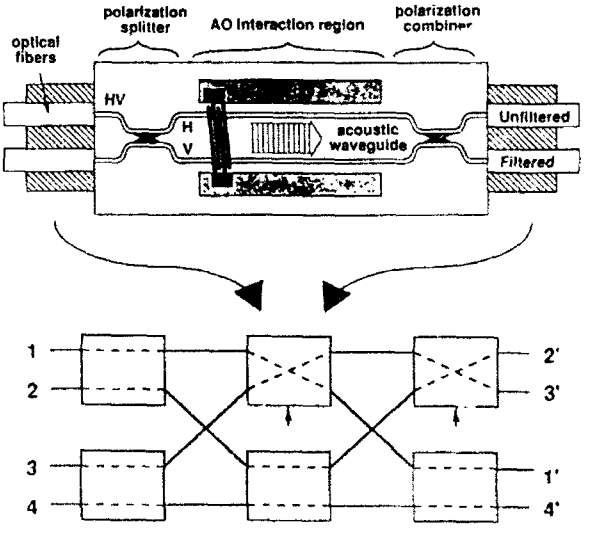


Fig. 2. (top) Polarization-diversity AO filter design (bottom) 4×4 wavelength crossconnect configuration.

MD2

BOUNDS ON THE NUMBER OF WAVELENGTHS NEEDED IN WDM NETWORKS

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1 Introduction

Consider the all optical network (AON) shown in Fig. 1a. The λ-nodes selectively route the signals on the input links to the output links based on wavelength only. We assume that the λ-nodes cannot be reconfigured, thus if there is a path from transmitter n to receiver m on wavelength λ, there is always such a path even if there is no traffic between n and m. Paths for three wavelengths, Red, Green, and Blue are shown in Fig. 1b. The only freedom, after the network topology (fig. 1a) and wavelength paths (fig. 1b) have been determined, is in the tuning of the transmitters and receivers. Note that this network can support any matching of the transmitters to two of the receivers (with no multi-casting) except the matching $T = \{(1, B), (2, C)\}$. The reason being that $(1, B)$ and $(2, C)$ must both use Red simultaneously. Since there is a path from 2 to B on Red, the two sessions collide at receiver B. This does not happen for any other pair.

In section 2, we present a lower bound on the number of wavelengths required to avoid collisions. This bound holds for any network topology with λ-routing and wavelength changing devices. We do not restrict ourselves, as we did in the example above, to traffics without multicasting.

We will see that for very large networks, $> 10^6$ users, λ-routing cannot provide full connectivity without some possibility of collisions. λ-routing can be combined with conventional circuit switching to produce networks of the type proposed by Stern [3]. In these networks, the λ-paths are reconfigurable. In section 3, we present a lower bound on the number of switching states required for a network with M users and F wavelengths. We show that unless $F \approx \sqrt{M}$, the number of switching states cannot be dramatically reduced from that of a conventional circuit switched network (F=1).

2 A Bound on the Required Number of Wavelengths

Let $s = (n, m)$ be a *session*, where n is a transmitter and m is a receiver. A *traffic*, T , is defined as a set of sessions. A receiver can be active in at most one session of a Traffic. A transmitter is permitted to be active in more than one session (multicasting). A *traffic set*, $\mathcal{T}$, is a set of traffics. The traffics, $T \in \mathcal{T}$ are the *allowable* traffics. Let $F(\mathcal{T})$ be the minimum number of wavelengths for any switchless AON needed to support $\mathcal{T}$ without contention. Then, we will show that

$$F(\mathcal{T}) \geq \left[\binom{M}{\rho M}^{-1} \sqrt{|\mathcal{T}|} \right]^{\frac{1}{\rho M}} - 1 \qquad (1)$$

where ρM is the maximum number of sessions that can be on at any time. $0 \leq \rho \leq 1$ is called the maximum utilization of the network.

Using eqn. 1, or variations of it, the number of wavelengths required for different $\mathcal{T}$ can be bounded. Three examples, all with maximum utilization, $\rho = 1$, are listed below. Upper bounds are obtained by construction. In each example, the best bounds known are presented. The last example shows that the lower bound can be very tight.

Arbitrary: $\sqrt{M} \leq F(\mathcal{T}) \leq M$

Each receiver can be paired with any transmitter.

Permutations: $\sqrt{\frac{M}{e}} \leq F(\mathcal{T}) \leq \lceil \frac{M}{2} \rceil + 2$

Arbitrary connections between transmitters and receivers without multicasting [2].

Blocking: $\frac{\sqrt{M}}{e} \leq F(\mathcal{T}) \leq \sqrt{M}$

Group the transmitters into disjoint sets, T-LANS, of size $\sqrt{M}$. Similarly group the receivers into R-LANS. Allow at most one active session between any [T-LAN,R-LAN] pair. A typical traffic is shown in Fig. 2. The upper bound construction can be implemented by making each T-LAN (R-LAN) a broadcast star.

[1]Research supported by the Army Research Office under contract DAAL03-86-K-0171

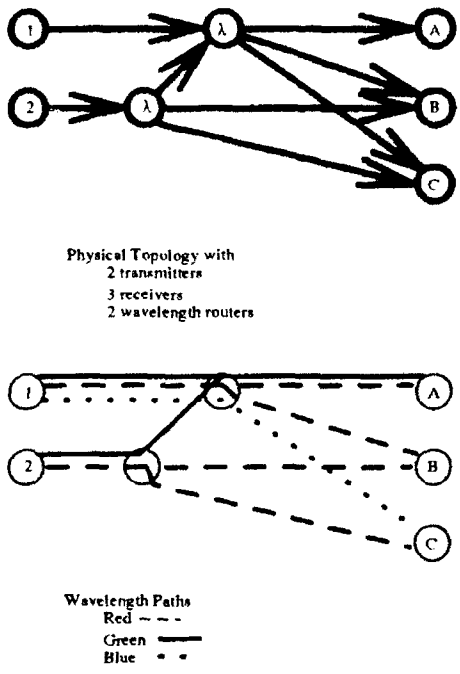


Fig. 1a,b

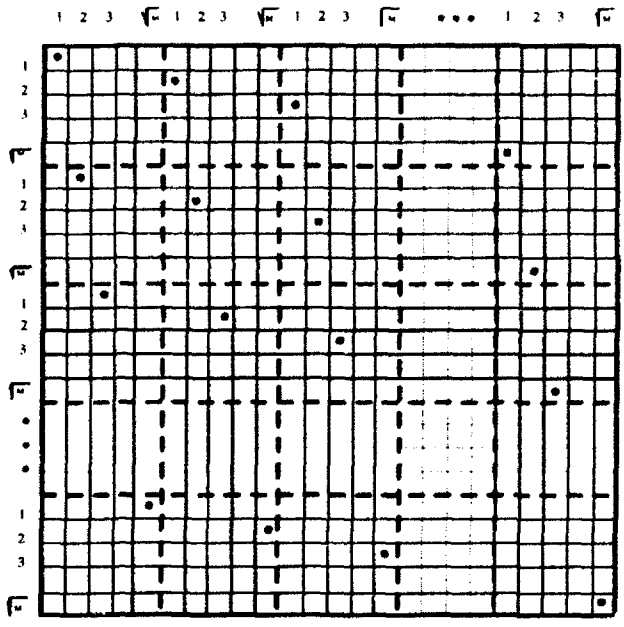


Fig. 2

3 Switching States

Now consider an AON with λ-routing, wavelength changers, and switches. Let S be the number of switching states. Then for permutation routing, the number of states is bounded below by

$$\log_2 S \geq M \log_2 M - 2M \log_2 F - 1.44M \qquad (2)$$

where F is the number of wavelengths. When $F = 1$, this agrees with the well known formula for the minimum complexity of an MxM non-blocking switch [1]. It can be seen that λ-routing cannot dramatically reduce the number of switching states unless $F \approx \sqrt{M}$.

4 Conclusions

Without switches, about F^2 users can be supported with F wavelengths with minimal blocking. For instance, dividing the fiber into 1000, 1 *Gbps* channels and using λ-routing, we can design a partially blocking network (Fig. 2) with 10^6 users. The maximum throughput is 1000 *Tbps*. Instead of blocking, wavelengths can be shared by using TDMA. In the worst case, 1000 users from one LAN connecting to 1000 users from another LAN, the user data rate is limited to 1 *Mbps*. It may be possible to design a switchless non-blocking fully connected network with F^2 users. This is an open question.

For networks with $\approx 10^8$ users, switches will be necessary. The main advantage here of combining λ-routing and switching is to reduce the frequency of changing states. This is because each state can handle many traffics (up to $\approx 10^6$!). This may greatly simplify control of the network.

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MD3 WAVELENGTH-CONVERTIBLE LIGHTWAVE NETWORKS

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ABSTRACT

A wavelength-convertible architecture for circuit-switched wavelength-division multiplexing networks is proposed in this paper. Wavelength converters shared by individual channel in the switch are used to enhance the performance. Routing algorithm is derived to conserve converters.

SUMMARY

Switch architecture In a circuit-switched wavelength-division multiplexin network, each switching node provides the cross-connect function using wavelength multiplexers and demultiplexers, optical signal couplers, and wavelength converters (Fig. 1). The nice features of this switch are: 1) wavelength converter can convert the wavelength of the incoming circuit, and wavelengths can be reused; and 2) the wavelength converters are shared by all the incoming circuits rather than having each converter dedicated to an incoming circuit, thereby reducing the number of required converters.

By implementing an efficient routing algorithm, it is very likely that most of the incoming circuits do not need any conversion, and very few wavelength converters may be necessary.

Routing algorithm A centralized dynamic routing algorithm is used to establish each circuit. This includes 1) a sequence of links for the circuit to pass through, 2) a channel in each of the above links for the signal of the circuit to go on, and 3) whether or not the circuit needs wavelength conversion at each intermediate node.

The routing algorithm finds the min-cost route where we model the cost function as the sum of individual cost due to using channels and wavelength converters. To facilitate formulating the problem, an auxiliary graph is created in which the channel and the wavelength conversion costs are interpreted as the arc weights of channel and converter arcs, respectively. The best route is found using the shortest-path algorithm.

Numerical results The algorithm is tested in the 21-node 52-link ARPA2 network with 16 wavelengths per link (Fig. 2). The results show that the blocking probability improves with wavelergth converters (Fig. 3). With our efficient switch architecture and routing algorithm, the number of converters required at each switch node is very small while achieving performance close to that of a fully-convertible network. For example, with three converters we can achieve a blocking probability close to that available in a fully-convertible network, i.e., 64 converters (16 wavelengths per link $\times$ at most 4 links per node in the ARPA2 network).

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Future research Several issues need further studies. Firstly, efficient allocation of wavelength converters needs to be investigated. Secondly, various converter models can be considered. Thirdly, a reconfiguring scheme which retunes the wavelengths or reroutes the links of existing circuits may further reduce the number of required converters. Finally, multi-cast services can be implemented in our wavelength-convertible lightwave networks.

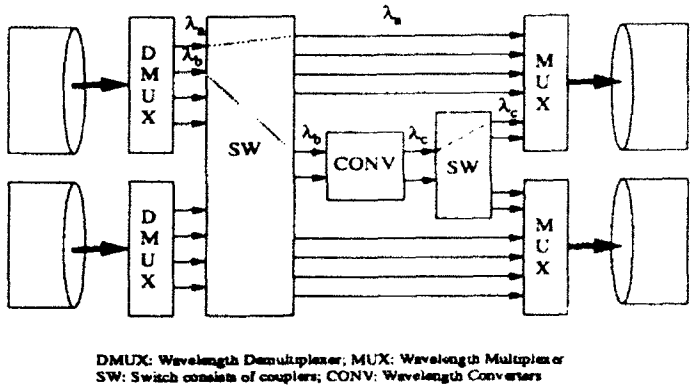


Fig. 1 Switch architecture in a wavelength-convertible network

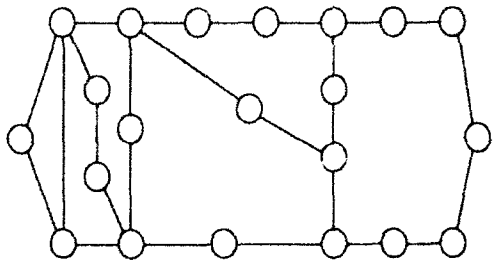


Fig. 2 The 21-node 52-link ARPA2 network

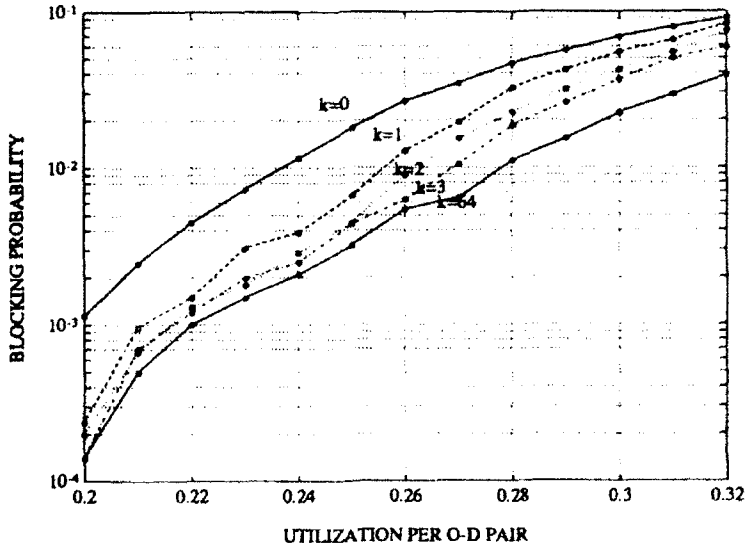


Figure 3: Blocking probability versus traffic loading at different numbers of converters k

MD4

WAVEBAND AND CHANNEL ROUTING IN A LINEAR LIGHTWAVE NETWORK

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This work is aimed at solving the problem of routing in a Linear Lightwave Network (LLN) [STE] with waveband selectivity. A LLN is an optical network in which the network nodes perform only linear operations on optical signals : power combining, dividing and possibly linear (i.e. non-regenerative) amplification. The transport of a signal from a transmitter to a receiver is all optical, with no electro-optic conversion taking place anywhere except at the transmitters and receivers themselves. Thus the network contains no "electronic bottlenecks". Furthermore, LLN's can have arbitrary topologies for reliability and load distribution.

The heart of the LLN is a Linear Divider-Combiner(LDC) located at each node. Its function is to direct prescribed combinations of the inbound signals at the node to each outbound fiber. It thus acts as a generalized optical switch, with the added functions of multicasting (signal dividing) and multiplexing (signal combining). The LDC's are electronically controllable under the command of a network manager. In this paper we assume that the LLN is operated in a circuit-switched mode, so that upon receipt of a call request, the network manager routes the call through the network by appropriately adjusting the parameters of the LDCs along the desired path. In a general LLN, routing can be performed in a waveband selective fashion, resulting in an additional degree of freedom. Waveband selectivity is acheived by making the LDCs waveband selective. Figure 1 shows an example of a LLN with waveband selectivity. Node B is blown up to show the details of an LDC. The optical spectrum is split up into wavebands with each waveband further subdivided into channels. Signals on each input fiber are demultiplexed into different wavebands $1, 2 ... K$. These demultiplexed signals are then sent to LDCs $1, 2, ... K$, where each LDC uses electronic control $\alpha_1, \alpha_2, ... \alpha_K$, to perform the required switching, splitting and combining of signals independently for its waveband. The signals are then recombined onto their respective output links by using a multiplexer. In the example shown in Figure 1 there are two wavebands and two channels per waveband.

A fiber in the LLN will normally carry several calls which must each be assigned to a distinct (waveband, channel) pair to ensure correct reception. Calls sharing the same fiber are referred to as interfering calls. Physical and cost constraints limit the number of wavebands and channels on each fiber. Calls allocated on the same waveband are subjected to certain constraints in an LLN[BSB]. These constraints arise owing to the fact that signals on a single waveband once combined on a fiber cannot be separated within the LLN (The selectivity of the LDC is fine enough to distinguish wavebands but not channels within the wavebands). The basic routing problem is that of choosing a feasible path through the network for each new call request and allocating a (waveband, channel) pair, taking into account the the various network constraints. If no feasible path is available, the call is blocked. The routing algorithm presented in this work is evaluated using the criterion of blocking probability. Details of the routing problem in networks without waveband selectivity can be found in [BSB].

This work focuses on waveband selective LLNs, using the following routing algorithm. A W list of the wavebands is kept with the least used one at the top. Starting with the waveband at the top of the list, an attempt is made to allocate it to the call. The physical path for the call is chosen from among **K-Shortest Paths(K-SP)** between the source and destination. From among the K paths the one that interferes with the least number of other calls in progress that use the chosen waveband, without violating the LLN constraints, is allocated to the incoming call [BSB]. Within the waveband the call is allocated the least used channel from among all channels with which it does not interfere. If a feasible path or channel cannot be found within this waveband then the next waveband from the W list is selected and the process is repeated until the call is successfully allocated or blocked.

A simulator evaluated the performance of the LLN using the routing algorithm proposed above with K=2. A random network was simulated, having 20 nodes (one transmitter per node) with an average degree of 3. Since the intent was to study the performance of the network, infinite receivers were simulated at each node to preclude the possibility of blocking due to receiver contention. A two state Markov chain was used to model each source with average idle ("on hook") time $1/\lambda$ units and average call holding time $1/\mu$ units. The load, λ/μ was varied from 0 to 5 units. The total number of channels in the optical spectrum was fixed at 4 and the number of wavebands was varied. The following pairs were studied - (1,4), (2,2) and (4,1) where (1,4) indicates that there is one waveband and 4 channels per waveband in the LLN. These numbers

do not have any technological significance and were chosen arbitrarily because the intent was only to make a comparative study. The numbers on the Y-axis in Fig. 2 represent the blocking probability. As is to be expected an improvement in performance is seen as the LDCs are made more waveband selective. The best performance is achieved for the case when each waveband has only one channel. Curves of this type are useful in evaluating the trade-off between improved performance and increased LDC cost and complexity as the number of wavebands is increased. Other (waveband,channel) allocation heuristics are also being studied.

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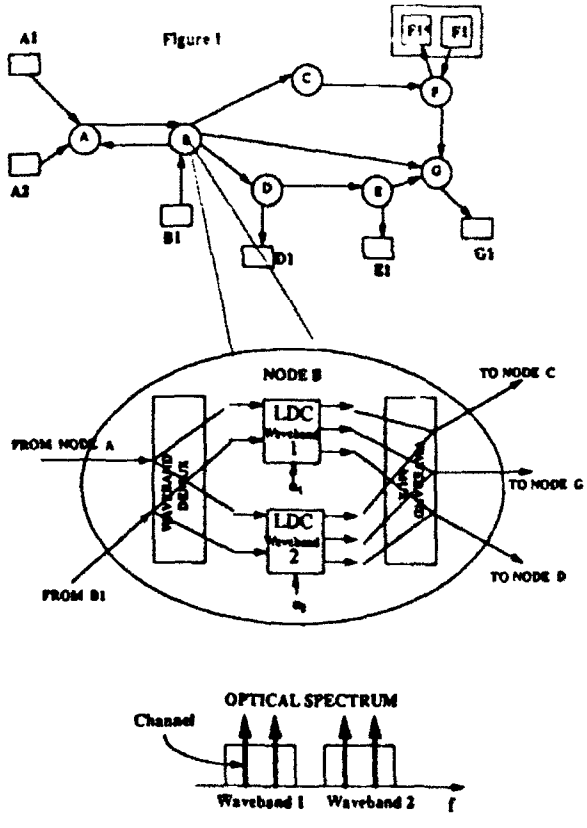
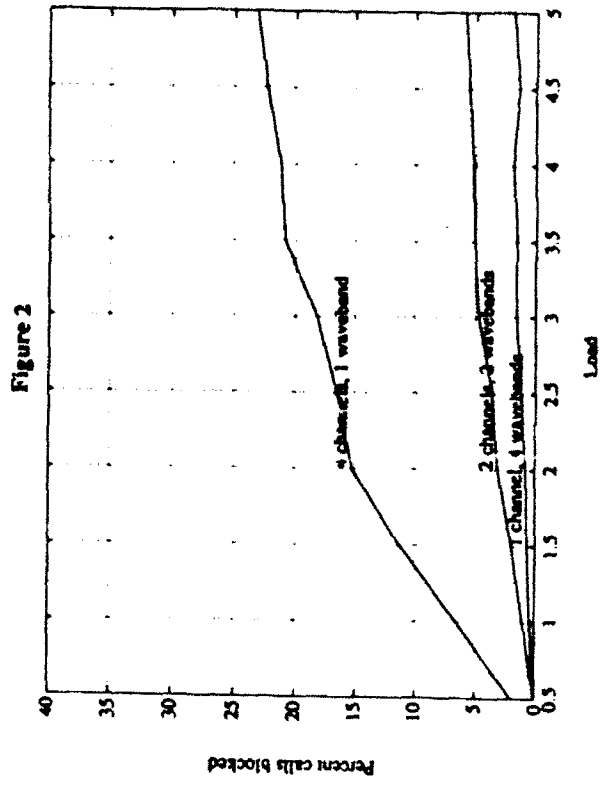


Figure 1



Tuesday

August 4, 1992

TuA: Optical Network Evolution

TuB: Multihop WDM Networks

TuC: Time Domain Technologies

TuD: Multiple Channel Networks

TuA1

OPTICAL NETWORK DEMONSTRATIONS IN THE EUROPEAN RACE PROJECT

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Abstract : RACE I and RACE II optical network demonstrations are reviewed. RACE II work and earlier field demonstrations in BT's London fibre network of reconfigurable networks incorporating optical switches, optical amplifiers and wavelength selective elements will be discussed in detail.

Background : The research and technology development in advanced communication technologies in Europe (RACE) programme started in 1985. The initial phase defined the overall target, determined common functional specifications and developed implementation strategies. The objective was the "Introduction of Integrated Broadband Communication (IBC) taking into account the evolving ISDN and national introduction strategies, progressing to Community-wide services by 1995". This phase was followed by the RACE I projects which explored numerous technology, networking and service related options for achieving the overall goal. The latest phase, RACE 1992 (RACE II), moves the program from research towards development and ultimately implementation.

The overall effort within the RACE I and RACE II programs is ~2500 MECU with a total Community financial contribution of 1039 MECU. This is split between about 160 projects formed from consortia of numerous companies in EEC and EFTA countries. In all there are more than 350 separate organisations and around 2000 persons contributing to the RACE projects at any given instant.

The RACE programme embraces all aspects of advanced communications from intelligent networking and services, switching, information security, test infrastructure, mobile radio, image processing and handling through to optical networking [1]. The project is organised into seven project lines which bring together related work areasas outlined above. All projects and project lines contribute to a consensus management project (R1045) which is responsible for generating common functional specifications used in the preparation and coordination of contributions to international standards bodies and in establishing common practices for the development and implementation of IBC.

Optical Networking : The optical networking project line is comprised of 35 projects, 20 within RACE II. The following list details some projects which incorporate optical network demonstrators :

Project	Acronym	Title	Lead Partner (+ partners)
R1010	CMC	Subscriber Coherent Multichannel System	Philips BV (+ 5)
R1030	ACCESS	Advanced Customer Connections, an Evolutionary System Strategy	NKT Elektronik (+ 12)
R1033	OSCAR	Optical Switching Systems, Components and Applications Research	GEC Marconi Research (+ 12)
R1036		Wavelength and Time Division Multiplexed (WTDM) Broadband Customer Premises Network	British Broadcasting Corporation (+ 9)
R1051		Multi-Gigabit Transmission in the IBC Subscriber Loop	Alcatel SEL AG (+ 7)
R1057	AQUA	Advanced Quantum Well Lasers for Multi-Gigabit Transmission Systems	Alcatel SEL AG (+ 8)
R2001		WTDM Pilot Installation	British Broadcasting Corporation (+ 11)
R2014		First-Fibre to the Residential Subscriber Terminal	NKT Elektronik (+ 9)
R2028	MWTN	Multi-Wavelength Transport Network	BT Laboratories (+ 9)
R2039	ATMOS	ATM Optical Switching	Alcatel Alsthom Recherche (+ 10)
R2065	COBRA	Coherent Optical Systems for Business Routing and Access	Philipls BV (+ 7)
R2070	MUNDI	Multiplexed Network for Distributive and Interactive Services	Siemens AG (+ 5)

Projects within the optical networking project line fall within three basic categories :

1 : Local access : passive optical networks / customer premises networks
2 : Core : distribution and switched networks / point to point systems
3 : Components and technologies.

Demonstrators form an important part of all projects especially in RACE II where the emphasis is towards development and implementation. Component and technology programs have a strong demonstrator base, eg. R1033 with the ACCESS [2] and OPTIMUSS [3] testbed demonstrations at the ECOC/IOOC'91 exhibition. R1051/R1057 also demonstrated at ECOC/IOOC'91 the distribution of 64 (HD)TV channels coded at 140 Mbit/s (total bitrate 8.96 Gbit/s) to 262144 subscribers in an optically amplified optical distribution network. Similarly, R1036 has demonstrated an optical path through a passive star network carrying digital TV signals at 155 Mbit/s and a PRBS at

2.5 Gbit/s. This network is capable of carrying signals at a wide range of bit rates from low speed data to HDTV us ing a combination of electrical time division and optical wavelength division multiplexing [5].

A number of RACE II projects build upon experience gained within earlier RACE I projects which are now in their last year. One example is the R2028 MWTN project for which BT Laboratories is the lead partner. This project brings together many areas of expertise gained from earlier RACE I projects in particular, optical switching from R1033 and fine grain technology from R1027, and combines these with the wavelength routed optical networks work of BT Laboratories [6]. An earlier informal collaboration between BT Laboratories, Ericsson and Pirelli established the viability of incorporating optical switches and erbium doped fibre amplifiers within reconfigurable wavelength routed network nodes [7]. This work has led to numerous experimental network demonstrations on installed optical fibres within BT's London optical fibre network [8] including the flexible routing of a 1.56 μm channel and the demonstration of wavelength drop and insert from an optical transport layer. The ideas generated by these early network demonstrations have been combined with the expertise of other MWTN consortium partners and have resulted in a network node design, figure 1, which incorporates power splitters, wavelength selective elements, optical switch matrices, variable attenuators, multiwavelength sources, optical receiversand optical amplifiers. This node architecture and others will be investigated within the MWTN R2028 RACE project. These reconfigurable network nodes will be demonstrated in numerous network configurations. An integral part of these demonstrations will be the control, management and monitoring of the network, it's configuration and the status of the individual network components. The purpose of these investigations will be to gain further experience in optical networking and to determine any factors which will limit the network performance and dimensions.

Conclusion : Optics is recognised in the European RACE project as being of key importance in the roll out of integrated broadband communications in customer premises networks, local access networks and core transmission networks. Numerous demonstrators have shown that the combination of optical techniques and optical networking principles with conventional electronic approaches can provide communications networks which will be flexible and reliable providing a suitable platform for tomorrow's networks and services.

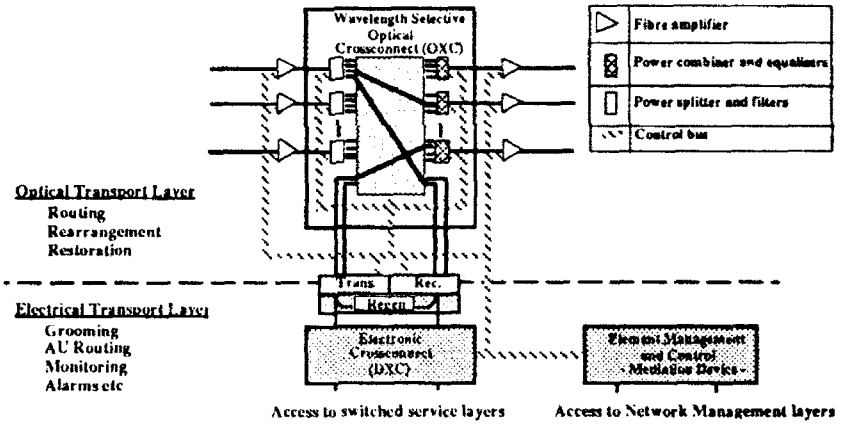


Figure 1 : Optically Reconfigurable Network Node and Functionality (R2028 MWTN RACE Project)

Acknowledgements : This work was partially sponsored by the European Community under the MWTN RACE project R2028.

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TuA2

TOWARDS AN ALL-OPTICAL TELECOMMUNICATIONS INFRASTRUCTURE

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As a discipline for focused research activity (but certainly not yet as an example of a successful commercial reality) the field of optical networks has most distinctly emerged from its infancy and has now entered its early adolescence. The early years were dominated by emphasis on the physical layer: physical topologies, passive optical components and active electro-optic devices which could be arranged in such a manner as to permit the creation of multiple distinguishable communication channels, all sharing a common fiber-optic medium. These channels would consume a proportionately larger fraction of the enormous bandwidth potential of the medium (and thereby support a correspondingly higher capacity) as compared against a single-channel point-to-point transmission link operating at a data rate equal to any one of the "optical network" channels. The two basic techniques considered for the creation of such multiple channels were wavelength division multiplexing (using either optical multiplexers/demultiplexers or, for finer line spacing, coherent optics) and time division multiplexing (using time-multiplexed streams of the narrow pulses created, for example, by a mode-locked or gain-switched laser; code-division multiplexing is a variant of this time-division approach).

In the opinion of this writer, the field of optical networks today has much more of a systems orientation. The focus has decidedly shifted from the creation of multiple channels to the allocation of these channels among a multiplicity of high-speed users, each offering multimedia traffic to the network and each demanding some guaranteed quality-of-service. From a systems perspective, the optical network might appear as shown in Figure 1. Here, users connect to the optical medium via geographically distributed access stations (shown as circles) which also contain the electro-optic converters. The medium itself is non-processing, and through the use of optical amplifiers, can provide service over wide-area service regions. The medium accepts the signals generated by the various users and delivers these over either the whole or a limited portion of the overall service region. In the aggregate, the medium creates a large capacity pool (measured in Terabits/sec.) which can be allocated upon demand, although no one user can access on a packet or circuit basis at a rate greater than that set by the electro-optic converters. The network supports connections among users and between users and some distributed service environment. The distributed management environment supports and integrates various classes of traffic through a combination of circuit and packet switching, and also manages faults and overall system growth.

Also in the opinion of this writer, the most appropriate technique for the creation of a wide-area optical infrastructure along the lines expressed above is wavelength division multiplexing. WDM supports transmission format-independent channels (TDM requires constant-rate digital signals), and, through the use of optical filters, permits signals to be guided to their intended receivers, thereby permitting wavelength reuse in geographically disjoint regions of the network. By tuning such

filters, the connectivity among access stations can be rearranged to dynamically track changing traffic patterns and avoid failed network elements. As optical device technology matures, the same basic WDM infrastructure accommodates faster E/O conversion and/or improved coherent multiplexing techniques. Through the use of a multihop overlay, Asynchronous Transfer Mode self-routing cells can be transported, thereby enabling a full range of multimedia Broadband ISDN services. The network is both modular and scalable up to wide-area configurations supporting hundreds of millions of access stations by appropriately routing and reusing a limited set of wavelengths available to each station, and quality-of-service guarantees can be provided over each connection.

The key device and systems technologies needed to enable the wide area optical infrastructure are (1) low-noise optical amplifiers with flat passbands; (2) low cross-talk tunable filters; (3) wavelength agile transmitters and receivers to permit reconfiguration on a circuit basis (or on a very long file packet basis); (4) traffic control algorithms; and (5) fast, distributed logical reconfiguration algorithms involving the core network tunable filters and the user's wavelength agile elements; and (6) an overall architectural design which sensibly integrated device capabilities, physical topology, logical topology (access station connectivity), management/control, user interfaces, high-speed protocols, terminal architectures, and applications (low and high speed).

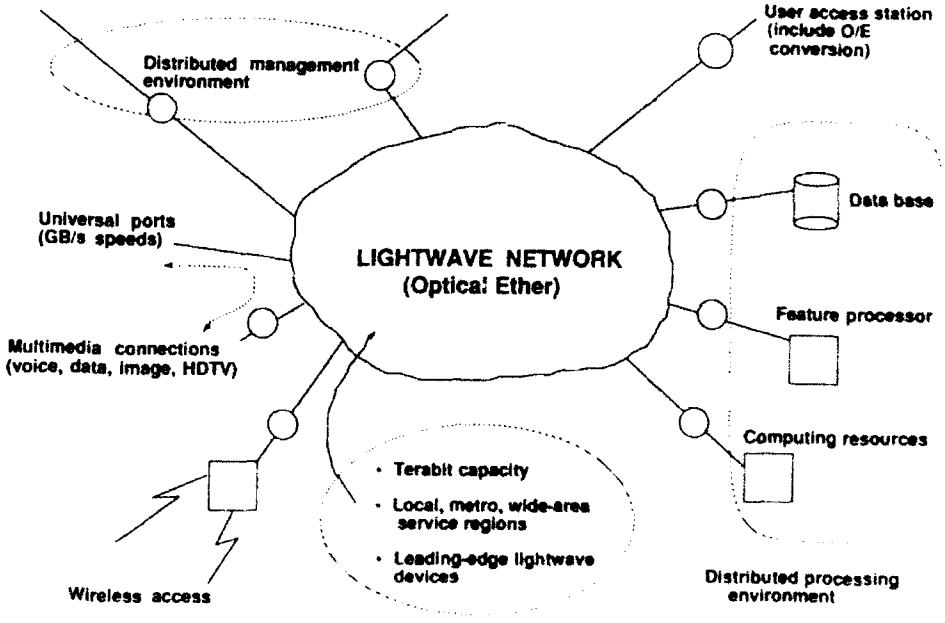
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TuA3 INTRODUCTION AND EVOLUTION OF OPTICAL ACCESS NETWORKS FOR BUSINESS AND RESIDENTIAL APPLICATIONS - VIEWS FROM RACE

P. Polese (RIC/Alcatel Italia - FACE), J. Vandenameele (Alcatel Bell)

1. INTRODUCTION

Different demand and traffic aspects are considered; main characteristics of the different services suitable for business and residential users are given

2. REFERENCE CONFIGURATIONS AND FUNCTIONAL ARCHITECTURES APPLIED TO OPTICAL NETWORKS

To ensure that all functions are covered in a consistent way a model has been adopted within RACE and Project R1044 in particular: the Reference Configuration (RC). It has been improved to cover new requirements imposed by the new services to be handled and to take into account the influence of new technologies.

The RC concept also provides the means of ensuring that different elements of the network can be interconnected in an effective manner and that the various technical and evolutionary options can be integrated to form a coherent network.

RCs are composed of functional groups and reference points. The arrangements of the functional groups and reference points can anticipate possible physical realisations which are represented by Functional Architectural Models (FAM). The paper will first address the optical aspects of the FAMs and discuss the different options for switched and non-switched services, covering optical integration (WDM) and electrical integration (TDM, ATM).

A major attention will be given to point-to-multipoint functional architectures where use is made of the Branching functional grouping (BRAN). Functions involved will be listed and discussed.

3. TECHNOLOGIES AND REALIZATIONS

The link will also be made with realization options proposed by two RACE projects in the technology area showing the mapping between the functions of the RC and the physical blocks of the technology project.

In order to enable an optical integration of services on the access line, agreements have to made on the allocation of the wavelength spectrum to the services to be covered. RACE has worked out a proposal in 1989 that has been improved last year. The proposal contains two wavelength allocation plans using the five wavelength bands 800 nm, 1300-nm, 1300+nm, 1500-nm and 1500+nm. They will both be discussed in the paper.

The paper also discusses the role of advanced technologies in access networks. Special attention is given to ATM, passive optical technologies and optical amplifers. The role of MAN as an evolution step towards B-ISDN and as a gathering network is also addressed, together with the evolution in optical MANs.

4. POSSIBLE INTRODUCTION STRATEGIES AND EVOLUTION SCENARIOS

In order to analyse and compare the more interesting evolutionary scenarios a suitable methodology has been developed within R1044/EPF. The new robust methodology can deal with clusters of new and not completely defined services, multiple system transitions and complex regulatory scenarios.

An evolutionary graph covering the most interesting evolution steps and paths towards IBC realisation is discussed.

Key issue in the successful introduction of B-ISDN services is the choice of the most appropriate Community Of Interest (COI) to be served.

A COI may include different types of subscribers belonging to different activity sectors that need to have relations in their working activities (e.g.: the publishing COI includes publishing companies, press agencies, large and small printing companies).

Among all the possible technological transitions from the existing situation towards the B-ISDN the more relevant ones have been focalised, namely:

- Pre-provisioning timeframe considering the evolution from the provision of existing services on existing networks to pre-provisioning of optical fibres to residential users and to the deployment of optical fibres and SDH systems to business users, introducing broadband services on leased lines

- Short term service provisioning timeframe characterized by the provision of semi-permanent connections and/or MANs for interactive services (mainly business users) and of semi-permanent connections and/or PONs for distributive services (mainly residential users)

- Medium term service provisioning timeframe characterized by the provision of switched (STM, ATM, MANs) interactive services as well as semi-permanent connections for distributive services using PONs

- Long term service provisioning timeframe characterized by the provision of switched (ATM) interactive and distributive services and of semi-permanent connections for distributive services, by the deployment of CMC techniques (50 GHz) in the access network and of optical switching

Different access configurations were studied in order to select the more appropriate ones and to evaluate the investment required for their deployment.

Various scenarios for the introduction of FTTH based on PON topologies are under study. The evolution of existing CATV users and their connection to B-ISDN is evaluated in this paper.

5. CONSIDERATIONS & CONCLUSIONS

Main available techno-economic results and the relationship of main variability factors are discussed. Guide-lines for network planning and design derived from the gained experience are given.

Main preliminary conclusions (the activity is still continuing) are reported.

TuB1

SCALABILITY AND MODULARITY IN MULTIWAVELENGTH OPTICAL NETWORKS

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The problem of creating both scalable and modular multiwavelength optical networks has only recently begun to be addressed. The lack of scalability is usually caused by the use of shared transmission media such as passive stars, busses, or rings. Simultaneous interconnection of many node pairs on a two-by-two basis then requires that each connection be allocated at least one wavelength, with the result that the number of wavelengths required scales linearly with the size of the network. If all nodes need to be simultaneously addressable by all other nodes, as in a completely connected mesh network, then the number of wavelengths must be identical with the number of nodes. The number of available wavelengths is, however, not unlimited. Despite the low loss of the fiber medium over some 200 nm, for all practical purposes the usable bandwidth of fiber networks is limited to the spectral region where fiber amplifiers have their gain. For the moment at least, that remains the erbium doped fiber amplifier (EDFA) bandwidth of about 30 nm or so. The number of wavelengths which may be independently addressed within that bandwidth is a function of the technology to be used. Theoretically, the capacity of the fiber is $B \cdot N = \Delta f/\rho$, where B is the bit rate per wavelength channel, N is the number of wavelength channels, Δf is the bandwidth available, and ρ is the spacing between channels measured in units of the bit rate. A value for ρ which is typical of many coherent transmission experiments is on the order of 20. Theoretically, ρ can be as low as 3 to 5 for various technologies, even in direct detection WDM (wavelength division multiplexed) systems. Practically, assuming a value of 20, N could be as high as 200 for B = 1 Gb/s. This is the information bandwidth limit.

Other limits which are more germane for optical networks, where tunability of components is an issue, are the limited resolution of the optical filters used, the registration and stability of the wavelengths, and crosstalk. A practical value in WDM systems may therefore be as low as a few tens of wavelengths. This is significantly lower than commonly assumed, and is largely due to the need to distribute both sources and filters over a wide geographic area and in varying environments to form real networks. The issue, then, is how to make scalable networks using only a few wavelengths.

We define scalability to be the ability to always be able to add one more node to the network, and modularity to mean the ability to add just one more node if desired. There are three key elements in making scalable networks: wavelength reuse, wavelength translation, and multihop interconnections. Wavelength reuse is most efficiently accomplished with wavelength routing techniques, where wavelength dependent components are used to direct the signals through the network along paths which are determined by their wavelengths and the ports at which they originate. Wavelength translation is the process of transferring the information on the signal from one wavelength to another. This allows the signal to move through the network, shifting from one wavelength to another as needed, until the destination is reached. It is an essential ingredient in minimizing the blocking characteristics of the network. If wavelength translation is implemented in the access nodes under switched control, a multihop network architecture results, with the possibility of packet-by-packet wavelength translation.

These three principles are illustrated in Fig. 1. The interior part of the network is optically transparent, with the wavelength routing being accomplished in the wavelength (WDM) cross-connects. λ_1 is seen to be reused in the interconnection of access node A to B and C to D, λ_3 is a

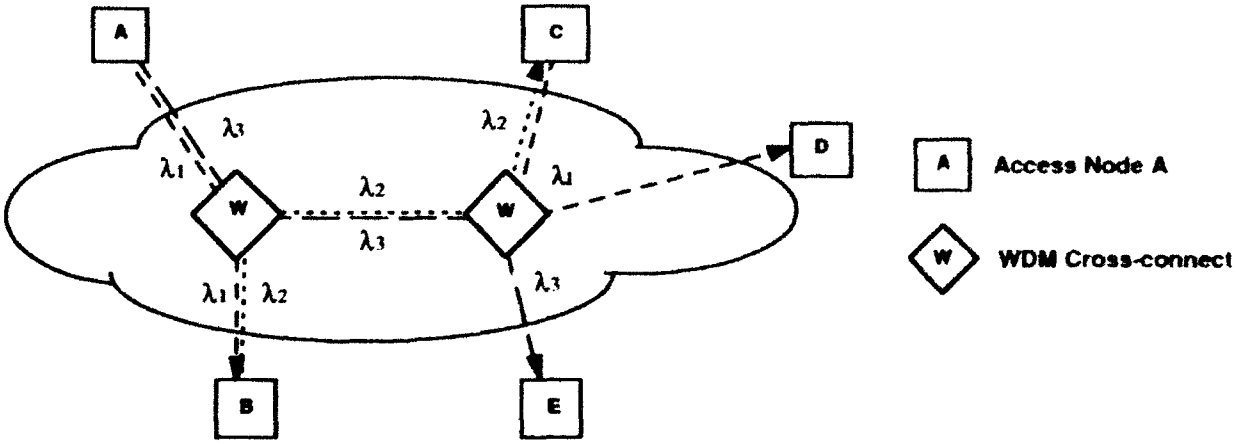


Fig. 1. A wavelength routed network architecture employing wavelength translation and multihop switching.

one-hop path between nodes A and E, and a multihop connection from node A to node C is achieved by taking A-to-B on λ_1, and B-to-C on λ_2. The interior part of the network is all-optical; the signals travel from access node to access node without detection. The access nodes perform the wavelength translation under switched control to take advantage of the different routes established by the wavelength routing network. A key feature of this sort of network is that each access node can directly access on a one-hop path as many nodes as there are wavelengths to which it has access. These one-hop destination nodes may be either local, or distant, and the choice of these one-hop paths is one of the key parameters to the efficient use of the network. One would, heuristically, choose the one-hop connections to serve either the highest traffic routes, or those requiring the highest performance, according to some algorithm which may operate in at least quasi real time. The one-hop paths may also be used to transport alternate service formats, as for example simultaneous digital and sub-carrier analog signals, or a combination of ATM and Fiber-Channel protocols. The inner, all-optical portion of the network of Fig. 1 would most likely be used in a quasi-static mode in which it is rearranged to meet the changing needs of the network traffic distribution and performance requirements, but would probably not be rearranged on a packet-by-packet basis.

The wavelength routed network of Fig. 1 can be made rearrangeable by using acousto-optic tunable filters (AOTF) to form NxN WDM cross-connects. The AOTF is a two-by-two exchange-bypass switching element which allows each wavelength to be switched independently with a response time of less than 10 μs. The extension of the 2x2 AOTFs to NxN cross-connects is subject to cross-talk limitations and therefore may require dilation in a manner similar to ordinary directional coupler switching structures.

In this talk we will show the beginnings of a network architecture which embodies these principles in forming a network scalable to national size at Gb/s access speeds, scalable to millions of nodes using as few as 8 wavelengths, with total network capacities exceeding millions of terabits per second. We will illustrate the abilities of such networks to produce multiple virtual networks with logical connectivity which is independent of the physical interconnection pattern, and we will discuss the technologies and techniques for realizing such networks.

TuB2

WAVELENGTH-BASED PACKET SWITCHING IN ATM MULTIHOP OPTICAL NETWORKS

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Wavelength agile lasers and optical receivers (e.g., electro-optic and acousto-optic filters) provide the technological platform upon which wavelength-based packet-switched services may be implemented in optical multiaccess networks. In large, high capacity optical networks, however, the fundamental limitation on providing wavelength-based packet switching is not necessarily the device agility. The relatively small number of total WDMA channels and the ability to resolve WDMA channel contention are other major issues that must be addressed.

We propose a multihop wavelength-based packet switched optical network architecture that is capable of supporting thousands of concurrently active users, each operating at a data rate of at least 1 Gb/s. As in other multihop approaches[1, 2], each user connects to the network via a Network Interface Unit (NIU) that is directly connected to a small number p nearest neighbors. If the packet destination is not one of the p nearest neighbors, it will hop through intermediate NIUs – functioning as packet switches – until it reaches the destination. In previous architectures, each NIU input/output port required a dedicated laser transmitter and receiver, and because these electro-optic components are the most costly and least reliable constituents of the NIU, p typically ranged from 2 to 4. An advantage of the proposed architecture is that the interconnectivity of NIUs is provided by WDMA channels selectable on a packet-by-packet basis; p is limited only by the tunability of the optical transmitter/receiver. Increasing p reduces the expected number of hops, thereby increasing the overall network capacity. The tuning may be implemented at either the laser or the optical receiver: for purposes of this discussion consider a tunable transmitter, fixed receiver approach.

The network consists of unconnected optical passive broadcast $(p+1)$x$(p+1)$ stars (Fig. 1). Each star supports p WDMA data channels and one WDMA clock channel. The optical clock signal, operating at the ATM cell rate, is used to allow synchronous slotted transmission of cells across the star. Although the transmitters and receivers sharing a star operate synchronously, stars operate asynchronously with respect to each other. An advantage of this topology is that the same WDMA channel may be used concurrently within different stars, thereby allowing the network to support more users.

Each NIU functions as a 2x2 space switch in which one input and output port serves as a bridge between two stars, and the other input and output port connects the user (Fig. 2). The NIU's output buffer on the network side is partitioned into p virtual FIFOs, each corresponding to one of p WDMA channels. To avoid WDMA channel contention, a cyclic TDMA service policy is used by each tunable transmitter. One TDMA frame is composed of p ATM cell length slots such that information in slot j is transmitted on wavelength λ_j by transmitter n and on wavelength λ_{j+1} by transmitter $n+1$. During each successive time slot, an ATM cell is read out from the next successive FIFO. Because each TDMA frame is composed of p slots rather than N as would be required by an N user single hop (star) network, the queueing delay experienced under low loads is kept small – on the order of the internode propagation time in LANs. The rate at which queueing delay increases with increasing load is minimized by employing a packet routing strategy that smoothes out the statistical variations in load amongst the FIFOs. We developed an Adaptive Shortest Path (ASP) routing procedure that accomplishes this while guaranteeing that packets are delivered along a minimum hop path.

ASP routing is accomplished by the following rule: ***choose the output FIFO from the subset of all output FIFOs on minimum hop paths to the destination that has the minimum local queueing delay.*** This algorithm takes advantage of the fact that in highly interconnected networks there are multiple minimum hop paths. For example, in a 162 node $p = 9$, 2 column ShuffleNet[1], over 44% of the packets can be placed in ***any*** of the 9 output FIFOs on their first hop, and still follow a minimum hop path.

Fig. 3 is the probability density function of delay in the above 162 node ShuffleNet with a single tunable transmitter for two routing algorithms; a real-time ASP self-routing algorithm that employs only local information – FIFO occupancies, current address, and destination address – and the fixed path minimum hop routing algorithm[3]. ASP routing not only reduces the mean delay experienced by a packet but, more significantly, reduces the variance of the delay. Both of these effects increase dramatically as the average load on the network increases. Minimizing delay variance is an important issue for broadband multimedia traffic such as real-time video. Fig. 4 illustrates the throughput-delay characteristics, under uniform traffic flow, of a 160 node $p = 2$, 5 column conventional two transmitter ShuffleNet, and the ShuffleNet from Fig. 3. Even

with half the number of lasers, the proposed network demonstrates better performance, and this advantage grows larger as the number of users or geographic size of the network increases.

In summary, we present a multihop optical network architecture that offers increased capacity and supports more total users relative to conventional multihop networks. This architecture also minimizes the use of electro-optic components, potentially lowering cost and improving reliability. Wavelength-based packet switching provides a larger fanout per node, thus increases network capacity by reducing the amount of relayed traffic in the network. The network topology provides for concurrent reuse of WDMA channels, so thousands of users may be supported. A cyclic fixed TDMA service policy for scheduling WDMA channel transmissions and an adaptive shortest path ATM cell routing procedure (ASP) that reduces average delay and delay variance are described.

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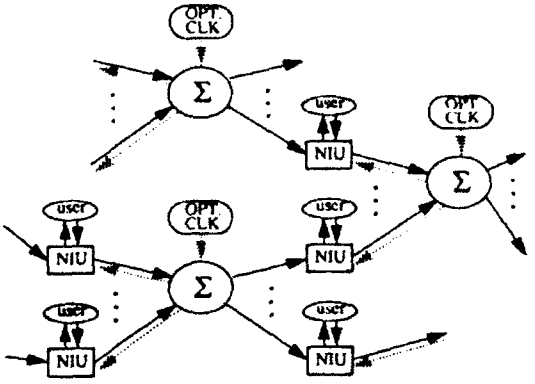


Fig. 1 Network topology. The optical clock signal is broadcast backwards to each transmitter for slot synchronization.

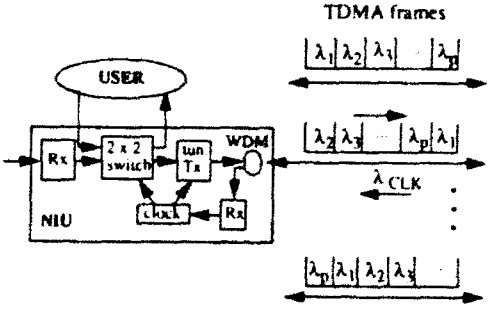


Fig. 2 NIU functional diagram. The TDMA frames used to schedule the WDMA transmission sequence of the p transmitters sharing each star are also shown.

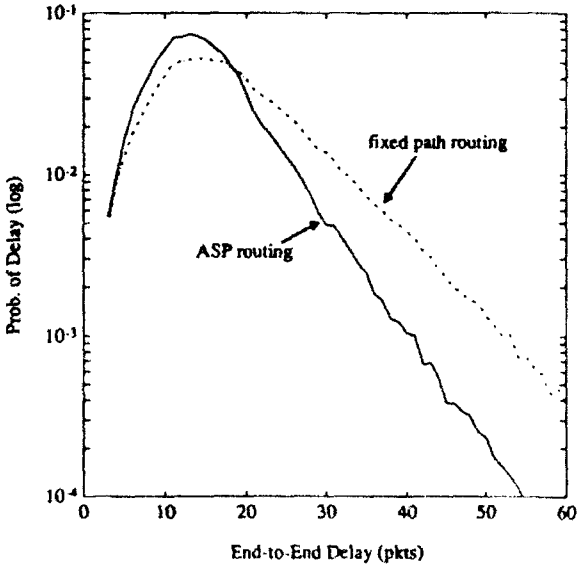


Fig.3 Delay probability density function in a 162 node p=9 tunable transmitter ShuffleNet at 24% uniform load with ASP and fixed path routing. Inter-NIU distance is 0 km.

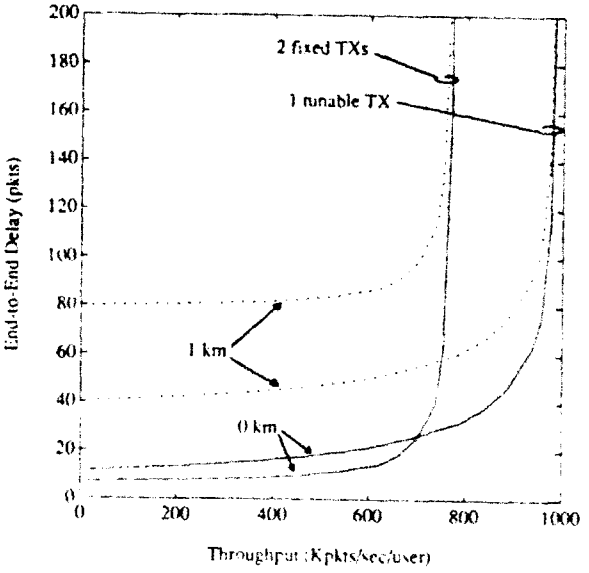


Fig.4 Comparison of a 160 node p=2 fixed transmitter ShffleNet and a 162 node p=9 tunable transmitter ShuffleNet with uniform traffic, 1 Gbps ATM cells, and two inter-NIU distances.

TuB3 OPTIMIZED ShuffleNet CONFIGURATIONS USING WDM CHANNELS

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I. INTRODUCTION

In recent years, the growing sophistication of the network users has resulted in an increased demand for multimedia services such as real-time voice, video, high-resolution graphics, distributed data bases, distributed computing among high-performance systems, etc. These applications require fast delivery of high volume of traffic over a larger area. To satisfy these demanding needs, fiber-optic medium, which offers a very high bandwidth-distance product, is commonly chosen as the transmission medium.

Although the plenteous and inexpensive bandwidth of the optical medium holds the potential for new services and capabilities, the ability of a user to access this huge bandwidth is constrained by the much slower electronic processing speed of its channel interface. Fortunately, by employing wavelength division multiplexing (WDM) technology, the vast optical bandwidth of an optical-fiber can be carved up into smaller-capacity channels, each of which can operate at peak electronic processing speed. The network can be configured as a broadcast-and-select network in which all of the inputs from various nodes are combined in a WDM star coupler and the mixed optical information is broadcast to all outputs [1]. Thus, given any physical network topology, the fact that the lasers (transmitters), and the filters (receivers), can be made tunable opens up a multitude of possible virtual network configurations.

Now, given that arbitrary virtual topologies can be realized, which is the best one? In this work we concentrate on multihop and regular structures since these networks allow concurrent transmissions, provide simple routing schemes, and do not require expensive transceivers with fast tuning speeds. All these properties are very desirable for high-speed switching environments. Moreover, ShuffleNet is a widely studied structure ([2-4]) and its performance is comparable to its competitive structures (e.g., de Bruin graph, Manhattan Street Network). Also, for a cost-effective network design, only a small number of transceivers are allowed at each node.

Performance of (unoptimized) ShuffleNets under *non-uniform traffic* is studied in [3]. In [4] adaptive routing schemes have been proposed for improved performance of ShuffleNets under skewed loads. In the present work we study the effect of optimized node placements under different traffic conditions.

Several optimality criteria may be considered depending on the design goals. These include minimizing average hop distance, minimizing maximum load over any link etc. In our present study *minimization of weighted average hop distance* is investigated. Note that this optimization function also minimizes the average packet delay in the network, since in high-speed networks propagation delays are much larger compared to the nodal queuing delays. In general, this optimization problem does not yield to polynomial time solutions (search space for the optimum solution grows exponentially with the number of nodes), so we investigate efficient heuristic algorithms for constructing near-optimal node arrangements in a ShuffleNet configuration.

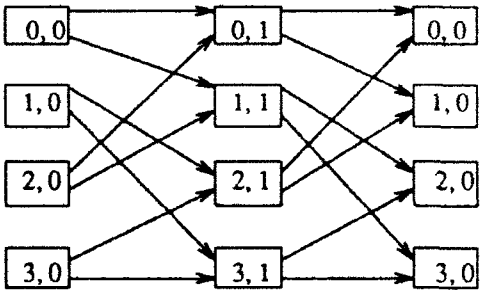


Fig. 1. An 8-Node ShuffleNet.

Consider a (p,k)-ShuffleNet consisting of $N = kp^k$ (k=1, 2, ···; p=1, 2, ···) nodes arranged in k columns with $m = p^k$ nodes in each column. Also assume perfect shuffle connectivity among the adjacent columns. Let the node positions in the ShuffleNet be denoted by ordered pairs (i,j), where, i (i = 0, 1, ···, p^k-1) is the row index and j (j = 0, 1, ···, $k-1$) is the column index. Let $\sigma_{q,r}$ denote the node located at row (q mod m) and column (r mod k). Also, let λ_{ij} be the traffic from the source Node i to the destination Node j and let $\Lambda = \Sigma_{i,j}\,\lambda_{ij}$ be the total load offered to the network.

II. ALGORITHMS

Given below are brief descriptions of three heuristics, first two of which are based on greedy approaches while the third employs an iterative approach. Additional details of these algorithms can be found in [5].

(i) Algorithm LOCAL: This algorithm determines the node connectivity pattern based on the traffic between the nodes of two adjacent columns (stages).

Step 1: Two groups with p nodes in each group are

chosen such that the traffic from one group (say group A) to the other (say group B) is heavy compared to the reverse-flowing traffic from Group B to A. Group A nodes are placed in column 0, and each of these nodes have a link to the nodes in Group B which are placed in column 1.

Step 2: From among the remaining nodes, another $2p$ nodes are chosen and so on until nodes are assigned to all the positions of Columns 0 and 1.

Step 3: The above steps are repeated for placing nodes in Column 2 and so on.

(ii) Algorithm GLOBAL: While assigning a node to a location in ShuffleNet, this algorithm takes in consideration the traffic to (and from) this node from (to) all the nodes that are already placed in the ShuffleNet.

Step 1: Node 0 is placed at (0,0).

Step 2: A penalty function, $P(i,r,c)$ for Node i ($i \in$ unplaced nodes) for position (r,c) ($(r,c) \in$ unassigned locations) is evaluated. Various possibilities for the penalty function exist, see [5]. Penalty function used here is based on the overall weighted hop distance of a candidate node from all the other nodes that are already placed.

Step 3: Node $\hat{i}$ is placed at $(\hat{r}, \hat{c})$ where $P(\hat{i},\hat{r},\hat{c}) = \min\{P(i,r,c)\}$ for all unplaced Nodes i and unassigned locations (r,c).

Step 4: Penalty values of all the unplaced nodes for all the unassigned locations are updated.

Step 5: Steps 3 and 4 are repeated until all the nodes are placed.

(iii) Algorithm ITERATIVE: Consider an $(N-1)$-dimensional surface, composed of points representing the values of our cost-function (i.e. weighted average hop-distance) for all different permutations of $[0, 1, \cdots, N-1]$ with Node i placed at location $\left([\, i \mod p^k \,], \left\lfloor i/p^k \right\rfloor \right)$. Then, this surface will have several local minima and one (or more) global minimum. Our iterative algorithm starts by picking randomly one point $(\sigma_0, \cdots, \sigma_{N-1})$ on this surface. Then, at each iteration, Node σ_k is inserted at the place of Node σ_r ($r < k$; $r = 0, \cdots, N-2$; $k = r+1, \cdots, N$) if the average hop distance in the new arrangement is less than that in the previous one.

In general the Iterative algorithm provides the best solutions but it is also the slowest. Global algorithm also provides good solutions and is the fastest. Performance of Local algorithm is not as good as the other two algorithms. All these algorithms are static, dynamic algorithms which can adjust the network topology in response to the changing traffic patterns are under investigation.

III. NUMERICAL EXAMPLES

Two traffic patterns are considered. The first one is random traffic where λ_{ij} are uniformly distributed random numbers between 0 and 1. In Table 1, the performance of the proposed algorithms (in terms of the flow in the most-congested link after optimization) are compared to that of a random placement algorithm where the nodes are randomly placed in the ShuffleNet.

Next, we consider a database server set-up (Table 2), where two nodes are configured as database servers each serving half of the remaining nodes. Traffic from a node to the database servers is uniformly and randomly distributed between 0 and 1, whereas the traffic from a database server to any node it serves is uniformly and randomly distributed between 0 and 100.

From Tables 1 and 2 we note that even for uniform traffic there is some room for improvement, however, for skewed traffic, performance of ShuffleNets can be significantly improved by optimizing the node placements.

Table 1: Uniformly Distributed *Random* Traffic

N	Random	LOCAL	GLOBAL	ITERATIVE
8	2.00	1.88	1.85	1.84
24	3.25	3.16	3.08	3.11
64	4.63	4.55	4.46	4.52

Table 2: Database Servers-Based *Skewed* Traffic

8	2.05	1.57	1.50	1.32
24	3.26	2.93	2.78	2.45
64	4.63	4.48	4.22	3.82

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TuC1

RECENT ADVANCES IN ULTRASHORT OPTICAL PULSE SHAPING FOR HIGH-SPEED COMMUNICATIONS

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In wavelength-division multiplexed optical communications, the different wavelengths are generally used as independent channels which are modulated separately and independently. The optical phases between the different wavelengths are neither controlled nor exploited, e.g., because the various wavelengths are derived from separate, mutually incoherent sources. However, ultrashort optical pulses in the picosecond and femtosecond range are comprised of a broad bandwidth of mutually phase-locked wavelengths. A 100-fsec pulse at a 1.55-μm wavelength, for example, will have a bandwidth on the order of the 30 nm, equal to the typical gain bandwidth of erbium-doped fiber amplifiers. In recent years we have shown that manipulation of the relative phases and amplitudes of the individual wavelengths allows synthesis of nearly arbitrarily shaped ultrafast optical waveforms[1]. Furthermore, we have pointed out that frequency-domain phase coding of coherent ultrashort pulses could be used as the physical basis for a high-speed code-division multiple-access (CDMA) optical network, in which multiple-access is achieved by assigning different, minimally interfering code sequences to different subscriber pairs[2]. In this talk we will report recent technological advances related to frequency-domain shaping and coding of ultrashort pulses and discuss the potential impact on CDMA networking. In particular, we will discuss holographic processing of ultrashort pulses, which can be used for decoding, matched filtering, and fiber dispersion compensation, as well as the use of acousto-optic tunable filters as integrated pulse coding devices.

Ultrashort pulse CDMA would have several unique attributes. One key point is that individual subscribers would operate at data rates compatible with electronic modulation and processing (<10 Gbit/sec or so). The very wide bandwidth associated with the use of ultrashort pulse would enable optical encoding and decoding (i.e., all-optical processing) to provide asynchronous multiple-access. Compared to WDM, in which a multiplicity of stabilized lasers at different wavelengths are required, all the wavelengths would be provided by a single (mode-locked) laser. Furthermore, in CDMA each data bit carries its own address, and coding provides a measure of security. These functions are usually implemented higher on the protocol stack.

However, several technological issues affect the ability to implement an ultrafast CDMA system. These include the need for compact and reliable ultrashort pulse sources and for low

power optical thresholding devices, as well as the requirement to compensate for fiber dispersion (which will likely limit ultrafast CDMA to relatively short fiber hauls for LANs or MANs) and for rapidly programmable and integrated pulse shapers and encoders. Two recent works, impacting the latter two requirements, are described in the following paragraphs.

First, we have demonstrated holographic processing of ultrashort pulses by using a modified pulse shaping apparatus in which the fixed phase masks used for encoding are replaced with a holographic recording material[3]. By recording the interference fringes between a shaped or coded signal beam and an unshaped femtosecond local oscillator, we have formed spectral holograms of coded pulses. Such spectral holograms serve as matched filters which can decode the incident coded pulses back into intense, bandwidth-limited femtosecond pulses suitable for detection. Furthermore, matched filters generated by spectral holography can be used to compensate for unwanted phase modulations, e.g., due to second or third order fiber dispersion. Third order dispersion compensation was previously demonstrated by using a specially designed phase mask within a pulse shaping apparatus[4]. A potential advantage of the holographic approach is that the required matched filter, either for decoding or for dispersion compensation, is generated automatically in a self-aligned process, so that *a priori* knowledge of the code or fiber dispersion is not required.

To date, shaping, encoding, and decoding of ultrashort pulses have been achieved using bulk optics implementations. In a second set of experiments, we have demonstrated the use of an acousto-optic tunable filter (AOTF) as an integrated pulse shaping device[5]. AOTFs have already received considerable attention as filtering and routing components for WDM networks[6]. The multichannel capability of the AOTF is of particular interest, since this allows simultaneous and independent control of different optical wavelength channels. Our experiments mark the first operation of the AOTF as a multichannel amplitude and *phase* filter to manipulate ultrashort pulses (for WDM applications only amplitude filtering is utilized). At present in our preliminary experiments, the number of independent wavelength channels is significantly less than achieved in bulk-optic pulse shapers. Nevertheless, our experiments do indicate the possibility of integrated ultrashort pulse shaping and coding devices, a development which would significantly enhance the useability of these devices for code-division multiple-access networking.

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TuC2

OPTICAL PROTOCOLS FOR TERABIT NETWORKS

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I. Introduction

Spectral CDMA involves simultaneous encoding across all the modes that make up the spectrum of a coherent, ultrashort pulse. This is usually done in conjunction with some suitable dispersive optical arrangement (*e.g.* using prisms, diffraction gratings) that maps the frequency components of the pulse in the spatial domain. Coding is then performed by introducing phase-shifts between the spectral components (*e.g.* via etch-coded optical phase-delay plates or multi-element phase modulators) before the pulse is reassembled for transmission. As one can easily generate bandwidths in the terahertz range (*i.e.* approaching optical fiber bandwidth limits) using ultrashort pulse sources, it is possible, in principle, to build such systems with aggregate capacities of 100 Gbit/s to Tbit/s. Even more exciting, however, is that the encoding/decoding scheme draws upon traditional technology used in the optical processing/computing field. This basic foundation allows certain boolean operations to be implemented totally in the optical domain, which can then be exploited for executing specific network protocols.

Spectral CDMA was first proposed several years ago by Bellcore, and some basic addressing experiments [1] were carried out in the visible wavelength range without fiber transmission. JPL is currently extending the technique to include optical fiber transmission at the telecommunications wavelength of 1.55 μm, and building a basic optical protocol suite on top of the spectral CDMA system. An all-photonic, source routed network is ultimately envisioned.

II. Optical Protocol Investigation

The network architecture assumes a star topology as shown in Fig. 2 of Ref. 2, with the associated optical encoders/decoders based on active, multi-element modulators (*e.g.* see Ref. 3). Orthogonal, pseudorandom, binary code sequences (*e.g.* *M*-sequences [1]) with high signal-to-noise discrimination are assumed. A node may consist only of a transmitter, or receiver, or both. The following networking protocols will be investigated:

Optical Address Programmability. A practical local area network (LAN) requires that node addresses be changeable. Indeed, here, lies the hallmark of the spectral CDMA scheme where address programmability is achieved naturally without any photon-electron-photon conversion. The speeds required for the multi-element modulator however, which should be commensurate with packet transmission times (< 10 ns), is still demanding by present device technology standards, especially for 1.55 μm wavelength. This powerful feature of dynamic address reconfigurability nevertheless has important bearings on other protocol functions discussed below.

Optical Broadcast. Many packet network administrative operations as well as CATV systems require that one source send simultaneously to many destinations. In the networking scheme described above, this can be established by allocating a unique, networkwide broadcast channel that all nodes can momentarily tune to. Periodic listening or tuning to this unique broadcast channel is then performed to check if there are any oncoming broadcast messages.

Optical Arbitration. Arbitration is responsible for resolving network contention and preventing interference between two sources sending to the same destination. This requires that blocking be setup once two nodes begin communicating. One way to implement this would be for the two nodes to switch to a reserved channel or some address that is unique networkwide before sending and receiving messages. This could be, for example, some convolution of the transmitting and receiving nodes' address codes. Another approach that requires less handshaking may require a second modulator device beyond the first one at the receiver's node that the transmitting node can optically program its address into. Thus, the convolution of the two will mutually exclude any other transmitting stations on the network and interference is prevented only until the second modulator

is cleared. However, this form of first-come, first serve (or statistical) arbitration may not be appropriate for many deterministic networks. In this case, another control channel may be used to periodically rotate access to a given receiver node.

Optical Routing. Another powerful feature of the spectral CDMA scheme is the ease by which address domain mapping may be accomplished. By simply pairing a receiver and transmitter station together, each having different addresses, the spectral components of the optical pulse are realigned by the receiver and are further remapped by the transmitter address. The result is a spectral phase transformation of the signal as it passes from one network domain to another. If all the routing information required can be contained in the spectral domain, then all-optical routing is possible. An interesting aspect of this form of self routing is that it works for packet data as well as streams. Internet-style domain routing may also be possible.

Error Detection and Correction. Phase noise and signal loss of selected (or all) modes can result in bit errors. One level of error detection/correction can be incorporated in the spectral domain by sacrificing modes used normally for addressing with error correction codes (ECC). Such a scheme though will not correct time dependent errors (for which one must use traditional electronic methods).

III. Experimental Testbed Status

An actively mode-locked, fully-integrated, erbium-doped fiber ring laser system was constructed to serve as the ultrashort optical pulse source at 1.55 μm wavelength. Currently, this source gives stable, transform-limited pulses of ~1 ps width, mode-locked at a repetition rate of 50 MHz. Having average output powers of around 3 mW, each pulse has a peak power of ~30 W, which brings it well into the soliton regime. Assuming these are soliton pulses, a pulsewidth of ~1 ps corresponds to a spectral width of ~2.5 nm, or at 1.55 μm, ~310 GHz of bandwidth for coding.

In the first phase of this experimental testbed, fixed, binary, optical phase plates made from etched fused-silica substrates are used as the optical pulse encoder/decoder. Orthogonal, pseudorandom, binary code *M*-sequences [1] are used. A series of diagnostic measurements had been conducted such as basic optical pulse dispersion in fibers and linearity tests in the CDMA encoder assembly. Studies on issues such as throughput, signal discrimination and channel interference etc. will follow. On the theoretical side, the model by Salehi *et al* [2] for this type of network is being improved upon by the addition of a Gaussian-type background noise in the receiving detectors. Effects of optical dispersion will be added later to predict networking distances that can be covered by this scheme. In the second phase of this experimental testbed, a suitable, multi-element, phase-modulator device will replace the fixed phase plate as pulse encoder/decoder. Subsequent investigation of optical networking protocols as discussed above would follow.

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Acknowledgements

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TuC3

COHERENT OPTICAL CDMA WITH INVERSE DECODING IN LADDER NETWORKS

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Fiber optic ladder networks, with impulse responses consisting of $P = 2^n$ pulses, have recently been studied to make coherent optical CDMA networks [1,2]. Conventional 1-channel operation leads to a coherent autocorrelation function, with a peak value of P^2, and sidelobes (the first one having unit amplitude). Here we show theoretically and experimentally that 2-channel operation leads to the elimination of sidelobes, and a peak value of $4P^2$; since this corresponds to the reconstruction of the original pulse, we refer to it as *inverse* decoding.

Figure 1 shows a network consisting of a two-stage encoder and a similar decoder, which can be connected by either fiber (c) or (d), or both. The two networks are matched in the incoherent sense, i.e. their impulse responses have identical pulse spacings. The pulses are only distinguished through their phases. Let ϕ_i represent the relative phase shift going through the ith lower branch. A π phase shift is experienced when going through a 2X2 couple: from upper left to lower right, and no phase shift otherwise. If an impulse is fed into (a), trains of four pulses emerge in fibers (c) and (d); each pulse has a phase reflecting its path, and thus a function of ϕ_1, ϕ_2, and π. Similar considerations apply for the impulse responses of the decoder, when excited by an impulse in either fiber (c) or (d). Assuming that ϕ_1 and ϕ_2 are given, ϕ_3 and ϕ_4 can be chosen to achieve optimum decoding.

Single channel. Consider the case where only one fiber is used to connect encoder to decoder. If (c) is used, and if (e) is the output, then the response of the whole network to an impulse into (a) is the correlation of the impulse response of the encoder from (a) to (c) with that of the decoder from (c) to (e). Optimum decoding (namely autocorrelation) will occur if

$$\phi_3 = \phi_2 + \pi, \quad \phi_4 = \phi_1 + \pi. \tag{1}$$

Likewise it can be shown that the *same* phase conditions would lead to optimum detection at (e) if (d) was used instead of (c). A similar construction exists to find the matched network in the general case of n stages.

Two channels. Consider now that both (c) and (d) are used, with no phase shifts. Paths (c)-(e) and (d)-(e) are simultaneously matched, and their autocorrelation peaks are in phase; these combine coherently into a peak of amplitude $4P^2$. This is the total energy fed into (a): hence all sidelobes cancel out, and all the energy appears as a delta-function in (e). We call this *inverse* decoding; the notion is similar to the result obtained by performing frequency-domain phase (de)coding [3]. We also note that under matched conditions a pulse from (b) would emerge from (f). This offers the possibility of transmitting two bits in parallel: Furthermore, since the matching conditions are independent of the direction of propagation, we could have two bit streams going simultaneously in opposite directions, say from (a) to (e), and from (f) to (b), thus permitting full duplex operation over that link.

The use of separate fibers for (c) and (d) could lead in practice to serious phase stability problems. This could be alleviated by using two orthogonal states of polarization in a polarization-preserving fiber (PPF). Furthermore, the (de)coder networks themselves could also be implemented by replacing the ladder networks by cascaded segments of PPF fibers, rotated by 45 degrees with respect to each other.

We have performed preliminary experiments, with a single-stage coder and decoder, and orthogonal polarizations in a single-fiber link. We have demonstrated inverse decoding, as shown in Fig.2. O_1 corresponds to the output from the matched port (e), and O_2 to the output from (f); both are displayed on a common oscilloscope trace by delaying O_2 by an additional delay line. Under ideal circumstances O_1 would consist of only the central pulse in the first group of three, and all pulses of O_2 would vanish. The departure from this ideal situation is due to experimental difficulties, particularly the lack of phase stability in the (de)coder. Nevertheless, the reasonable agreement with the theoretically expected results indicates that one should be able to accurately obtain inverse decoding with improved equipment.

Coherent coding makes it possible to change addresses by changing phases only. Hence a single easily-modified encoder is needed per station, in contrast to very complex encoding networks for incoherent CDMA. For very short

pulses the encoder could be in integrated optic form, and be very similar to concatenated Mach-Zehnder structures developed for FDMA networks [4]. Interference between multiple users would set an ultimate performance limit; that limit would be similar to that of WDM if very short pulses were used. Such coherent CDMA networks may thus provide an attractive means of implementing high-speed optical multiple access networks, particularly in view of their advantageous security features.

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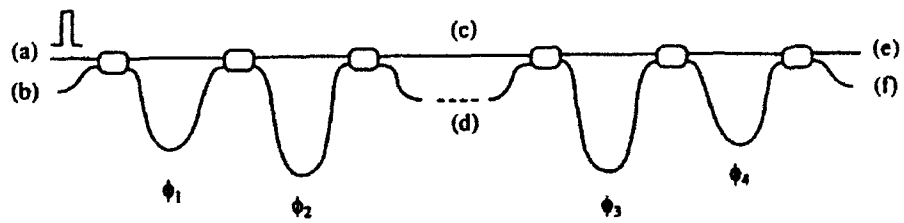


Fig.1. Network formed by a ladder encoder connected to a ladder decoder ($n = 2$).

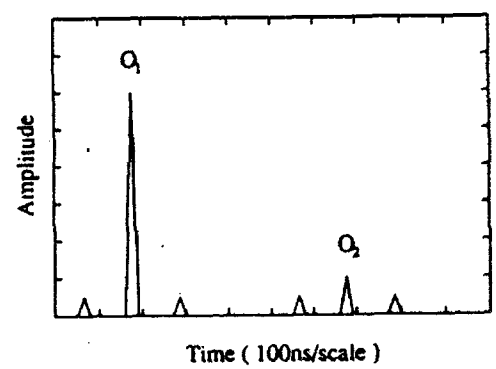


Fig.2. Output pulses of the network of Fig.1, set for inverse decoding.

TuC4

MISUNDERSTOOD ISSUES IN LIGHTWAVE NETWORKING

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Introduction

There appear to me to be some persistent misconceptions on the part of device people about what works in a practical network and on the part of network architecture people about the difficulty of realizing a proposed architecture with practica' devices. This presentation will discuss a number of these misconceptions. I consider myself highly qualified to talk about misconceptions, since almost every one to be mentioned here is one that I have held at one time or another. Most of these are analyzed in Reference [1].

Architecture misunderstandings

- **Present "optical" network directions, such as SONET and ATM will suffice** - These are gigabit-per-network solutions and thus form only a short-term and insufficient base on which to build a gigabit-per-node network future. They are single-wavelength systems that do TDM interleaving of multiple traffic streams. Making the full 25,000- GHz bandwidth and low BER potential of fiber available directly by means of dark fiber provides a better foundation.
- **The traditional layer structure is still valid** - The performance problems associated with maintaining a separation between physical, multiaccess (MAC), logical link, network and transport layers exact too heavy a penalty in a gigabit-per-node networking environment [2].
- **MAC protocol "business-as-usual" will work** - To continue to design MAC protocols that use contention algorithms (e.g. CSMA/CD) in either data channels or signalling channels results in intolerable inefficiencies [3], because of the large ratio of propagation latency to packet duration.
- **Optical logic can be used to decode headers, to buffer messages, etc.** - Components to do these things are sure to be so complex, expensive and difficult to keep in adjustment that this set of options appears impractical for the foreseeable future.
- **Star networks based on space-division are as useful as star-based WDM networks** - Both forms of network solve the *electronic bottleneck* problem in that the per-node bit rate need no longer be on the order of the aggregated bit rate (as with traditional TDM rings and busses), but the space-division option suffers from several disadvantages. It is not as flexible with respect to add-drop-change reconfiguration, protocol transparency, bandwidth-on-demand, and other parameters. It is no accident that PBX-based LANs never really made it compared to the more flexible Ethernets and token rings.
- **The advent of photonic amplifiers makes busses preferable to stars** - This is true as long as only one transmitter is active, but if many are active simultaneously (at different wavelengths), gain saturation effects are so harmful that the star (with a filter before each amplifier) remains a better solution [4].
- **Code-division (spread spectrum) is an attractive option** - TDM is bad enough, in that each bit time is split into N slots, with concommitant increase in sychronization and dispersion difficulties. CDMA compounds this by requiring that each bit time be further subdivided into KN "chips", where K ranges from several tens to hundreds. Also, no energy-efficient CDMA codes are known.

Device misunderstandings

- **Coherent reception is an option for networks** - Coherent may still be an option for long telco links, but with networks (and with fiber-to-the-home too), cost and ease-of-use requirements dominate [5]. The fact that doped-fiber amplifier-based direct detection receivers are dropping

rapidly in cost and can perform as well as coherent receivers (at least for ASK) seems to have settled the argument, in my view.

- **Multi-gigabit device speed is important** - With networks, connectivity and ease of service are much more important than bit rate [6]. Since the components in all-optical networks do not have to handle aggregated bit rates and since it appears unlikely that individual applications running at above one Gb/s will emerge for many years, much of the current emphasis on lasers and photodetectors that run at tens of Gb/s., on solitons, dispersion-shifted fibers, and so forth appears to be irrelevant to networks. Large all-optical WANs will require either some measures against dispersion or all-optical gateways between subnetworks do some pulse reshaping.
- **When you've proved the network in the lab, you're more or less done** - Our experience has been that after basic feasibility has been proved in the lab, less than half the work is done. Getting a real wavelength-acquisition protocol to work, dealing with drift and stability problems in real devices, and providing a practical software interface by which applications can access the network resources consitute at least as large a task.
- **When you've proved a tunability technology in the lab, you're more or less done** - Devices that demonstrate wide tunability often prove to be very difficult to control. Sometimes multiple control signals and discontinuous wavelength-versus-control exacerbate the problem. Dealing with temperature sensitivity, thermal creep, backlash, hysteresis and other factors converts a seemingly straightforward and simple component solution into a complex subsystem.
- **Fast optical tunability is not a bottleneck issue** - Packet switching is a must in computer applications; circuit-switched applications are few. Continuing to do the fast packet switching electronically, as for example with multihop architectures, not only invites the electronic bottleneck but leads to large transit time latencies. Systems in which the optical switching is rapid but must be coordinated over continental distances do not provide a solution either, because of latency.
- **LANs and MANs are sufficient** - Even though 25,000 Ghz is enough for LANs/MANs of up to several thousand nodes, anything less than a complete WAN solution fails to exploit the full potential of all-optical networks. Large scalable WANs require wavelength reuse and the attenuation accumulated by large distances. The latter can be dealt with by photonic amplification (up to a point), but the former requires escaping the restrictions posed by single star or bus geometries. Active wavelength swapping gateway technologies and passive wavelength-routing technologies are required. These should be receiving the same kind of attention that tunable lasers and tunable filters are receiving.
- **The link budget can always be compensated by simply raising the transmitter power level until intermod products due to fiber nonlinearities become excessive** - This overlooks the eye safety problem. Power limits set by current international standards are much more restrictive than those set by nonlinearities.

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TuD1

TRADEOFFS IN THE DESIGN OF MEDIA-ACCESS PROTOCOLS FOR HIGH-SPEED PACKET-SWITCHED BROADCAST MULTICHANNEL NETWORKS*

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ABSTRACT

We summarize the tradeoffs involved in the design of media-access protocols for high-speed, packet-switched, broadcast, multichannel networks between tunability and scalability, processing and number of control channels, network throughput and cost, reservations and delay, and synchronization and support of different traffic classes.

SUMMARY

We consider high-speed, packet-switched, broadcast, multichannel networks where every station's transmission reaches all the stations in the network and the total available bandwidth is partitioned into many communication channels. The primary example of such a network is a fiber-optic wavelength-division-multiplexed (WDM) network, where the transmissions from all the stations are combined and broadcast using a passive optical star and the available bandwidth on the optical fiber is divided into many channels with each channel corresponding to a different wavelength. We assume that all stations need to communicate reliably with all other stations and that every station has only a small number (one or two) of transmitters and receivers. We further assume that the total number of available channels is much smaller than the total number of source-destination pairs. If we then dedicate each channel to a source-destination pair, a station will not be able to transmit directly to all other stations and packets will have to be forwarded by intermediate stations (*multihop*). In a *single-hop* network, all the stations must share the available channels in some co-ordinated fashion, so that they can communicate directly with other stations without going through intermediate stations. This is the function of the medium-access control (MAC) protocol. If the channel sharing is done statically using fixed time-division-multiplexing, then bursty traffic cannot be supported efficiently. In this paper we discuss some of the tradeoffs involved in the design of MAC protocols that allow dynamic sharing of the channels in single-hop networks. We shall arbitrarily use DT-WDMA [3] as an example to illustrate these tradeoffs.

Tunability and scalability: Given the above scenario, either the transmitters or the receivers (or both) must be tunable over (almost) all the available channels in the network. Consider the case where N channels are available, and each station has a receiver that is fixed-tuned to a different one of these N channels and a transmitter that can tune to any of the N channels. In this case, we will have a *collision* when two or more transmitters try to send a packet to the same receiver at the same time. The MAC protocol has to schedule the transmissions so as to avoid collisions or provide a mechanism to recover from collisions. On the other hand, suppose each station has a transmitter that is fixed-tuned to a different one of the N channels and a receiver that can tune to any of the N channels. In this case, when two transmitters send a packet to the same receiver at the same time, the receiver can only receive one of these packets. The MAC protocol has to prevent such *receiver contentions* or recover from them. Note that a contention is different from a collision in that one of the packets involved in the contention can be successfully received whereas all packets involved in a collision are lost. Thus it might appear that it is better to have tunable receivers and fixed-tuned transmitters rather than tunable transmitters and fixed-tuned receivers. However, the situation may be different when one considers how to schedule transmissions. If only the receivers are tunable, there must be a mechanism to apprise a receiver when it must tune to a particular transmitter to receive a packet. Schemes proposed for this purpose (e.g., DT-WDMA) do not, in general, scale well with the number of stations N. Therefore, we conjecture that for large N, having the transmitters fixed-tuned and only the receivers tunable may not be practical.

*This paper is based on work described in [1] and [2].

Processing and number of control channels: Many MAC protocols rely on a separate control channel shared among all the stations (e.g., DT-WDMA). This is used to coordinate transmissions between the stations. However this channel can introduce a *processing* bottleneck because a station has to process information about all the packets in the network all the time and not just the ones it is transmitting and receiving. Having multiple control channels and using them so that each station only processes information relevant to its connections alleviates this bottleneck [1]. Thus in this case, processing power can be traded off against the number of control channels.

Network throughput and cost: Except for static scheduling schemes which are not appropriate for handling bursty traffic, collisions and contentions are unavoidable in any scheme that has only the transmitters or the receivers tunable. Collisions and contentions reduce the network throughput (which measures how efficiently the available bandwidth can be utilized). Therefore, in order to attain a high throughput, some schemes employ a lot of processing (e.g., DT-WDMA), and others use *both* tunable transmitters and tunable receivers; both approaches increase the cost per station.

Reservations and delay: In some MAC protocols, a station has to make a reservation and wait for at least one round-trip delay from the star (in the case of a star network) before it can transmit a packet. This helps in reducing collisions and contentions, leading to a higher throughput, at the cost of greater processing. Other protocols have a feature where a station simply informs the destination that it is transmitting a packet and goes ahead and does so without waiting any further ("tell-and-go", e.g., DT-WDMA). When the traffic is light, collisions and contentions are rare, and tell-and-go schemes have considerably smaller delays than reservation-based schemes. This is a desirable feature in high-speed networks where the round-trip delays are much longer than the packet transmission times.

Synchronization and traffic classes: Almost all the schemes proposed in the literature (including DT-WDMA) are intended to support datagram (connectionless) traffic. We believe it is desirable to support different traffic classes in the MAC layer itself as a means to integrate the MAC and transport layers into a single slim layer. This is the basis of the work in [1], which supports connection-oriented traffic with or without guaranteed bandwidth, as well as connectionless traffic. Providing guaranteed bandwidth enables support of isochronous traffic (traffic requiring delay guarantees like real-time video). It appears that we cannot support isochronous traffic without having network-wide synchronization. Synchronization may be difficult to implement in practice. Also, having network-wide synchronization enables us to use slotted schemes which are, in general, more efficient than unslotted ones.

Many MAC protocols that have been proposed to date are compared using the above metrics in [1, 2].

In the multihop approach mentioned earlier, a packet is retransmitted several times, in general, before it reaches its final destination. Thus the packet delay is increased and the network throughput is reduced by a factor of at least the average number of hops. However, this does not imply that the performance of multihop networks is inferior to that of single-hop networks since in the latter, we have a similar loss in throughput and increase in delay due to contentions and collisions.

More work needs to be done in order to understand these and other tradeoffs more quantitatively. We do not think there is any one protocol that is superior to all others and there is room for improved protocols. Also, fast-tunable transmitters and receivers are not yet available and many implementation issues (e.g., network-wide synchronization) need to be addressed. Ultimately, the protocols that achieve wide-spread acceptance may be those that are implemented early on, as was the case with Ethernet.

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TuD2

PERFORMANCE OF MULTIPLE ACCESS WDM NETWORKS WITH SUBCARRIER CONTROL CHANNELS

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Wavelength division multiplexing is widely recognized as a way to fully exploit the vast bandwidth of the optical fiber. A variety of mutiple access WDM network topologies have been proposed[1]. In any multiple access WDM network a control channel is required to provide the receiving node with information as to which wavelength(s) carry the incoming messages. Many control protocols can be chosen. Typical examples include the use of an independent signalling wavelength shared by all nodes and the use of a tunable filter to scan through the transmitter wavelengths. Use of an independent wavelength will need a second DFB laser at each node for transmitting the control packets. Also, the control channel itself may have to transmit at a very high data rate when the number of nodes increases, causing contentions. One way to avoid these difficulties is to use subcarrier multiplexing (SCM) for control channels. This immediately eliminates the need for a second DFB laser at each node. It can also alleviate the control channel contention problem by channelizing the control packets. By channelizing the control channel packets, the control channel data rate can be kept low, typically in the 10-100 Mb/s range, making it possible to process the control information with low cost silicon technology.

In this paper we analyze the contention problem and network throughput of multiple access WDM networks with SCM control channels. It is assumed that the network has N nodes and that each node transmits on a separate wavelength λ_i with i=1,2,..., N. The network topology is arbitrary. Each node transmits basedband data packets which have an average duration of t_d. Each node has a fixed-wavelength transmitter and a wavelength-tunable receiver. The network control is accomplished by transmitting the control packets on Q subcarriers with frequencies f_i, i=1,2,...,Q. The receiving nodes have fixed-frequency SCM receivers, while the transmitters can transmit at any of the Q subcarrier frequencies. Each subcarrier frequency can be shared by up to q receiving nodes with $1<q<N$. Each message contains a control packet and a data packet. The control packet has a duration of t_c, which is treated as a basic unit, called a time slot. The data packet has a duration of t_d which occupies $r=t_d/t_c$ time slots. We assume that transmission of control packets is a Poisson process. Two types of control networks are considered here: slotted and random-arrival networks. In the former, contentions occur when two or more control packets on the same subcarrier arrive in the same time slot. In the latter, the control packets are allowed to transmit at any time and contentions occur when two or more control packets on same subcarriers arrive within two time slots from one another. In either case, if the receiving node is busy receiving an earlier data packet, the arrving control packet(s) will be turned away. In the following, we analyze the performance of both types of networks.

Case I. Slotted networks: Let G be the average number of total control packets transmitted in a time slot. Assuming that the traffic is equally distributed among the nodes, the throughput of the network can be derived as

$$S = (1+r)G \exp(-G/Q)/[1+rG/N \exp(-G/Q)]. \qquad (1)$$

The maximum throughput occurs at G=Q and is given by

$$S_{max} = N(1+r)Q/(eN+rQ). \qquad (2)$$

For illustration, the throughput for a slotted network with five nodes and five subcarriers is plotted in Fig. 1.

Case II. Random-arrival networks. In this case, the vulnerable period for control packet contention is two time slots. The throughput of the network is given by

$$S= (1+r)G \exp(-2G/Q)/[1+rG/N \exp(-2G/Q)]. \qquad (3)$$

The maximum throughput occurs at G= Q/2 and is given by

$$S_{max} = N(1+r)Q/(2eN+rQ). \qquad (4)$$

For comparison, the throughput of a random-arrival network with five nodes and five subcarriers is shown in Fig. 2.

For long data packets, r >> eN/Q, S_{max} = N for both networks.. For zero data packets (control channels only), S_{max} = Q/e for slotted network and S_{max} = Q/2e for random arrival network, respectively. In this case, if Q=1, the two networks become slotted ALOHA and pure ALOHA networks, respectively. If only data throughput is considered, (1) and (3) are still valid with the factor (1+r) replaced by r.

In summary, we have analyzed the contention problem of multiple access WDM networks with SCM control channels. General expressions for the network throuhghput are derived.

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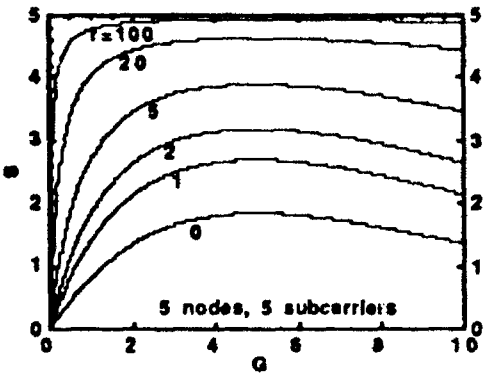


Fig. 1. Throughput of a multiple access WDM slotted network with five nodes and five subcarrier control channels.

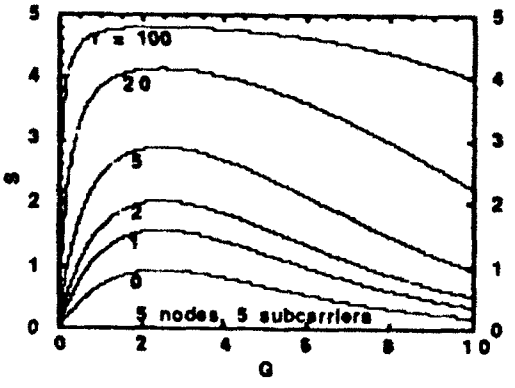


Fig. 2 Throughput of a multiple access WDM random-arrival network with five node and five control channels.

TuD3 HIGH-CAPACITY PACKET-SWITCHED (ATM) WDM NETWORKS WITH TUNABLE LASERS AND SPATIAL REUSE OF WAVELENGTHS

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Recent device breakthroughs have brought about lasers discretely tunable to sixteen frequencies regularly spaced over a range of 650 GHz (around a wavelength of 1.53 μm) with very fast tuning times (under 10 ns) [1]. Therefore, an important question is how such fast tunable devices should be used in distributed packet-switched lightwave networks (e.g., LANs and MANs). We address this question by illustrating a WDM network architecture that uses fast tunable lasers to provide dynamic connectivities among nodes, eliminate internal network congestion, and minimize the average number of hops from packet sources to destinations. For illustration, we focus on WDM ring topologies, although the architectural concepts also apply to bus, tree, star, and other topologies.

Wavelength-division multiplexing (WDM) is a technique that allows many nodes to transmit simultaneously on different wavelength channels, thereby achieving network concurrency and yielding substantially larger throughput than the electro-optic transmission bottleneck. In this proposal, we partition a LAN or MAN into a number of subnetworks, creating, for example, a multi-ring network, with each node assigned to receive packets (or ATM cells) from only one (or, in general, a small number) of the subnetworks. But since all the subnetworks are wavelength-division multiplexed onto an optical fiber, each node can access every subnetwork by appropriately tuning its transmitter. Specifically, in a multi-ring configuration, each node can tune its transmitter such that it sends a packet over the correct subnetwork (i.e., ring) to reach its destination. The packet circulates around the ring until it reaches its destination, without the need for store-and-forward buffers. This may be the main advantage of tunability: the simplification of network access and flow control. Once a packet enters the network, it doesn't encounter internal congestion.

Before we describe this specific multi-ring network in further detail, note that this partitioning into subnetworks, in general, enables nodes to use either fast- or slow-tuning lasers. Of course, nodes that pay for faster-tuning lasers can sustain higher throughputs since they will waste less time retuning their lasers between successive packet transmissions. In addition, fast-tuning lasers (tuning from one channel to another in at most a few nanoseconds) will enable gigabit-per-second ATM switching. Finally, if traffic patterns change with time, note that the network can be re-partitioned into different subnetworks if the nodes are equipped with (slowly-) tunable receivers.

Figure 1 shows a fault-tolerant example configuration, referred to as a dual ring-shaped passive bus, in which nodes access two optical fiber loops via passive taps. One closed circular loop of fiber is used for transmissions in the clockwise direction and the other is used for counterclockwise transmissions. Multiple subnetworks (rings) are wavelength-division multiplexed on the fibers. Each node has one wavelength-insensitive passive tap (per fiber), which is used for both a tunable transmitter and a fixed-wavelength receiver. The passive taps attenuate the optical signal and thus allow reuse of the same wavelength in various

nonoverlapping portions of the fiber [2]. This wavelength reuse is important because WDM technology is currently limited to perhaps tens of wavelength channels on a fiber, far short of the thousands theoretically available. In addition, spatial reuse of WDM channels allows the achievable network capacity to be greater than the number of wavelengths times the transmission bit rate.

Figure 2 shows a block diagram of a network interface unit. For each fiber, a node has a tunable transmitter, a fixed-frequency (F_B) transmitter, and a fixed-frequency (F_A) receiver. The FIFO in Fig. 2 stores network packets that happen to arrive while the tunable transmitter uses frequency F_B. When the tunable transmitter uses other frequencies, the fixed-frequency transmitter can simultaneously use F_B. Note that a frequency conversion (e.g., from F_A to F_B) occurs at the regenerator (regenerators are needed to support an arbitrary number of nodes). This frequency conversion prevents the fixed-frequency transmitter from interfering with the receiver (recall that a single passive tap is used for both the transmitter and the receiver). Consequently, each subnetwork (i.e., ring) is formed by point-to-point links between nodes, with different frequencies used for successive links of the subnetwork. Naturally, frequencies can be used in multiple subnetworks and can also be reused within a subnetwork.

In this general network architecture, many possible access protocols can be used by the subnetworks; different subnetworks can even use different protocols. Furthermore, each subnetwork can have its own signal formats and transmission rates. Although many network topologies are possible, the sequential ordering of nodes around a ring can simplify the access protocol. One example we discuss in this presentation is a buffer insertion protocol with a reservation scheme that provides fair access to the time slots, and a tunable "activity detector" that informs a node when a particular subnetwork is idle.

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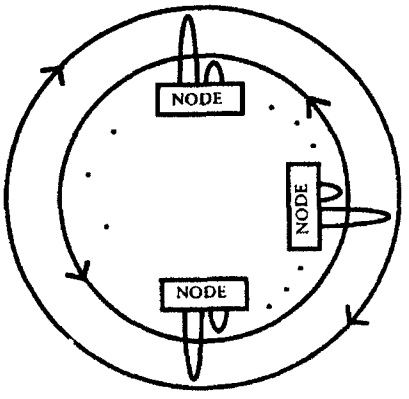


FIG. 1 A DUAL RING-SHAPED PASSIVE BUS WITH MULTIPLE WDM SUBNETWORKS

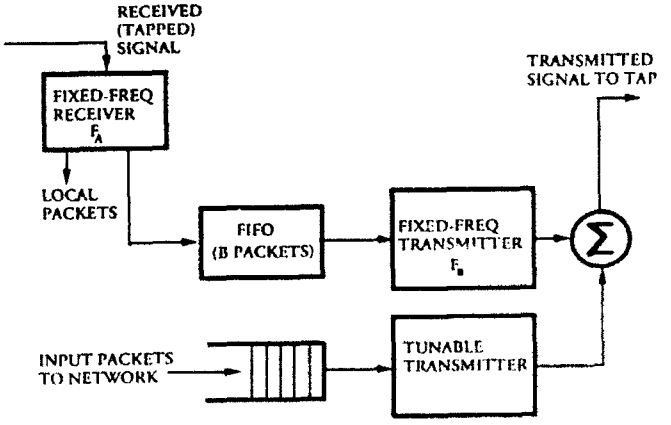


FIG. 2 NETWORK INTERFACE UNIT

Wednesday

August 5, 1992

WA: Optical Network Components

WB: Single-Hop Networks

WA1 ULTRAFAST LOGIC GATES IN A SOLITON RING NETWORK

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We describe the application of ultrafast, all-optical logic gates to a soliton-based local- or metropolitan-area-network. The slotted ring network serves a few hundred users and uses self routing packet switching with a 100 Gbps peak data rate and a 1.25 GHz packet rate. This is a "light-pipe" system where the data remains in optical format throughout the network, converting to electronics only at the host and destination nodes. The packets have an eight-bit address, 32-bit payload and two bits for synchronization and network management. The packet address is selected and decoded using recently demonstrated soliton-dragging and -trapping logic gates, which are long latency, ultrafast fiber devices that satisfy all cascadability and logic requirements for a digital optical processor. A ring network is one potential application of these logic devices that requires only a handful of gates per node.

The hierarchical network is a slotted ring with up to 254 user access nodes. In this straw man example we select a trivial protocol: 1) if *ForMe* then remove packet and replace with empty packet; or, 2) if *Empty* and packet queued in buffer, then replace the empty packet with the new packet. The design focuses on the network access nodes (Fig. 1), where ultrafast gates are used to decode the header, which has the same physical format as the data. The code matching logic module operates at the bit-rate and checks if the header matches the local address or corresponds to an empty packet. The outputs from this module are electronic signals that control a network of routing switches. The delay in the upper arm compensates for the latency in the logic module. The exchange/bypass network routes the incoming packet or a new packet, operates at the packet rate, and can be reconfigured in the time guard band between packets. When the packet reaches its destination, it is demultiplexed or bit-rate down-converted to speeds accessible by electronic shift registers. An optical phase-lock loop is used to synchronize the local clock to the ring data, and erbium-doped fiber amplifiers are used to compensate for the insertion and splitter losses.

Block diagrams of the code-matching logic modules and the exchange/bypass network are shown in Fig. 2. The first gate of the code-matching logic module removes the header from the packet and performs logic-level and timing restoration. The resulting signal is duplicated and forwarded to two separate selection circuits. The upper AND-gate detects if the packet is empty: an empty packet is assigned an all one header to maintain clock synchronization. The lower circuit, which consists of an XOR-gate and another AND-gate, detects if the packet should be read. We select the logic functionality for both circuits so that the desired output signal occurs only when all eight-bit outputs are zero, making it simpler to set the threshold.

The exchange/bypass network routes the packet depending on the signals from the code-matching logic module. If READ is true, then the optical exchange/bypass network routes the incoming packet to the bit-rate down converter and switches an empty packet on-line. If the EMPTY and QUEUE bits are both on, the empty packet is replaced with the new packet. Only one input to each routing switch is used to avoid cross-talk.

By using bit-rate switches and guaranteeing bit-level synchronization, we can implement a "logic tuner" rather than a physical tuner (as in wavelength division multiplexing). For example, the frequency filter in a wavelength system is replaced by the local node address, and we transmit to different users by different codings of the header. A "logic tuner" may be advantageous for implementing digital systems with broadcast capability where every node consists of identical hardware.

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[2] J.R. Sauer is with the University of Colorado, Boulder, CO.

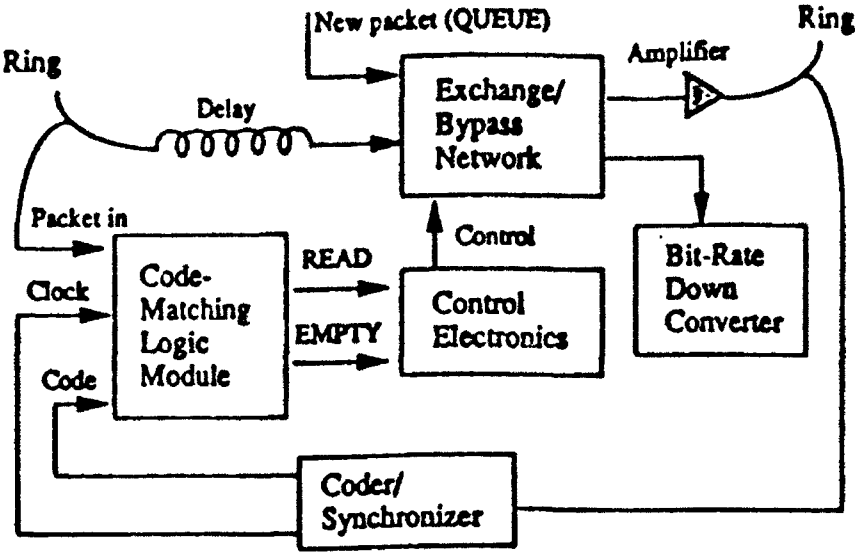


Figure 1. Schematic of a network access node in a soliton ring network.

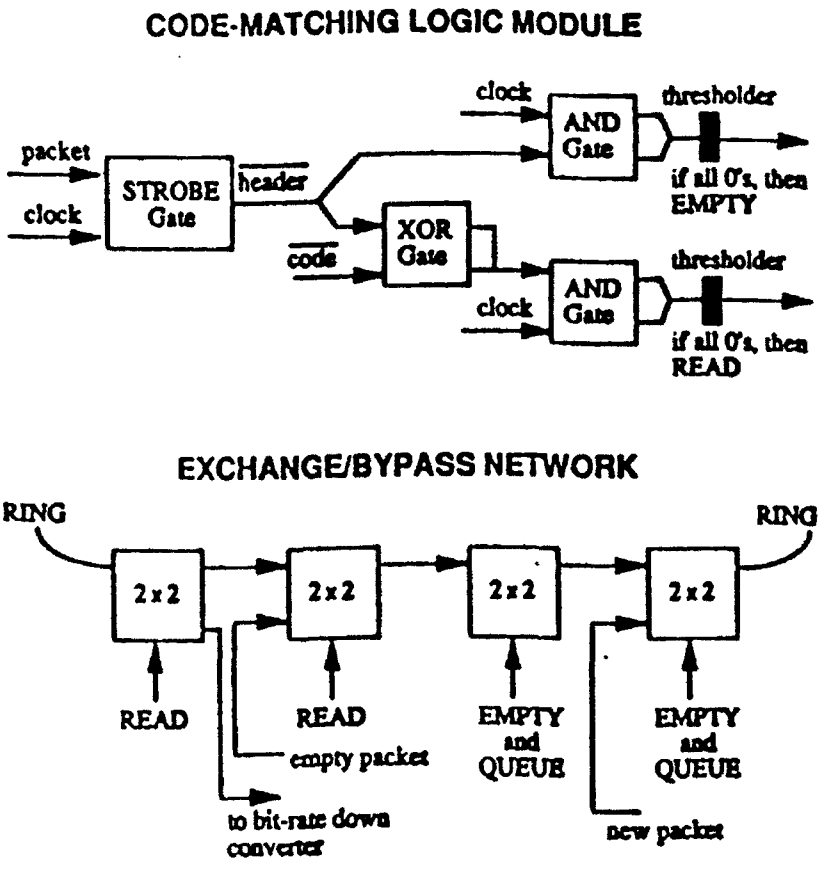


Figure 2. Block diagrams of the code-matching logic module and the exchange bypass network. The code matching logic contains the ultrafast soliton gates, while the exchange/bypass network consists of slower electro-optic switches.

WA2 SELF-PULSATING LASER DIODES AS TUNABLE TRANSMITTERS FOR SUBCARRIER MULTIPLE-ACCESS NETWORKS

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Subcarrier Frequency-Division Multiple Access (SFDMA) offers a simple, low-cost alternative for providing multiple access to a relatively small number of users ($\leq$30) at moderate bit rates ($\leq$100 Mb/s). In this paper, we study the FM characteristics of a compact-disk, self-pulsating laser diode (SP-LD). The high-speed dynamics of the intensity pulsations is examined in detail, and the self-pulsating frequency *itself* is used as a microwave subcarrier for transmitting digital information. We show that 800 Mb/s microwave FSK is possible, and assess the feasibility of employing SP-LDs as fast tunable FSK transmitters in local-area, SFDMA networks.

The FM response of the self-pulsation is first characterized using the set-up in Figure 1. A Sharp LTO22MC compact-disc, multimode, SP-LD emitting at 780 nm was used. The self-pulsating frequency (in MHz) vs. bias current follows $f_{sp} \approx k_f(I_{dc} - I_{th})+500$, where k_f = 80 MHz/mA and I_{th} = 47 mA. For the measurements, the laser was biased for a self-pulsating frequency of 3 GHz with a linewidth of 4.5 MHz. A swept-frequency sinusoid from port 1 of the network analyzer was then applied on top of I_{dc}, modulating the self-pulsating frequency. The results are shown in Figure 2. The FM bandwidth of the self-pulsation is $\sim$ 700 MHz over a large range of source powers.

The system illustrated in Figure 1 was also used to transmit FSK data. A 500 Mb/s ($2^{15} - 1$) NRZ psuedorandom bit stream was applied to the SP-LD. The peak-to-peak amplitude of the pulses was set at 750 mV, for a Δf_{sp} of 500 MHz and an FM index $\beta = \Delta f_{sp}/B = 1$, where B is the bit rate. The measured bit-error-rate vs. carrier-to-noise ratio is plotted in Figure 3. Figure 4 depicts the optical power penalty incurred at various bit rates (as compared to 500 Mb/s), while maintaining an error ratio of 10^{-9}. For an additional 1-2 dB of optical power, FSK at 800 Mb/s is possible at a reduced FM index. An error-rate floor of 10^{-3} appears at 900 Mb/s due to the finite FM bandwidth of the self-pulsation, while the lower end is limited to $\sim$125 Mb/s by the finite linewidth of the self-pulsation. The latter can be eliminated by using a higher FM index, which should permit operation at bit rates down to 10 Mb/s.

One method of providing multiple-access is illustrated in Figure 5. Each user has autonomous access to a tunable transmitter and a fixed receiver. The receiver contains a microwave bandpass filter with a center frequency corresponding to the users address. Data is transmitted in packets by first tuning the self-pulsating frequency to an RF frequency corresponding to a user's address. Packects of data subsequently FSK modulate the laser about that RF frequency. Using the above experimental results, we project that 20 to 30 users at 10 Mb/s/user can be accommodated. Alternatively, 4 at 100 Mb/s/user is possible. The number of users is limited by the self-pulsating frequency range of the laser. Operation is further limited to an octave within this range (2-4 GHz in our case) to avoid interference from the higher order harmonics of the self-pulsation. Lasers have been fabricated to self-pulsate over a wider range (e.g. 1-10 GHz) [1]. This can more than double the number of users at higher bit rates. Optical beat interference should not limit the number of users since it is not observed with low-coherence, SP-LDs [2].

The proposed architecture takes advantage of the simplicity of FSK discriminator detection compared to coherent BPSK or QPSK [2]. The need for a microwave local oscillator is also eliminated. In addition, it does not have to contend with synchronization problems inherent in TDMA systems. The entire modulator can be built with potentially very-low-cost commercially available products, and realized on a circuit board typically found in personal computers.

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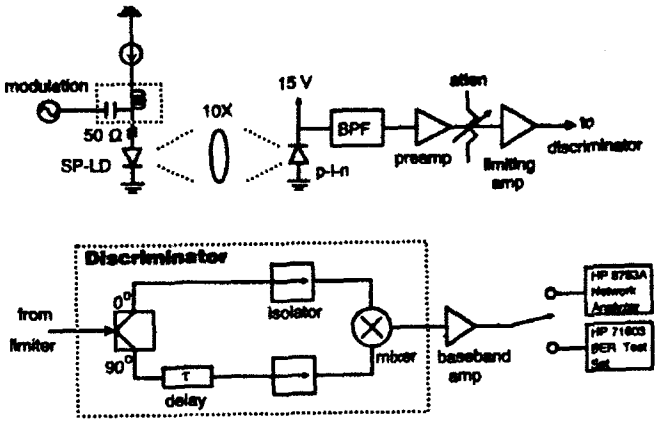


Figure 1. Set-up used to measure the modulation response of the self-pulsating frequency and to send FSK data.

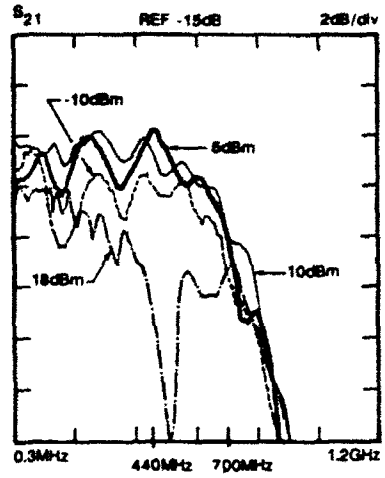


Figure 2. Modulation response of the self-pulsating frequency at various drive powers.

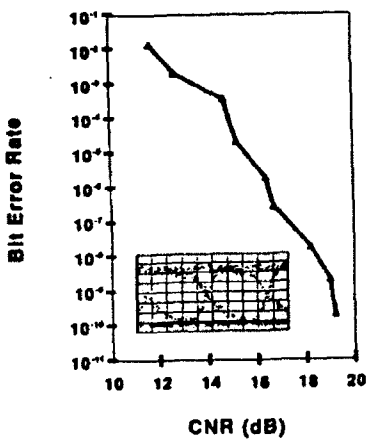


Figure 3. BER vs. CNR for FSK data transmitted at 500 Mb/s. A CNR of 19 dB is required to maintain a 10^{-9} error rate. Inset shows the eye-diagram at 500 Mb/s.

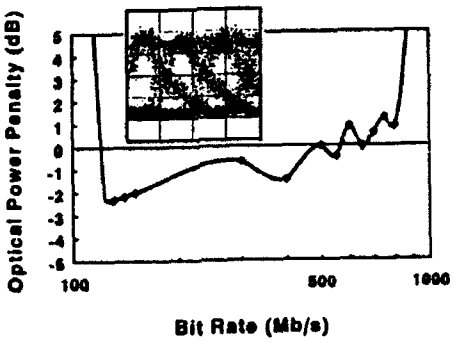


Figure 4. Power penalty. Inset shows eye diagram for 800 Mb/s.

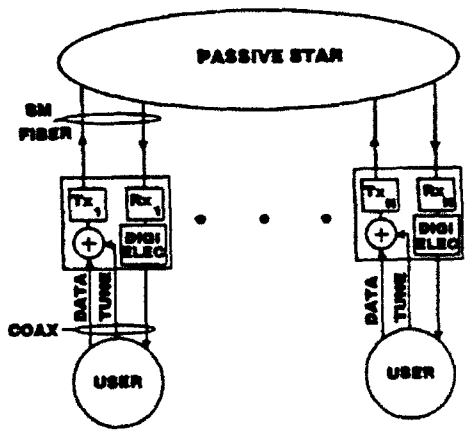


Figure 5. Block diagram of the subcarrier packet network.

WA3

ANALYSIS OF TUNABILITY AND SPECTRAL PURITY FOR TUNABLE SEMICONDUCTOR LASERS USING GRATING-ASSISTED CODIRECTIONAL-COUPLER FILTER

by
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Summary

Recently monolithic tunable semiconductor lasers incorporating filters with very wide wavelength tuning ability have been under intensive investigation[1-4]. This is motivated mainly by the increasing demand on high capacity data transmission in optical fiber communication. Wavelength division multiple access (WDMA) using tunable lasers and/or receivers are promising to utilize the tremendous optical bandwidth of the fiber and achieve high data transmission capacity. Present tunable lasers using Distributed-Bragg-Reflectors(DBR) have maximum relative tuning range, $\Delta\lambda/\lambda < \Delta n_{eff}/n_{eff}$[5], the relative effective index change, and this is limited to below 1%. Alferness et al. demonstrated an integrated vertical codirectional-coupler filter in InGaAsP/InP and proposed a much wider wavelength tunability[1] with the grating-assisted codirectional-coupling(GACC) as compared to that of a contradirectionally coupled DBR filter. They have also demonstrated recently a tunable laser that used the GACC filter as an intracavity filter which tuned over 57 nm around 1.5μm[2].

This paper addresses the inherit problem of relatively poor spectral purity when using GACC filters as an intracavity filter in a laser structure. In a GACC structure, two waveguide modes with different propagation constants, β_1 and β_2, propagate codirectionally. The two modes are coupled with the assistance of a longitudinally corrugated grating to provide the wavelength selectivity. The filter center is determined by the phase matching condition

$$\beta_1 - \beta_1 = K, \tag{1}$$

where $K=\Lambda/2\pi$ is the wave vector of the fundamental harmonic of the first order grating and Λ is the period of the grating. Because the two waveguide modes are spatially separated, it is pratically possible to change propagation constant of one of the waveguide modes by changing its effective refractive index via electrooptic or carrier injection effects. If the index changes are the same for the DBR and the GACC filters, we find that the wavelength tuning is improved by a factor of

$$F = \frac{n_g}{n_{g1} - n_{g2}}, \tag{2}$$

where n_g is the group index of the waveguide mode of the DBR filter and n_{gi} are the group indexes for the two waveguide modes in the coupler filter. For a design with a small value of n_{g1}-n_{g2}, a great improvement in tunability can be achieved. However, as the tunability is widened, the filter bandwidth is broadened at the same time. The normalized FWHM filter bandwidth is found to be

$$\frac{\Delta\lambda_{1/2}L}{\lambda_0^2} = 0.8\frac{F}{n_g}, \tag{3}$$

where L the filter length. Assuming the total cavity length of the laser is L_T after incorporating the GACC filter as an intracavity filter, we found that the mode suppression ratio (MSR) of the laser is

$$MSR \approx \delta\left(\frac{1}{F}\frac{L}{L_T}\right)^2, \tag{4}$$

the prefactor $\delta \sim 1\text{x}10^4$ for typical laser parameters. Figure 1 plots the MSR and the FWHM bandwidth VS the tuning improvement factor F. It shows the critical tradeoff between tunability

and spectral purity. Note the difficulty in obtaining large MSRs in widely tunable lasers. The minimum value of F is limited by the group index difference of the two waveguide modes that can be obtained. Figure 2 shows a generic twin-guide structure using a separate-confinement-heterostructure single quantum well for the active guide and a bulk phase shifter for the passive guide. Figure 3 plots the design curves based on this generic structure using the device parameters listed in Table I. Limitation on the achievable F and the corresponding device performances will be discussed, namely, the threshold current of the laser and the efficiency of wavelength tuning.

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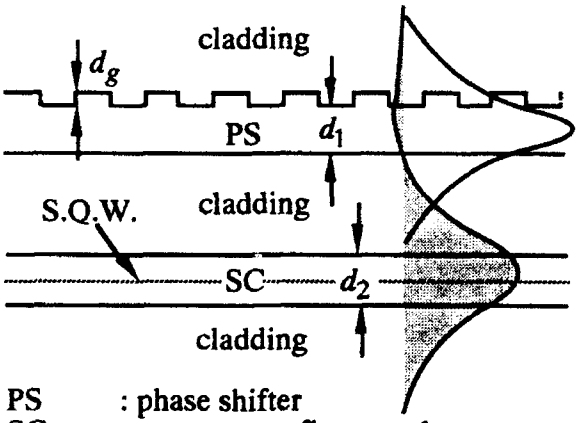


Figure 2

Table 1. Device parameters of the twin-guide structure for the GACC tunable laser.

Parameter	GaAs/AlGaAs	InGaAsP/InP
λ	0.98 μm	1.55 μm
S.Q.W.	$In_{.2}Ga_{.8}As$	$In_{0.52}Ga_{0.48}As$
Cladding	$Al_{.6}Ga_{.4}As$	InP
PS	GaAs	InGaAsP (1.3 μm)
SC	I: $Al_{.4}Ga_{.6}As$	IV: InGaAsP (1.1 μm)
	II: $Al_{.3}Ga_{.7}As$	V: InGaAsP (1.2 μm)
	III: $Al_{.2}Ga_{.8}As$	
d_2	0.2 μm	0.2μm
d_g	0.1 μm	0.1μm
coupler length	500 μm	500 μm

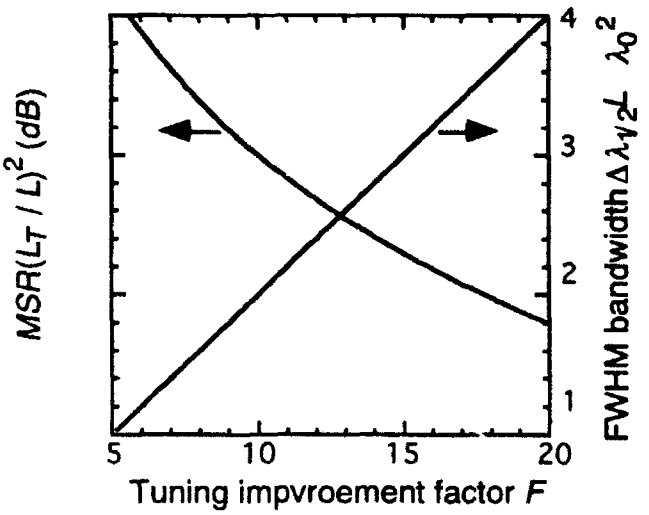


Figure 1

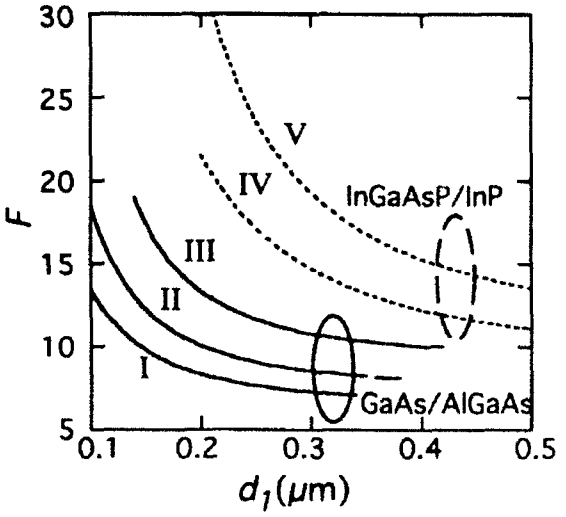


Figure 3

WA4

SYNCHRONOUS OPTICAL NETWORK APPLICATIONS USING MODELOCKED SEMICONDUCTOR DIODE LASERS

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In this summary, we show that hybrid modelocked semiconductor laser systems are attractive sources of low jitter optical pulses, and can provide optical timing information, with varying amounts of residual timing jitter depending on the synchronization method used.

Three techniques have been used to provide multi-port synchronous optical timing signals. The first method (Fig. 1(a)) relies on splitting a single modelocked optical pulse train and distributing this signal to the individual ports. This has the advantage that port to port jitter is only influenced by the random variations of the transmission path lengths and is unaffected by the jitter in the pulse generation process. The second technique (Fig. 2(a)) uses a single coherent electrical signal to drive independent modelocked oscillators which directly lends itself to multiwavelength applications. The third technique uses optical injection of one hybrid modelocked laser to synchronize a separate passive modelocked laser, in a master-slave configuration. An advantage of this technique is that large phase changes in the master laser are tracked by the slave laser.

The external cavity hybrid modelocked semiconductor diode laser systems are constructed from AlGaAs angle striped traveling wave optical amplifiers [1,2]. These laser systems are comprised of three main components; a low power hybrid modelocked master oscillator, a high power single pass semiconductor traveling wave optical amplifier and a grating compensator for pulse compression. The wavelength and duration of the pulses generated from these laser systems are 830 nm and ~ 500 fsec, respectively, with ~ 10-12 mW of average output power.

In the first method, only one laser system is used. The optical pulse train produced by this system was distributed to 1024 port using an optical fiber splitter. The pulse train was detected and amplified using a commercial receiver, and then used to drive a divide-by-two ECL logic circuit to generate a square wave clocking signal. The jitter on the modelocked laser was initially measured to determine the lower limit of the relative timing jitter and was determined to be ~ 0.5 psec. In order to determine the relative timing jitter between ports, a correlation experiment is performed. Two output signals from the detectors are combined in a microwave mixer. The relative time of arrival of the two signals are adjusted so that a peak in the correlation signal is obtained. The relative delay between the two signals are then adjusted so that the height of the correlation peak is a sensitive function of the relative delay between the two inputs. Under these circumstances, a correlation jitter sensitivity of 0.6 psec/mV was obtained. Using a max-min excursion feature of a sampling oscilloscope the total dynamic clock jitter between the two ports was measured to be ~ 12 psec over measurement periods of 1 hour (Fig. 1(b)).

The results of the experiment using the second method are summarized in Fig. 2(b). Two laser systems are synchronized to the same repetition rate by an R. F. synthesizer operating at a frequency of 335.48 MHz. The resultant timing jitter is determined by sending both pulse trains into a rotating mirror optical correlator with a small (~ 10 psec) fixed time delay τ_d separating the combined pulse trains. Variations in the cross-correlation FWHM and peak position give information about the relative variations in time delay τ_d. The displayed signal shows the correlation of a two pulse input signal, giving the expected three peaked signal shown in the figure. The

center peak is the sum of the autocorrelation functions of the individual input laser pulses. The sidelobes are the cross-correlation signals of laser system 1 with laser system 2. This cross-correlation signal shows a FWHM of ~ 3 picoseconds where the measurement has been averaged over a 2 second interval. Since both optical pulse trains are composed of pulses with temporal durations of less than a picosecond, the sidelobe widths, being ~ 3 psec are dominated by the relative timing variation separating the pulse pairs. An important result from this experiment shows that synchronization on a picosecond time scale can be achieved without the use of sophisticated control loops.

The third method is used for synchronizing a master hybrid modelocked laser with a slave passive modelocked laser. This requires an injection seed pulse from the master laser into the slave laser. Both the master and slave lasers must have similar spectral characteristics. The free running slave laser shows considerable phase noise sidebands associated with pulse to pulse timing jitter which is characteristic of passive modelocked lasers (Fig. 3(a)). With ~ 100 μW of optically injected power from the master laser into the slave laser, the optical pulses became synchronized with master laser, as observed on the sampling oscilloscope and by the elimination of the phase noise sidebands of the slave laser (Fig. 3(b)). The resultant pulse to pulse timing jitter on the slave laser was measured to be ~ 5 psec.

In summary, three methods of utilizing hybrid modelocked external cavity semiconductor lasers for providing synchronous timing information to several independent ports have been demonstrated, with differing amounts of timing jitter. These experimental results are the first to out knowledge of synchronized high power subpicosecond diode lasers.

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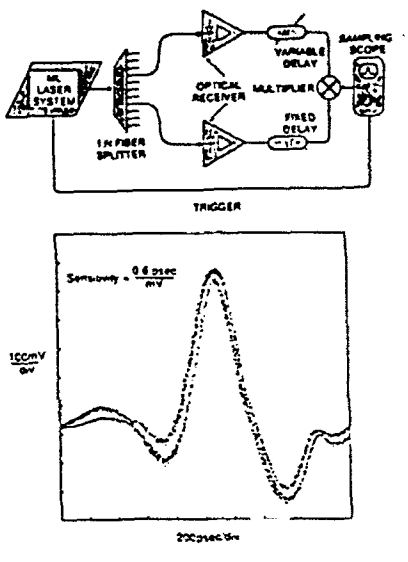


Fig. 1:
(a) Clock distribution technique,
(b) correlated jitter measurement.

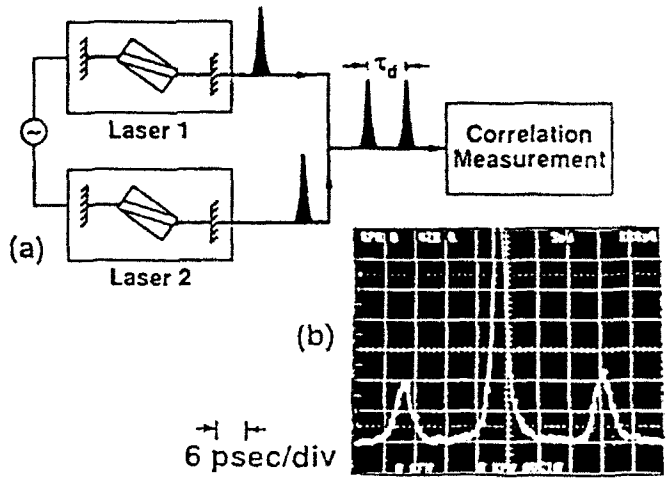


Fig. 2:
(a) Clock synchronization technique,
(b) correlated jitter measurement.

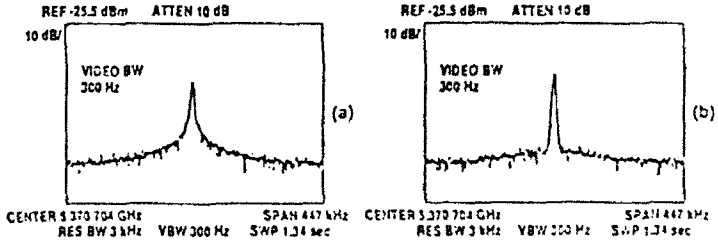


Fig. 3:
(a) Free running clock,
(b) synchronized clock.

WB1

A SCALABLE RESERVATION-BASED SINGLE-HOP WDM LIGHTWAVE NETWORK

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Summary

We propose a single-hop WDM lightwave network which is scalable and is capable of supporting both packet-switched and circuit-switched communications. The network employs a passive star coupler (PSC) connecting all nodes with two-way fibers. A separate channel is dedicated as control channel (CC) and the rest of the channels are used as data channels. Each node's network interface unit (NIU) has one fixed transmitter (FT) and one fixed receiver (FR) (called control transmitter and control receiver, respectively) which can only access the control channel. In addition, each NIU is also equipped with one tunable transmitter (TT) and one tunable receiver (TR) (called data transmitter and data receiver, respectively) which can be tuned over all of the data channels. Following the notations introduced in [1], such a system is called CC-FTTT-FRTR. Single-hop communication is achieved by tuning the sending node's data transmitter and the receiving node's data receiver to the same data channel for the packet transmission duration, and the coordination is done through control packets transmitted over the control channel. A control packet consists of source address, destination address and number of data packets to be transmitted. Length of a control packet is normalized to be unity (one slot) and time is divided into slots synchronized across all channels.

Unlike the TDMA scheme used to access the control channel in [2, 3, 4, 5], slotted-ALOHA protocol is employed to access the control channel in our protocol to accommodate system scalability. Upon arrival of a control packet, every node executes a reservation protocol which selects a proper data channel and schedules data packet transmissions on that data channel. Since multiple data packets can be scheduled with a single control packet transmission, the pre-transmission coordination overhead for long messages (containing mutiple packets) is reduced and circuit-switched service can be supported. Various scheduling mechanisms can be developed to incorporate different service requirements. In a high-speed network, little processing time is allowed at each node. Thus, we propose a simple reservation protocol based on the earliest available time of data channels and of destination nodes (denoted as the EATS algorithm).

Let the tuning time for data transceivers be T slots and the length of a data packet be L slots. There are M network nodes and N data channels. τ_i (i=1,2,...,M) is the distance between node i and the passive star coupler (PSC) and is measured by the channel propagation delay in number of slots. Assume all of the τ_i are known to all of the nodes. The protocol requires that each node maintain the following data structures:

- **Channel Available Time (CAT).** CAT[i] is the time that channel i will be available, i.e., channel i has been reserved until CAT[i]-1, i=1,2,...,N.
- **Receiver Available Time (RAT).** RAT[j] is the earliest available time for scheduling a new data reception at node j, j=1,2,...,M.
- **Local Receiver Scheduling Queue (LRSQ).** LRSQ stores scheduling information for receiving data packets which are directed to the local node. Each element in LRSQ contains source address, data channel number, scheduled receiving time and number of packets to receive, and these elements are stored in FIFO order.
- **Local Transmission Queue (LTQ).** All data packets generated by the local user are first put into LTQ and will be transmitted in order of arrivals. Each element in LTQ consists of destination address, number of data packets, and the data packets themselves.

To describe the EATS algorithm, let a control packet from node s to node d be received by node i at time t_c, and let the control packet request the transmission of m data packets. The earliest available time for node d to receive is

$$t_r = max(t_c + \tau_d - \tau_i, RAT[d])$$

The earliest time the source node s can transmit is

$$t_s = t_c + \tau_s - \tau_i$$

Due to the propagation delay from node s to node d, node s can transmit $\tau_s + \tau_d$ slots ahead of the time node d is ready to receive, so the earliest time to transmit is

$$t = max(t_s, t_r - \tau_s - \tau_d)$$

A data channel w is selected, which satisfies

$$CAT[w] = min(CAT[j], 1 \leq j \leq N)$$

so that w is the earliest available data channel to schedule this transmission. Therefore, the final scheduled time for node s to transmit is

$$t_1 = max(t, CAT[w] - \tau_s + 1)$$

The receiving time for node d should be

$$t_2 = t_1 + \tau_s + \tau_d$$

A node updates its RAT[d] as

$$RAT[d] = t_2 + T + L + (m-1) * L = t_2 + T + m * L$$

and it updates its CAT[w] as

$$CAT[w] = t_1 + T + m * L + \tau_s$$

If $d = i$, i.e., the packet is directed to the local node, an entry is created with source address, data channel number, scheduled receiving time (t_2) and number of packets to receive, and is inserted at the end of node i's LRSQ. The control packet will eventually be received by all nodes. Since all nodes execute this algorithm when they receive the control packet, the contents of RAT and CAT will be consistent across all nodes.

The throughput analysis is easy to conduct, which is mainly determined by the throughput on the control channel accessed via the slotted-ALOHA scheme. Although the maximum control channel throughput under slotted-ALOHA is 0.36 control packets per slot, we expect that higher throughput on data channels can be achieved since the length of a control packet is very short when compared with the length of a data packet and multiple data packets can be scheduled using a single control packet. Further research on this system includes analysis of packet delay and comparisons of alternative scheduling schemes with the EATS algorithm. We will report on these results at the conference.

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WB2

PERFORMANCE IMPACT OF SWITCHING LATENCY ON PRE-ALLOCATION PROTOCOLS FOR WDM STAR-COUPLED NETWORKS

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Summary

This paper studies the performance impact of the switching latency of the wavelength tunable devices on preallocation protocols for WDM star-coupled networks. *Preallocation* protocols are designed for WDM star-coupled networks with data channels pre-assigned to the nodes in the system. The data channels could be pre-assigned to the nodes for data packet transmission (a fixed transmitter and a tunable receiver) or for data packet reception (a tunable transmitter and a fixed receiver). Pre-allocation eliminates the requirement that a node possess both a tunable transmitter and a tunable receiver.

The preallocation protocols considered in this paper are designed for a system with channels pre-assigned for data packet reception. A source node tunes its transmitter to the home channel of the destination node and transmits according to the media access protocol. Each node receives traffic directed to it on its home channel. A home channel may be shared if the number of nodes exceeds the number of channels in the system. *Optical self-routing* where a node only receives traffic destined to it in a multi-access environment may result when the number of nodes equals the number of channels. Access arbitration on the data channels is based on **random access** and **static allocation**. Any node in the system can determine the home channel of any other node in a decentralized fashion with knowledge of the destination node number and the total number of nodes and channels in the system [1, 2, 3].

Pre-allocation approaches appear to be very promising due to their low implementational and operational complexity. Pre-allocation protocols were considered in [4, 5, 1, 3, 6], where random and static access protocols for passive star-coupled photonic systems were proposed and evaluated. This paper studies the impact of transmitter switching latencies through semi-markov models and discrete-event simulation. The performance is evaluated in terms of network throughput and packet delay with variations in the number of nodes, data channels and packet generation rate.

Description of Protocols: The first approach is a simple random access scheme based on interleaved access of Slotted Aloha (I-SA) channels. The second approach statically allocates interleaved access in a time division fashion (I-TDMA) where a source node transmits on the home channel of the destination node in the pre-assigned slot of the source node with non-gated sequential service.

With I-SA, any node that has a packet to be transmitted to any other node attempts transmission after α time slots corresponding to the time required by a tunable transmitter to switch to the wavelength of the destination node home channel. Time is slotted and transmission is synchronized to data packet boundaries. If a collision occurs during packet transmission, the transmitter behaves as with Slotted Aloha.

Collisions can occur during the transmission of a packet with the I-SA protocol described above. This requires packet retransmission which increases the packet delay and decreases the network throughput (but doesn't require an additional switching interval). The I-TDMA protocol avoids collisions and the complexity of supporting transmission of acknowledgments and retransmissions by time multiplexing access to the destination nodes. Time is slotted on each channel, and the home channels are pre-allocated for packet

[1] This work was supported by the National Science Foundation under Grant CCR-9010774 and ECS-9112435.

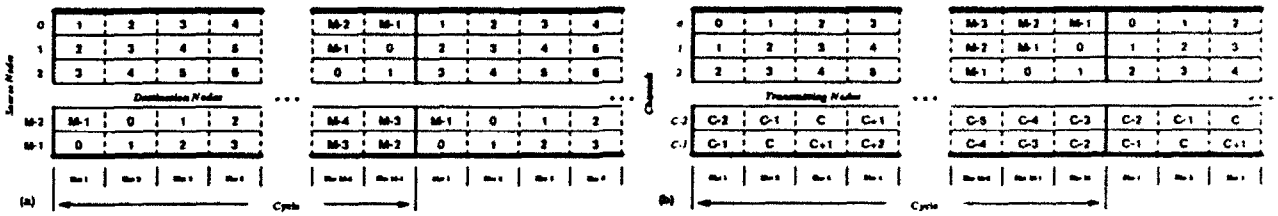


Figure 1: Allocation map for I-TDMA. (a) Source Node/Destination Node space-time diagram when $M = C$ and cycle length is $M - 1$ slots, (b) Channel/Transmitting Node space-time diagram when $M > C$ and cycle length is M slots.

reception. Every node in the system has a chance to transmit to a destination node on each channel per cycle.

Determining the slot which is assigned to a particular source-destination pair is simple and decentralized and based on the home channel allocation policy defined above for I-SA. Fig. 1(a) shows an example of a source node/destination node allocation map when $M = C$. Each node has a slot reserved for it on each channel (other than its home channel) during each cycle. In this case, optical self-routing is achieved and the cycle has a length of $M - 1$ slots assuming that a node will not be required to transmit to itself. Fig. 1(b) shows a channel/transmitting node allocation map when $M > C$. Partial optical self-routing is achieved with this case and the cycle has a length of M slots since transmission on the home channel of a node will be necessary since it may be shared. The tuning time required by the transmitters is overlapped with the initial synchronization time required by time multiplexing. A node is assigned a total of C slots per cycle and remains idle for the remaining $M - C$ slots. However, as shown Fig. 1, the channels are fully allocated with both cases. The overlap of switching latency with the wait time reduces the impact of tuning time on the performance of I-TDMA.

Performance Analysis: The I-TDMA and I-SA protocols described above are analyzed through semi-markov models. The models assume that at most B packets can be buffered at the transmitter. The models enable prediction of the behavior due to changes in various parameters such as the number of nodes, the number of channels, the switching latency and the packet generation rate. The performance metrics of primary concern are network throughput, buffer occupancy and average packet delay.

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WB3 **AN ALL-OPTICAL MULTIFIBER TREE NETWORK**

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Problem Description

Because the bandwidth of single-mode optical fibers significantly exceeds that of electronic devices, it is desirable to eliminate electrooptical bottlenecks within the network. All-optical networks afford the well-known advantage of message transmission without intermediate electrooptical conversion. However, signal distribution in all-optical networks presents problems unless optical amplifiers are used, since optical power is lost in fibers, splices, and couplers. Consequently, most proposals for all-optical networks rely on the liberal use of optical amplifiers, such as erbium-doped fiber amplifiers. Currently, such amplifiers are expensive and prone to failure because of their reliance on pumping lasers.

It is commonplace for manufacturers to package many optical fibers in a single cable. For example, AT&T offers cable with a count of over 200 optical fibers, and Cavi Pirelli sells cable with a count of over 600 optical fibers. Given that the bandwidth of a single-mode optical fiber exceeds a terabit/s [Bra90], the aggregate bandwidth of a multifiber cable approaches a petabit/s. It is the goal of this presentation to describe a network design to harness the potential of multifiber optical cables.

Although multifiber optical cable is more expensive than single-fiber cable, the marginal cost of an additional fiber is low, because packaging and other expenses dominate the cost of the cable. The cable structure is the same for a few fibers as for many fibers. Even more significant is the fact that the cost of installing and maintaining the cable is roughly the same for a high-fiber-count cable as for a low-fiber-count cable. It has been reported [HMTS90] that the installation cost for a linear foot of cable runs as high as $23 in a campus setting—this figure is higher if conduit needs to be constructed or rights-of-way obtained. The upshot is that the acquisition and installation costs for multifiber and single-fiber cable systems differ by little.

With few exceptions (e.g. [Kar88]) the exploitation of multifiber optical cables has not been aggressively explored. Recently, a proposal for a multiple-bus network that is based on ideas similar to those presented here appeared in [Bir92]. We discuss multifiber optical networks that employ a combination of time-, wavelength-, and space-division multiplexing to achieve high bandwidth inexpensively. We describe how to construct all-optical networks that achieve very high throughput without reliance on optical amplifiers. These networks, which are based on a multifiber version of TreeNet [GF88], can serve a large population of users. Signal distribution to all users is accomplished with a realistic optical-power budget.

All-Optical Networks Based on Multifiber Cable

The multifiber optical network uses a multifiber cable plant connected by couplers, splices, and optomechanical switches. The network is designed to allow any two stations to communicate directly and without intermediate packet or circuit switches, i.e., in a single-hop manner—although multihop communication is also allowed for users that can tolerate variation in delay. Topologically, the network is a binary tree that consists of nodal "closets" joined by multifiber optical cables. The closets house the couplers and splices that interconnect the optical fibers of the cable plant. Consisting of an array of couplers whose input and output ports are connected to external fibers in a set pattern, closets can be manufactured to specification by automated techniques and efficiently installed in the field by ribbon splicing. The stations of the network are grouped into clusters. The network cable plant can be viewed

as two tiers of trees, the intercluster and the intracluster cable plants. All stations of a given cluster are connected by an intracluster tree, and the intercluster tree connects groups of clusters.

In an accompanying paper [BGK92] we describe in detail how several fiber plants can be embedded within a multifiber cable plant. Specifically, we address the nontrivial problem of how to provide a collection of fiber plants, so that there is complete connectivity among a large population of stations and the fiber plants are capable of meeting a reasonable optical-power budget.

The solution is to embed tree-like fiber plants within a supertree. Given a reasonable optical-power budget, the fiber plants can accommodate a small number of stations. However, a station can select a specific fiber plant by mechanically switching its transmitter to the desired fiber plant. It can be shown mathematically [Mil72, Mil73] that a relatively small number of fiber plants can provide total pairwise connectivity among a large population of stations. A modest level of wavelength-division multiplexing allows users to share a single fiber plant. We give a specific construction to achieve the desired connectivity. We analyze the number of fibers per cable needed to embed the fiber plants and derive formulas for the component (e.g. couplers, splices) counts required. We also determine the number of wavelength-division-multiplexing channels that are needed to provide a given level of service to network users.

We show in the presentation and in [BGK92] detailed examples illustrating how the network can support over 2000 stations with an optical-power budget of less than 50 dB using a 264-fiber optical cable. We also determine for each example network the number of passive optical components needed to implement the network.

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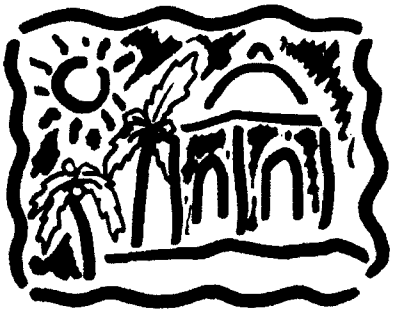
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WA1

INTEGRATED OPTOELECTRONIC REQUIREMENTS FOR CONSUMER APPLICATIONS

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The main attractive point of integrated optoelectronic devices when considering their use in consumer products is their compactness. Sony was the first electronic maker to introduce an integrated optical device ($6.5 \times 6.5 \times 1.7 mm^3$) in a consumer product, the 'Jacket Discman' - a 14.8mm-thick pocketable compact disk (CD) player [1]. Now a 64mm diameter, magneto-optical (MO), digital audio disk system, 'Mini Disc (MD)' is ready for introduction this autumn [2]. This employs two new technologies; a newly developed bit reduction scheme which allows a maximum playback time of 74 minutes, and a buffer memory system to eliminate the effects of shock and vibration making the Mini Disc particularly suitable for outdoor use. Here, we describe integrated optoelectronic requirements for optical disk applications, particularly focusing on the feasibility of an integrated optical pickup for the MD.

There are four main considerations in developing technologies for the MD; power consumption, size, low noise and cost. From point of view of power consumption, an integrated optical pickup used in a portable MD must be as efficient as possible and be combined with a low threshold current LD. The main effort required here is to optimize the coupling efficiency.

Regarding player thickness, conventional optical pickups like those for the ISO standard MO drives are typically 40mm in thickness. A breakthrough is to use an integrated optical pickup such as the 'Laser Coupler (LC)' developed by Sony. As is shown in Fig.1, it consists of a LD chip sub-mounted on a Si substrate with a monitor photo diode (PD) and a $1.5 \times 1 \times 0.6 mm^3$ micro-prism to separate the beams to and from the optical disk. These are both precisely bonded on a Si substrate, where multiple PIN PD's are formed with built-in pre-amplifiers and additional operational amplifiers to obtain RF, focusing and tracking error signals.

Another approach is to use integrated waveguide pickups as proposed by Nishihara et. al [3], because thinner and more sophisticated optical elements can be fabricated using semiconductor processes. A holographic optical element (HOE) is another candidate. However, both these approaches suffer from the fact that diffractive optics tend to be highly dispersive, when used as a lens combined with a LD source, thus chromatic aberration is a serious problem. Very stable visible light sources such as a miniature integrated, diode-pumped, frequency-doubled Nd:YAG laser [4] could overcome this difficulty.

The third consideration is that optical disk systems require very low noise and aberration. The noise sources in an optical disk drive are light source noise, disk noise, photodetector and pre-amplifier noise. An integrated optical pickup tends to suffer from difficulties in isolating the LD from light returning from the optical disk and stray light from optical components, because the LD to disk distance is well within coherent length of the LD. Enormous efforts are required to reduce these disturbances. Furthermore, an optical disk system must remain strictly diffraction-limited even under the severe storage and operating test conditions.

Finally, there is also the important consideration of cost An optimized design using the least number of optical elements with maximum tolerance is required from the viewpoint of mass production.

So far we have discussed the integrated optoelectronic requirements for consumer optical disk applications.

In summary, the smartest way is to integrate conventional and new technologies in a compact device. A low dispersive micro molded lens should be used as a focusing element to avoid chromatic aberration. Alternatively, a very stable LD or a miniature-integrated second harmonic generation (SHG) green laser could be used. In order to realize sophisticated servo error signal detection together with Kerr rotated RF signal detection, integrated optoelectronic devices combined with waveguide and or holographic techniques including a polarization element are promising.

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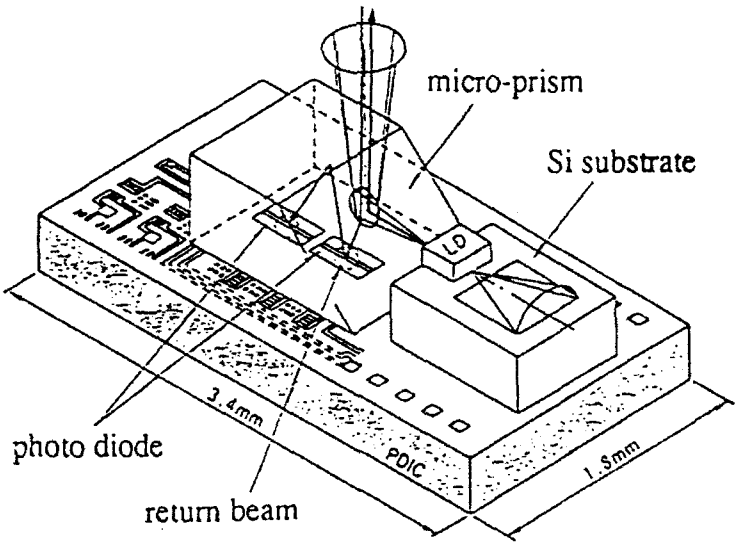


Fig.1 The configuration of a Laser Coupler.

WA2

OEIC'S FOR TELECOMMUNICATIONS

- Invited Talk -

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1. Introduction
2. Dream and Reality
3. Micro-Electronics and OEIC's
4. Analog Function and Digital Function
5. What's an Impediment to progress
6. Toward Photonics-Through-The-Network
7. Concluding Remarks

WA3 MANUFACTURING LOW COST OPTOELECTRONIC COMPONENTS

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Major driving forces for optoelectronic integration are higher performance, improved reliability, smaller size and lower cost. Low cost doesn't automatically occur when an OEIC is designed, and too high costs may impact the acceptance and usage of the part.

This invited paper presents a tutorial on the manufacturing cost of optoelectronic components. The goal is to help researchers better understand how manufacturing cost is calculated, and to show the major factors which affect cost.

The three major elements of product cost (direct materials, direct labor and overhead) are defined. An illustrative example is given showing how these elements are combined together to obtain manufacturing cost. Product volume strongly influences cost and this relationship is discussed in detail. Other factors addressed are chip size, process complexity and yields.

Packaging of an optoelectronic integrated circuit adds additional cost to the product. Assembly and testing costs commonly are comparable to the cost of the optoelectronic chips. This talk will discuss how packaging piece parts and assembly processes affect the manufacturing cost of a component. Low product cost is achieved by careful optimization of the chip, assembly and testing yields.

WB1 WDM DETECTION USING INTEGRATED GRATING DEMULTIPLEXER AND HIGH DENSITY p-i-n ARRAY

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Summary

Multi-wavelength systems are being advocated for use in future telecommunication networks and for computer processor links. In research systems the multiplexing and demultiplexing of the different wavelength signals is currently achieved through the use of bulk optical components. When channel separation are on the order of a nm or so - which is typical of 'high density' direct detection systems - the MUX/DMUX function is generally done with a diffraction grating. WDM detection at the receiver end is then btained by assembling a detector array, placed in the focal plane of the optical grating system.

There is apparant advantage to be gained if the hybrid bulk-optic demultiplexer and array detector system can be replaced by a single monolithic component. Multiple component assembly would be eliminated and the internal alignment would be automatic; reliability would be increased, with the potential for significant cost reduction. In this paper, we report our recent realisation of such a monolithic component. The InP-based device presented integrates a grating-based wavelength demultiplexer with a dense p-i-n array on a single p'anar waveguide structure, measuring about 12mm x 4mm.

The 'optical cavity' of the device is a double heterostructure waveguide, InP/InGaAsP/InP. Through this structure, a vertical-walled focusing diffraction grating is etched [1]. The multi-wavelength input signal is fed into the cavity via a single moded etched ridge waveguide and the demultiplexed, 1-nm spaced, outputs are taken away by similarly etched guides which feed them into monolithically integrated p-i-n detectors. The geometry of the device is shown schematically in Figure 1. A device operating on similar principles operating with a channel separation of 4nm was also recently reported [2].

The grating disperses light signals at 1nm wavelength separation into the output waveguides [1]. The WDM performance is shown in figure 2. This plots the detection wavelength across a span of 75 channels. (Only the position of every second channel is shown in the figure.) The FWHM for channel detection was typically 6Å-8Å. Channels far from each other are well isolated (<-30dB cross-talk), though inter-guide coupling reduced next-neighbor cross-talk to ~-15dB and nearest neighbor cross-talk was - 7-8dB. This could presumably be improved by etching isolation trenches between the guides.

The waveguide detectors integrated with the output waveguides employed a novel waveguide / detector coupling geometry [3]. Ths is a 'hybrid' between the conventional butt- and vertical-coupling approaches, obtained by first growing the waveguide core and detector structure; then, after mesa-etching the detector, the upper waveguide cladding layer is regrown. The resulting structure allows strong coupling between the guide and the InGaAs detector absorption layer, giving near-complete absorption in a short length of detector. The 25μm long detectors employed in the WDM array reported here, absorbed ~90% of the incident waveguide light. The small capacitance of the short detector yielded a detector bandwidth of ~15GHz. See Figure 3.

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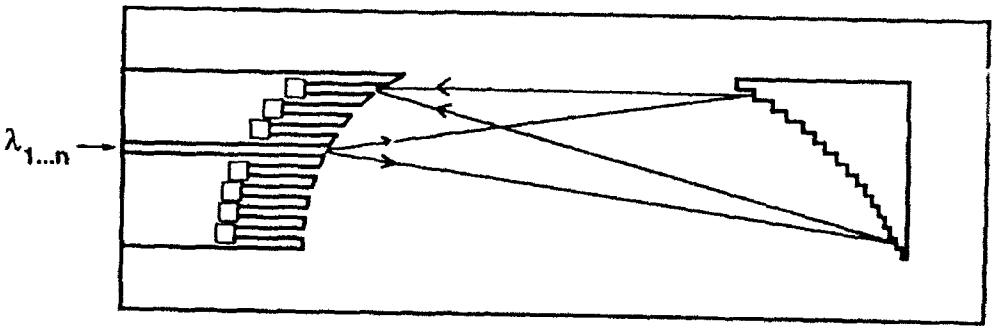


Figure 1. Schematic of the monolithic WDM detector chip.

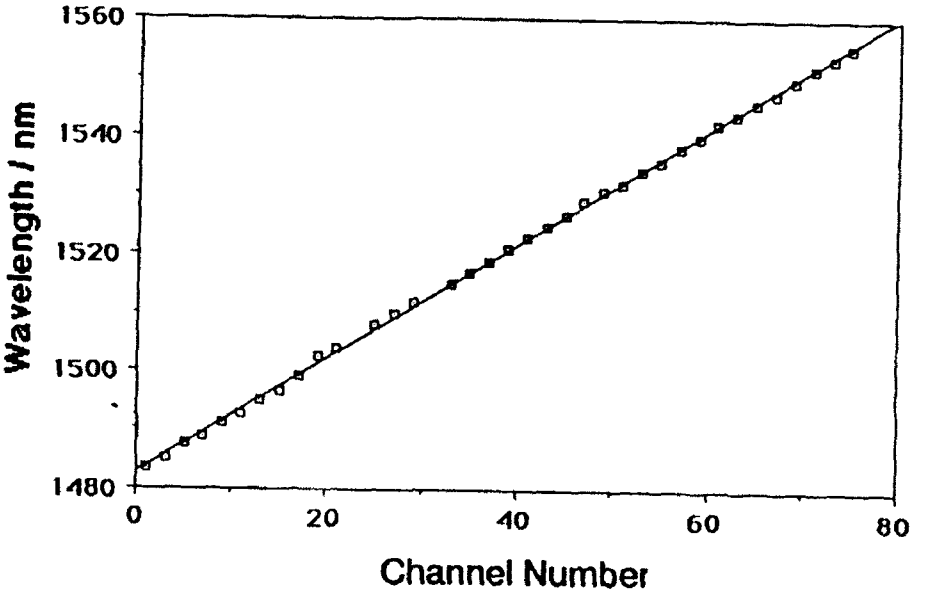


Figure 2. Wavelength demultiplexing performance; position of every second detector shown.

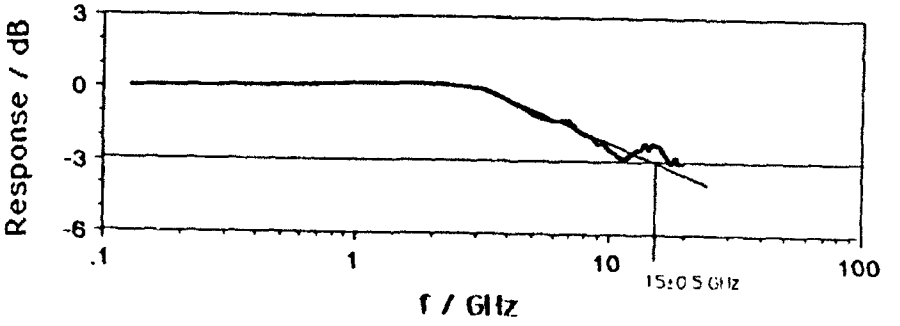


Figure 3. Frequency performance of the 'hybrid' waveguide detector used in the WDM array.

WB2

ECHELLE GRATING SPECTROMETER INTEGRATED WITH CURVED OUTPUT WAVEGUIDES

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Wavelength division multiplexing (WDM) has become an important part of the integrated optoelectronics for optical fiber communication. The most promising multi/demultiplexer design is one that uses an echelle grating spectrometer based on a Rowland circle grating. In this design channels at different wavelengths can be spatially separated and guided into separate output waveguides. Using this configuration, efficient and compact structures were demonstrated with high resolution [1-2]. In these structures, the input and output guides were very close to each other, making measurement and future integration difficult. In this work we demonstrate the integration of echelle grating spectrometer with low loss 90^{o} curved waveguides. This structure is very suitable for the integration of spectrometer with active elements such as lasers and detectors.

A waveguide structure of 1.6 μm $Al_{.28}Ga_{.72}As$ buffer layer and 0.6 μm of GaAs guiding layer was grown by MBE. A thin layer of SiO_2 was sputtered on the wafer which is used as intermediate layer for pattern transfer into GaAs. The echelle grating and outer portion of the curved waveguides were then defined by focused ion beam (FIB) lithography in PMMA resist and reactive ion etched (RIE) into the oxide and the GaAs layer. Finally the straight and inner portion of waveguides were fabricated by a second step of FIB lithography and RIE.

A schematic diagram of the structure is shown in Figure 1. It consists of one input waveguide, one echelle grating and eight curved waveguide outputs. The size of the structure is 8.5 mm x 2.5 mm. The separation between outputs facets is 300 μm. both eighth and eighteenth order gratings were fabricated. The length of the grating region is 1 mm. Input and output waveguides are 4μm and 6μm wide respectively.

TE polarized light from a tunable Ti:sapphire laser was coupled into the device through a polarization preserving fiber. The output response was imaged on an infra-red camera and measured with an InGaAs photodiode. Eight channels near 1 μm having 2 nm separation were measured. Figure 2 shows the wavelength response of one of the output channels. The channel width was typically 1.5 nm in good agreement with the theoretical estimation. Cross talk between neighboring was typically -7 dB. Insertion loss of the device will be discussed.

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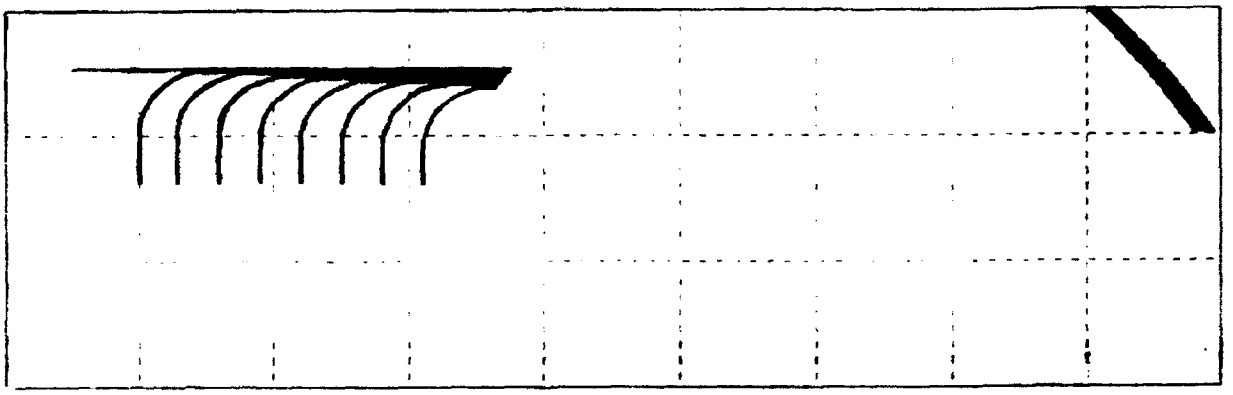


Fig. 1 : Schematic view of the echelle grating-curved waveguide structure.

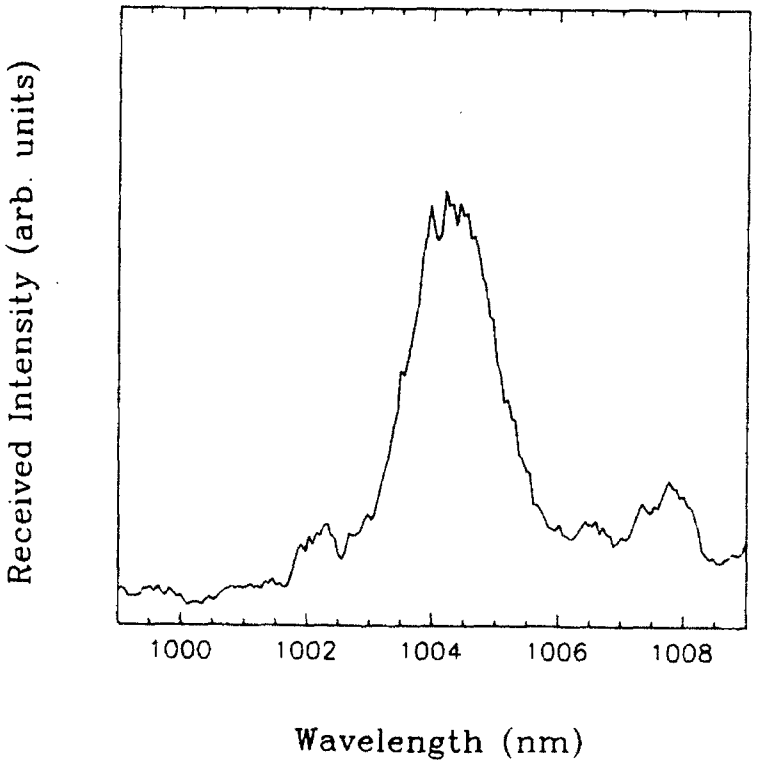


Fig.2 : Wavelength response of one the output channels.

WB3

InGaAs/InGaAsP INTEGRATED TUNABLE DETECTOR GROWN BY CHEMICAL BEAM EPITAXY

by

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The below threshold biased tunable distributed-Bragg-reflector (DBR) laser has recently been used as a tunable wavelength demultiplexer with the advantages of simple integrated structure, convenient center wavelength tuning and easy filter bandwidth controlling [1]. However, some disadvantages have also been observed [2]. First, using the active medium as a detecting medium produces lower quantum efficiency and higher signal distortion. A quantum detector (instead of Fermi-level detector) is necessary to be added to the back of the active filter to separate the detection function and filter function of the device. Second, even though the DBR laser is single mode when biased above threshold, it usually allows more than one Fabry-Perot (FP) mode under the Bragg reflection band (stop band) of the waveguide grating. Fig. 1 shows the below threshold noise spectrum of a typical DBR laser we have been using. When such a device is used for active filtering and amplifying, signals with the same frequencies as other FP modes will get amplified and make the output very noisy. This problem limits the useful tuning range of the tunable detector to only half of the FP mode spacing. In order to fully utilize the tuning range of a DBR active filter, a carefully designed device with only one below-threshold FP mode has to be fabricated for operation. Taking the advantages of excellent uniformity and well controlled growth rate of chemical beam epitaxy (CBE), we report in this paper the design, fabrication, and performance of such an integrated tunable detector with the desired features we described above.

Fig. 2 shows the growth layer and device structure of the integrated device. A waveguide detector with the same material as the laser active medium is added to the back of the DBR filter with no additional processes. The grown layers of the DBR laser have a 2700 Å thick 1.25 μm wavelength InGaAsP (1.25 Q) waveguide layer and a 250 Å thick 1.25 Q grating layer with thin InP etch stop layers in between. The gain medium, on top of the grating layer, is composed of six 50 Å thick InGaAs strained quantum wells and six 120 Å 1.25 Q barriers. Because the thickness of the grating layer is controlled by the CBE growth time, the waveguide grating coupling constant, κ, is also well defined. In order to obtain the designed characteristics, we need a gain section short enough to produce wide longitudinal mode spacing but long enough to provide the threshold gain. We also need a long and weak grating to provide narrow band reflectivity but not too weak and long to increase the equivalent cavity length. A theoretical calculation by using effective index method has been employed to optimized the design before we did the growth. We found a κ around 50 cm^{-1} provides the optimized result. With the gain and grating sections of 225 and 360 μm long respectively and waveguide loss of 10 cm^{-1} for the passive guide, both the theoretical and measured below threshold spectra show the two side modes are suppressed and can not grow when the bias is increased. Fig. 3 shows part of the calculated results and a comparison of experimental data from a below threshold biased filter with equivalent device structure.

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The completed devices have been mounted for characterization and system experiment. Preliminary result on DC measurement is described below. The fabricated devices have laser thresholds around 20 mA when biased above threshold. Some of the lasers has generated record high side-mode-suppression-ratio of 58.5 dB. A pair of devices with very close output wavelengths were used for DC gain on- and off-resonance measurement. The device has a normal free-space coupling loss around -8 dB which can be considerablely improved when a fiber pig-tail is used. The off-resonance coupling loss is around 3 dB which is a result of the waveguide and grating scattering losses when the signal pass through the active and the grating section. The measured on-resonance gain is 17 dB at the in-waveguide signal level of -26 dBm and reduces to 5 dB at the level of -10 dBm due to gain saturation. Detailed experiment and some of the AC and system experiment results will be reported.

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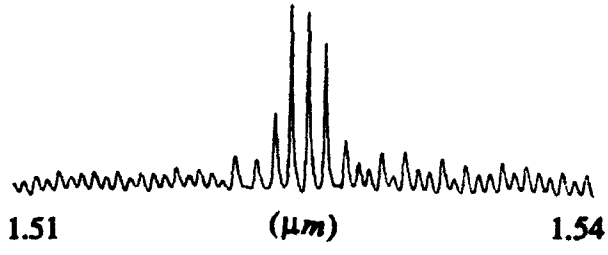


Fig. 1 Output spectrum of a conventional DBR laser when biased below threshold.

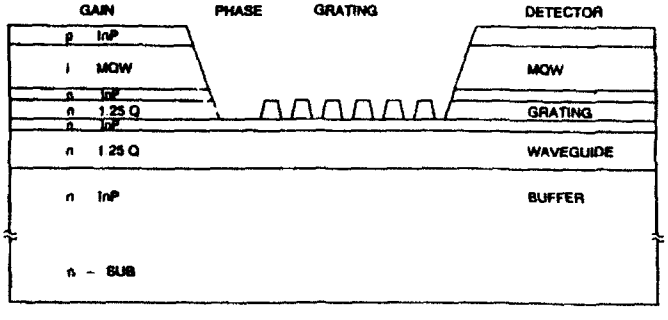


Fig. 2 The growth layer structure of the DBR laser.

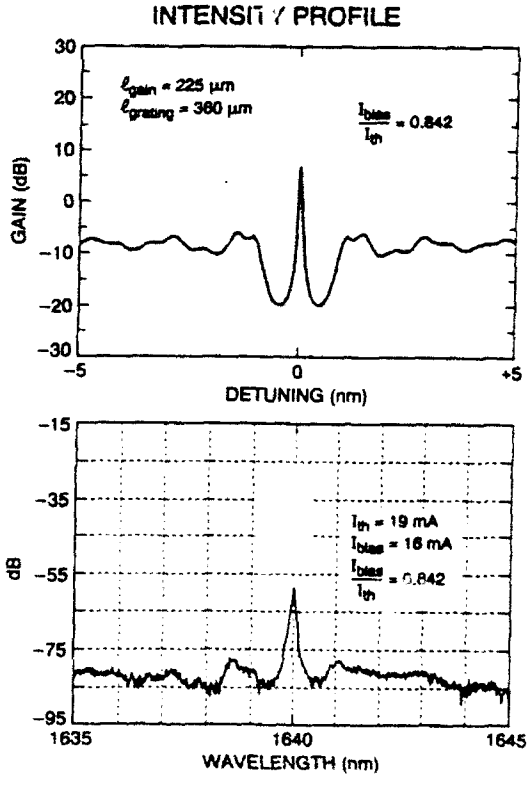


Fig. 3 Output noise spectra, upper: calculated and lower: measured

WB4 WAVELENGTH TUNING IN ACTIVE SURFACE-EMITTING HARMONIC GENERATORS FOR APPLICATION AS SPATIALLY ADDRESSABLE COHERENT DETECTORS

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Recently, there has been considerable interest in enhanced surface-emitting-harmonic generation (SEHG) using GaAs/$Al_xGa_{1-x}As$ multilayer waveguides because of the potential for novel optoelectronic device applications[1-4]. An active SEHG device with an on-board laser reference source offers compatibility with practical optical integrated circuits (OICs). In this work we report on the successful fabrication of active SEHG devices monolithically integrated with double-segment strained InGaAs/GaAs single-quantum-well (SQW) lasers. We investigate the wavelength tuning behavior for the SQW lasers by pumping the two active segments at different current levels. We demonstrate, for the first time, the active control of the deflection angle of output harmonic signals by varying the injection current level in the double-segment lasers.

Figure 1 shows a schematic drawing of the active SEHG device. The epitaxial layer structure was grown on a (100) GaAs substrate using molecular beam epitaxy and consists of an n-GaAs buffer layer (0.5 μm), an n-$Al_{0.66}Ga_{0.34}As$ cladding layer (1 μm), an undoped $Al_{0.90}Ga_{.1}As/Al_{0.66}Ga_{0.34}As$ multilayer (640nm/640nm, 4 periods) embedded with an undoped GaAs/$In_{0.22}Ga_{0.78}As$ SQW separate confinement heterostructure (SCH) active layer (100 nm, 10nm, 100 nm), a p-$Al_{0.66}Ga_{0.34}As$ cladding layer (1 μm), and a p-GaAs cap layer (0.18 μm). The thickness of the multilayer and SCH layers was designed according to the phase matching condition for enhancing the SEHG process. For 1/3 of the laser cavity length (450 μm) in the center region of the device, the p-cap and about 0.8 μm of p-cladding layer was etched away to radiate the harmonic light.

The threshold current of the broad area device was 450 mA when pumping only one active segment. The lasing wavelength measured under pulsed operation was 985.5 nm. The wavelength tuning behavior was investigated by injecting current into the second active segment while keeping the first segment above threshold. When the current on the second electrode is increased from 0 to 100 mA, a wavelength decrease (blue-shift) of about 3 nm was observed (Figure 2). This blue shift can be understood as the result of reduced resonant absorption loss in the cavity due to current injection into the previously unpumped section. Larger shifts can be expected from a ridged device because of the higher carrier densities[5,6].

The SEHG operation is based on the nonlinear interaction between the onboard laser signal and the counter-propagating input signal. Sum frequency light is radiated at an angle from the device surface normal governed by the simultaneous requirements of energy and momentum conservation. This was demonstrated by coupling an 1.06 μm Nd:YAG light into the device as input signal. As seen from Figure 2, the deflection angle of the output green harmonic light was changed by more than 0.4 degrees with increasing injection current at the second electrode. Noting that the phase information is preserved in the overall nonlinear interaction, the current device can thus be used as a novel spatially addressable coherent receiver by electrically tuning the onboard laser wavelength.

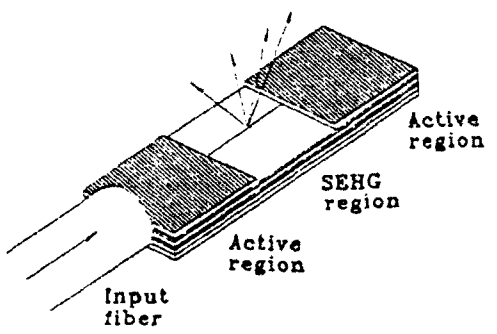


Fig 1. Schematic drawing of double active segment SEHG device.

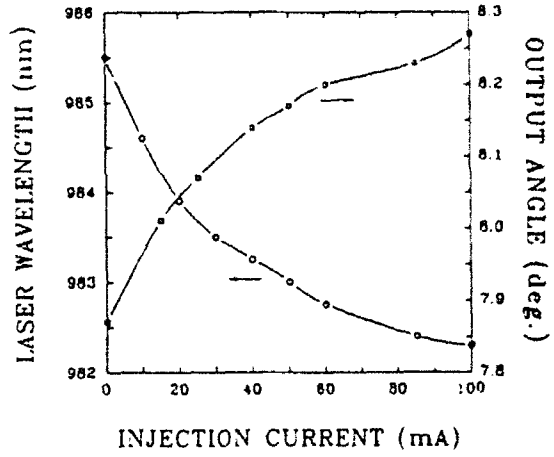


Fig 2. Wavelength tuning and harmonic radiation angle versus injection current.

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WB5

DISCRETELY TUNABLE, MULTIPLE-QUANTUM-WELL, ASYMMETRIC Y-BRANCH LASER FOR WDM NETWORKS

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Tunable semiconductor lasers are crucial components for wavelength-division-multiplex (WDM) optical networks[1]. Wide laser tuning range and fast and simple access to a large number of frequency channels are of primary importance for such systems. In this paper we describe the design, fabrication, and characteristics of a novel multiple-quantum-well (MQW) asymmetric Y-branch (AYB) tunable semiconductor laser. Such lasers appear promising for applications in WDM multi-channel systems.

Discretely tunable lasers produce an optical frequency shift Δf proportional to the refractive index change Δn: $\Delta f/f=\Delta n/n\times$(Lever). Tunable laser structures using distributed Bragg reflection[2] have the index lever factor of unity; the tuning range is then limited by the small achievable index change. The Mach-Zehnder interferometric filter, which is used in the AYB laser, and the co-directional grating-assisted-coupler filter[3] both have a large lever factor that potentially leads to a wide tuning range. To achieve such leverage, the first filter uses a geometrical length difference between two optical paths, while the second uses the material refractive index difference. Using such index levers for tuning, tunable lasers with the co-directional grating-assisted-coupler filter[3] and the symmetric Y-branch lasers[4] have been reported.

A schematic diagram of our AYB laser is shown in Figure 1. Unfolding the laser resonator at the right and left mirror facets shows clearly that a Mach-Zehnder interferometer is the underlying frequency selective mechanism of this laser structure. The design of the AYB laser involves a trade-off among the free spectral range (FSR) (which limits the tuning range and number of accessible frequency channels), the tuning lever, and the filter selectivity (which determines the side-mode suppression ratio (SMSR) of the laser). Figure 2 shows the laser SMSR as a function of the filter selectivity between the main and the side modes; filter discrimination of a few percent is sufficient to produce SMSR of 20dB.

For our optimized design of the AYB laser in Figure 1, the branch lengths are $L_1\approx1201\mu m$, $L_2\approx1263\mu m$, and $L_3\approx300\mu m$, for a total device length of $1500\mu m$. From the geometry, we expect the side-mode transmission of 98.4%, and SMSR≈15-20dB. Separate electrodes are formed for branches 1,2, and 3, and the laser is tuned with current through segments 1 or 2. We minimized the radiation loss of the bends and the bend-to-straight waveguide transitions by parabolically tapering the waveguide curvature; the minimum radius of curvature is $R_{min}=700\mu m$.

The AYB lasers were fabricated using the Semi-Insulating Buried Ridge (SIBR) transverse laser structure, shown schematically in Figure 3. First, the base wafer is grown by Metal Organic Vapor Phase Epitaxy (MOVPE), including a four quantum well, compressively strained InGaAs/InGaAsP active layer. Then the active ridge structure is produced by a combination of selective and non-selective chemical etches. Finally, the ridge, which contains the MQW layers, is buried by the semi-insulating InP current blocking layers. To produce electrical isolation between the different electrodes of the AYB laser, we have used a shallow reactive ion etch with ohmic contact metallization as the etch mask. The SIBR laser structure is easy to process, allows flexible transverse mode control, and provides excellent electrical isolation between electrodes of multi-segment lasers, such as the AYB lasers.

The devices were tested as cleaved with no facet coatings. The lasing threshold was 65mA when all three segments were connected in parallel, and the output power reached 13mW. Electrical isolation between segments was ~10kΩ. Figure 4 shows tuning of the AYB laser with current I_2

through segment 2, while the other two currents were fixed. For most steps in Figure 4 the laser operated in a single longitudinal mode, although a few steps were multimode and a few Fabry-Perot modes were skipped on tuning. With this single-knob control, the tuning range is 890GHz (6.7nm), with the average tuning rate of 29GHz/mA, or about 1mA/mode (channel). An inset in Figure 4 shows the spectrum of one of the modes. Overall, 24 single-mode frequency channels over 1.0THz (7.5nm) range could be accessed with a single current control. Fast channel switching is expected, because all the laser segments are active. Under different bias conditions, tuning rates in excess of 100GHz/mA were observed, with tuning direction dependent on whether the longer (2) or the shorter (1) segment was used for tuning. Such high tuning rate confirms the large tuning lever of the structure. Further design improvements promise even wider tuning ranges for such AYB tunable lasers.

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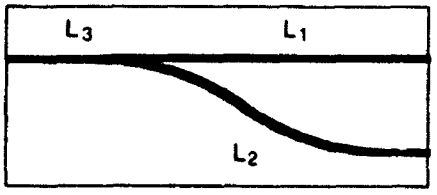


Fig. 1. Schematic diagram of the AYB laser structure.

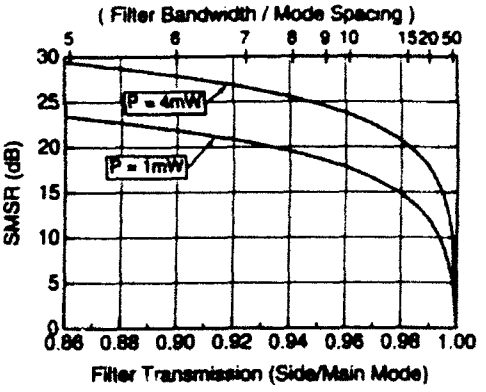


Fig. 2. Side-mode suppression ratio of a laser with an intracavity filter.

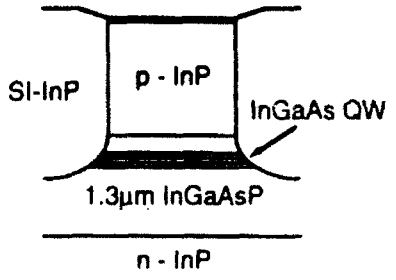


Fig. 3. Semi-Insulating Buried Ridge (SIBR) transverse laser structure.

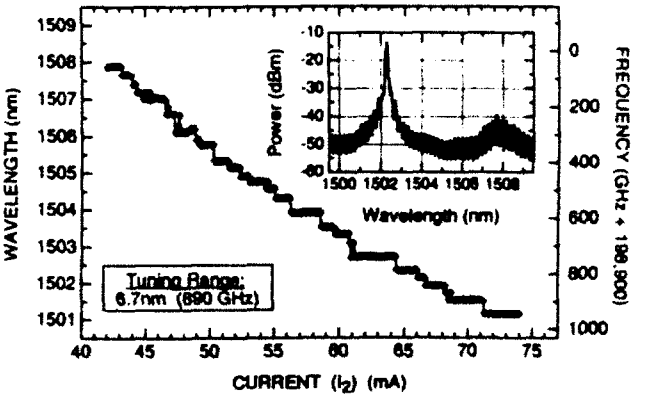


Fig. 4. Frequency tuning of the AYB laser with current I_2. Inset: mode spectrum (SMSR=18dB).

WC1

SELECTION & OPTIMISATION OF TECHNOLOGIES FOR A GENERIC InP OEIC CAPABILITY

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Introduction

Progress towards InP-based OEICs has now reached MSI size at a few research centres, and good yields have been obtained on simple circuits, such as receiver arrays. Until now most studies have concentrated on binary combinations of technologies such as electronics and detectors, electronics and lasers, or lasers and waveguide devices. Future applications will necessitate richer functionality, the attainment of which would be greatly simplified by a generic electronics technology compatible with the full range of optical components. This paper summarises recent progress at BT Laboratories towards such a generic technology, and discusses transistor options, and the mutual compatibility of analogue and digital electronics, lasers, photodetectors and waveguides.

Integration Objectives

The primary objectives of OEICs are of system cost reduction through enhanced monolithic functionality, simplified packaging and reduced parasitics. Clearly there is a level beyond which hybrid integration is more effective, but at this limit a system composed of complex OEICs interconnected on a silicon motherboard is envisaged.

Applications under consideration include:-

* OEICs, especially arrays, for telecommunications access, core and switching
* interfaces between optical networks and high complexity silicon ICs
* interfaces between optical and radio networks
* 2D arrays of optoelectronic functionality for 3D optical processing or switching

The criteria for selection of a generic process centre on:-

* performance *compatibility *simplicity *reliability *yield
*cost *turnaround time (from concept to market)

Progress To Date

Key features of four transistor structures at differing levels of development at BTL are given in Table 1. All technologies were grown using rotating substrate epitaxy and processed as full wafers. The GaAs MESFET is a strong candidate as performance of devices grown on InP substrates is essentially identical to that from a standard MESFET process, and reliability results are favourable. The process has been modified for OEICs by using a using a seeded mask to obtain quasi-planar horizontal integration of islands of GaAs electronics with InP-based optoelectronic regions. This mature process can, in principle, be used with short-gate GaAs PHEMTs on InP to give high performance electronics, where needed.

The lattice-matched diffused InGaAs JFET process has optical components grown above electronic layers on unpatterned substrates. Selective etching is used to expose FET layers. This process requires fewer epitaxial growth stages, but has limited potential and higher gate leakage. An alternative is the InGaAs/InAlAs HFET, which has threshold voltage uniformity better than 50 mV across 1 cm. The same device has demonstrated applicability from MSI circuitry at a few Gbit/s with 0.7 μm gate-length, to MMICs with an f_t of 113 GHz obtained on a 0.25 μm T-gate. Compatibility of the HFET with optical devices has been demonstrated [1], [2]. BNR have recently produced a PINHFET receiver OEIC with a BER of -21.2 dBm at 6 GBit/s, using similar technology with a gate-length of 1.5 μm [2].

GaInAs/InP HBTs have shown considerable promise [3], as confirmed by f_t of 60 GHz with a 5x5 μm emitter size. However, simpler circuit design is offset by complex interconnection.

Circuits

The MESFET and JFET have been used in various OEIC receiver designs culminating in a 4 channel variable bandwidth receiver array with level shift and 50 Ohm buffer. For the JFET yields above 80% for single channel, >60% for 4 channels have been obtained, with a sensitivity of -31.2 dBm at 1.4 GBit/s, [4,5]. BNR have recently reported an 8 channel receiver array OEIC using grown-in JFET technology, a BER of -32.1 dBm at 622 MHz was achieved and 37% of circuits had all 8 channels operational [6].

Integration with lasers is more difficult, and a buried heterostructure laser in particular would increase complexity. We have used a ridge waveguide (RW) design, modified for use on semi-insulating substrates. Integration of a 4 transistor drive circuit with a double-cleaved laser produced good yields of functioning transmitters. In a more complex OEIC, an etched facet RW has been incorporated in a full regenerator circuit (external clock). All the features of this chip: detector, pre-amplifier, gain block, latch, driver circuit and laser are functional - a total of 120 elements. More significantly, optical detection and emission have been monolithically integrated with both digital and analogue electronics. The high level of complexity can be extended by increasing circuit size and functionality. The Fabry-Perot laser can be modified to a DFB laser, and waveguides and related devices can be included by a generic scheme which will be discussed. Additionally, non-linear switching elements give, in principle, the ability to incorporate optical non-linear functions.

Conclusions

Many future OEICs will need an intimate mix of electronic and optoelectronic devices. The generic process described here allows systems designers to exploit whichever functional element best suits their application, and to have them monolithically integrated for low cost, high functionality solutions. The final cost of OEICs will be determined by demand.

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TABLE 1

	GaAs MESFET on InP	InP/InGaAs JFET on InP	InP/InGaAs HBT on InP	InAlAs/InGaAs HFET on InP
Feature Size (μm)	1	1	5x5	0.25
Performance gm (mS/mm) or β	170	250	300	270
Vt (V)	-1.50 ± 0.20	-1.50 ± 0.15	0.9	-1.50 ± 0.05
ft (GHz)	16	22	60	100
Integrability	medium	high	high	medium
Maturity	high	medium	low	low-medium
Overall Suitability	demonstrated but limited	demonstrated but limited	good but needs much development	potentially best

WC2 HIGH BANDWIDTH InGaAs p-i-n PHOTODETECTOR ARRAY FOR OPTOELECTRONIC SWITCHING APPLICATIONS

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With the advent of optoelectronic and fiber technologies, applications for OE switching have steadily increased. Examples of these applications are steering of phased arrays,(1) optical crossbar switching,(2) and programmable transversal filters.(3) In this paper, we report our work in developing a 5-GHz-bandwidth bias switch using an array of 1×4 InGaAs p-i-n photodetectors with 4 discrete GaAs MESFETs and 4 capacitors. These devices are assembled in a custom-made high frequency package (Fig. 1).

The cross-section of the back-illuminated InGaAs/InP detectors is shown in Fig. 2. Figure 2 also shows a 1×4 InGaAs photodetector chip. The chip size is 0.5 mm × 1.6 mm, and the 4 detectors are on 400 μm centers. The photodetectors are connected in a common cathode configuration with the FET switches used to open the unwanted detector circuits. These four detectors have very uniform electrical and optical characteristics. The detector leakage current is very low: a typically 65 pA at –5.0 V. The capacitance is 65 fF at –5.0 V for each detector, and the quantum efficiency for the non-AR-coated diode is 60%.

In the bias switch (Fig. 1), the detector array is flipchip bonded onto a ceramic submount. Multiple input beams from four fibers are incident and focused on each of the four mesa detectors through the transparent InP substrate. A FET switch is connected in series with each of the four detectors to perform signal selection. By closing a particular FET switch and opening all others, we can detect the particular optical beam we desire. Clearly the FET switch on/off ratio, the bandwidth of the array, and the RF insertion loss through the switch are important to fully characterize the switch performance.

We used an optical heterodyne technique to measure the frequency response and on/off ratio of each individual detector in the array. In this experiment, we focused the laser on one detector under test and kept the others in the dark. The detector under test was switched on and off by applying zero and negative voltage, respectively, to the gate of the FET switch. Within the frequency range from dc to 6 GHz, these packaged detectors were nearly identical, with flat frequency performance response to about 4 GHz (Fig. 3). The 3 dB bandwidth is 5 GHz, and we obtained a 70 dB (electrical) on/off isolation ratio. The average photocurrent for these measurements was 7 mA.

We also measured the crosstalk isolation between two neighboring detectors using different frequency tones on each detector. In this experiment, we used two similar pigtailed lasers (1.5 mW output power) with one laser modulated at 820 MHz and the other at 840 MHz. The two input beams were then focused on the two separate neighboring detectors. We measured the RF power output from the bias switch by closing one FET switch corresponding to the 820 MHz, and opening the FET switch corresponding to 840 MHz. The difference in output power between the RF signals at 840 MHz (On), and at 820 MHz (Off), is a measurement of the crosstalk between the two neighboring detectors. In this experiment the crosstalk isolation is 43 dB (electrical) with the average current being 1.0 mA. This result indicates that the electrical isolation between the two detectors in our optoelectronic switch is high.

We further tested the bias switch using a pigtailed 1.3 μm semiconductor laser. The laser was spliced into a 1×4 fiber coupler and was incident on four detectors in the bias switch. The four detectors in the array gave identical frequency performance. The RF fiber link insertion loss was –17 dB measured at 1 GHz from the laser to a single detector in the bias switch, and was –30 dB when we split the optical power to the four detectors. This loss figure is consistent with the excess loss figure of the coupler. Furthermore, it shows that little or no RF combiner loss occurs in the common cathode configuration.

Because of low RF insertion loss (17 dB), high isolation on/off ratio (70 dB), low crosstalk (43 dB), and high bandwidth (5 GHz), this optoelectronic switch can be used in many applications, such as in a true time delay network for optical control of phased array, crossbar switching, optical delay line programmable filter and wavelength division demultiplexing. To our knowledge, this work reports the highest frequency packaged photodiode array response used for optoelectronic switching.

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Acknowledgment

This work is partially supported by ROME LAB—DARPA under Contract No. F30602-91-C0006. Two of the authors (SRF and YL) are also indebted to DARPA for partial support of this work through the National Center for Integrated Photonic Technology.

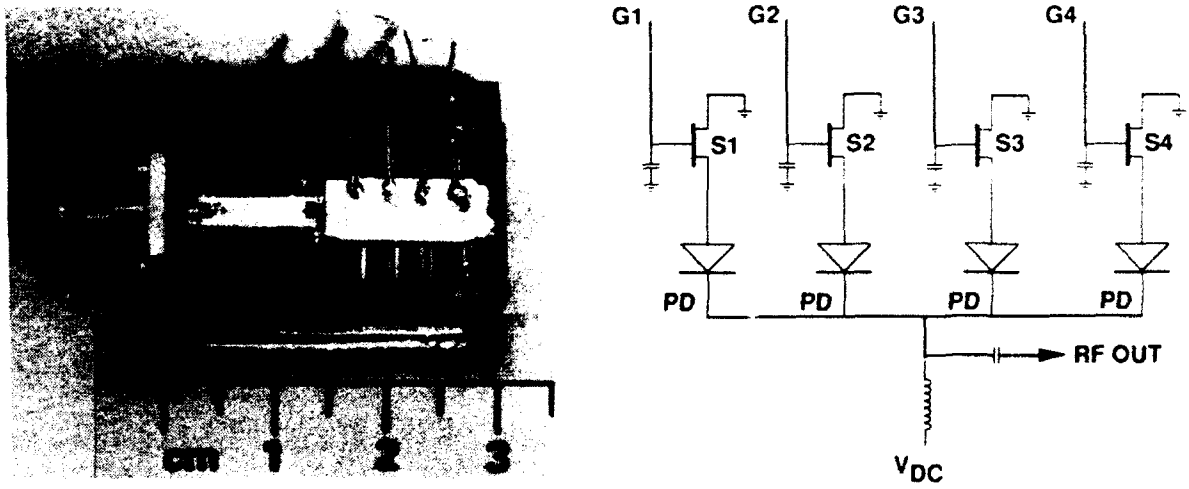


Fig. 1. Photodectector array for optoelectronic switching.

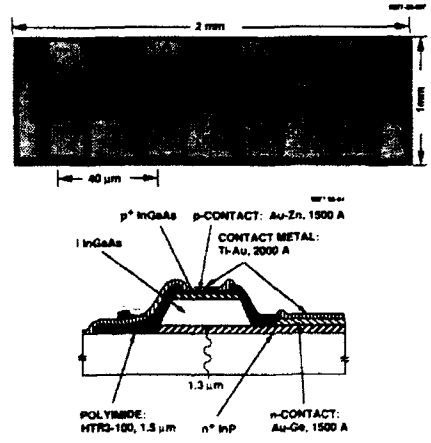


Fig. 2. InGaAs/InP p-i-n photodetector structure.

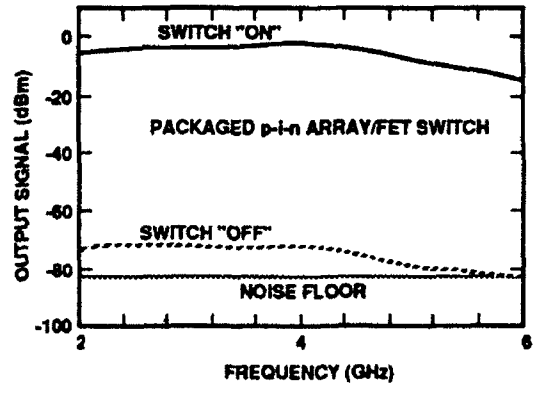


Fig. 3. InGaAs p-i-n detector array frequency response.

WC3

A HIGH SENSITIVITY MONOLITHIC PHOTORECEIVER AT 2 Gb/s INCORPORATING InP/InGaAs PHOTOTRANSISTOR AND BIPOLAR TRANSISTORS

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Most monolithic photoreceivers reported to date utilize either a p-i-n or a metal-insulator-metal (MSM) photodetector for signal detection, driven by the simplicity of the structure and the ease of integration with the electronic devices. There is, however, one other photodetector with a potential for high performance and well suited for monolithic integration. It is the heterojunction phototransistor (HPT), which is identical to the heterojunction bipolar transistor (HBT), with the added feature that the base-collector junction can be a photodiode and photocurrent generated there is amplified by the transistor action. The HPT, with a well designed structure for sufficient quantum efficiency, optical gain and speed, becomes a viable alternative to the p-i-n, or the MSM, or even the avalanche photodetector (APD). We had earlier demonstrated [1], for the first time, an all-bipolar monolithic photoreceiver incorporating an HPT followed by HBT amplifiers and showed successful operation at 100 Mb/s. In a subsequent work [2], we showed that the only advantageous way of using the HPT is with a base terminal, under which condition it can have large optical gain and bandwidth at low incident optical power. In this paper, we follow up our earlier work and demonstrate for the first time the use of an InP/InGaAs HPT in a multi-gigabit all bipolar monolithic photoreceiver.

Epitaxial layers grown by metal organic molecular beam epitaxy (MOMBE) were used to fabricate the photoreceiver. The HPT was a single heterostructure design, with a 1μm thick InGaAs collector for light absorption and an InP sub-collector facilitating backside illumination. An advanced self-aligned process was used to fabricate the transistors. The monolithic photoreceiver was a transimpedance design consisting of an input three-terminal phototransistor followed by two HBT amplifying stages built from the same transistor structure (Figure 1). The transistors had each an emitter-base junction area of $7\times13\mu m^2$ and base-collector junction area of $15\times33\mu m^2$.

Individual phototransistors exhibited small signal electrical current gain between 150 and 200, with a quantum efficiency of 40% for the base-collector photodiode (with no anti-reflection coating). The packaged photoreceiver was tested at a wavelength of 1.53μm. The small signal bandwidth was 1.1 GHz with a smooth roll-off (Figure 2). A bit error rate measurement was performed at 2 Gb/s and yielded a sensitivity of -26.3 dBm for a bit error rate of 10^{-9} (Figure 2). This is the highest bit rate operation demonstrated for any long wavelength phototransistor. The sensitivity-quantum efficiency product of -30.3 dBm makes our result comparable with the best p-i-n hybrid photoreceiver at this bit rate. The results also confirm our earlier finding that operating the HPT with a base terminal enhances its speed without compromising noise due to the additional base current.

In summary, we have demonstrated an all-bipolar monolithic photoreceiver, incorporating an InP/InGaAs phototransistor, operating at 2 Gb/s with high sensitivity. The simplicity of the implementation makes it attractive for application at higher speeds.

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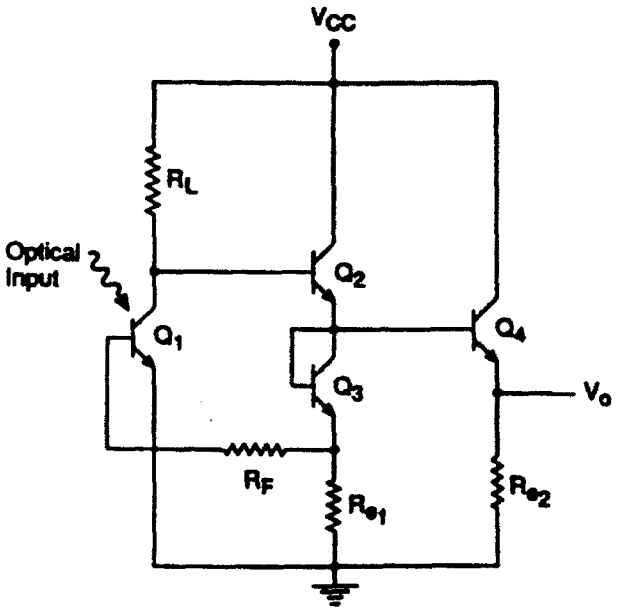


Figure 1

Circuit schematic of the all-bipolar photoreceiver.

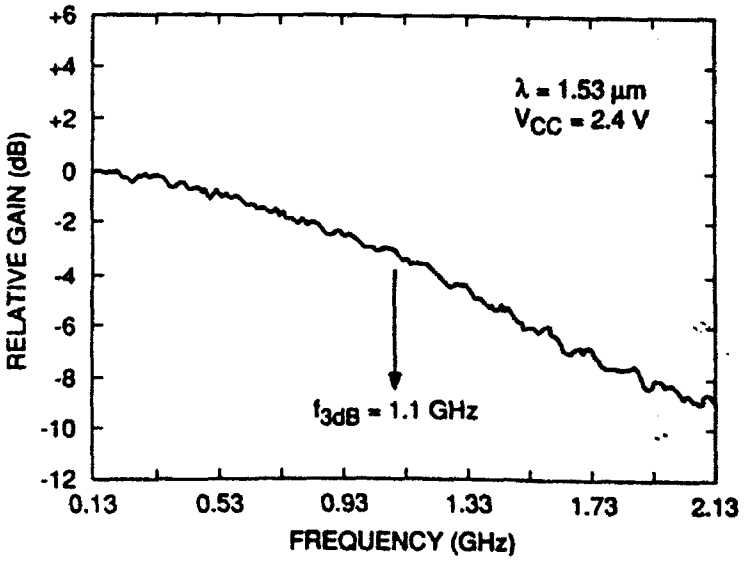


Figure 2

Small signal frequency response of the monolithic photoreceiver.

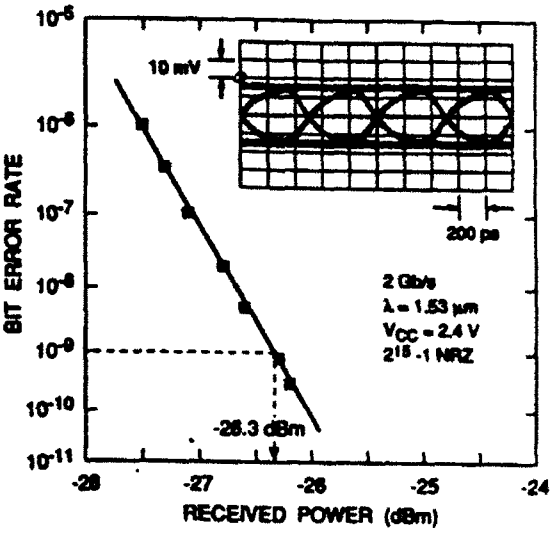


Figure 3

Measured sensitivity of the photoreceiver at 2 Gb/s.

WC4

FABRICATION OF A MONOLITHICALLY INTEGRATED InP-based WAVEGUIDE-pin PHOTODIODE FIELD-EFFECT TRANSISTOR TRANSIMPEDANCE RECEIVER OEIC

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An InP/InGaAs transimpedance photoreceiver OEIC comprising a photodiode (PD) coupled to an InGaAsP waveguide and a preamplifier in JFET technology is demonstrated for the first time. This is in contrast to previous works /1,2/ where only one JFET has been integrated. Fig. 1 shows the circuit diagram of the photoreceiver. The preamplifier comprises a cascode input gain stage and a source follower to provide a 50 ohm output impedance. The OEIC circuit contains in particular a waveguide fed photodiode (PD), three junction field-effect transistors (JFET) and five WSi_x resistors. The vertical coupling between the slab waveguide (WG) and the photodiode is achieved by evanescent field coupling. A micrograph of the OEIC chip is shown in Fig. 2.

The layer sequence was grown lattice-matched on a planar semi-insulating InP:Fe substrate by single step metalorganic vapor phase epitaxy (MOVPE). A schematic cross section of the planar OEIC is shown in Fig. 3. The layer structure consists of a 1.0 um thick n^+-doped InP buffer layer, an 0.5 um thick undoped InP layer, an unintentionally doped 0.7 um thick InGaAsP ($_g$= 1.05 um) waveguide layer, an 0.2 um thick undoped n^--InP intermediate layer, an 0.95 um thick n^--InGaAs absorption layer and an 0.3 um thick n-InP cap layer. In this WG/PD layer sequence the JFET structure was implemented by three local ion implantation steps /3/. The n^+-doped InGaAs channel was realized by a Si implantation and the buried p layer beneath the channel was formed by Be implantation. The space charge region of this p-n junction confines the drain current to the channel of the JFET and suppresses the influence of the underlying layers. An additional Si implantation was performed to reduce the n contact resistance of source and drain of the JFET. The implantations were simultaneously annealed at 700 ^{0}C for 30 s. The WSi_x resistor layer was deposited by RF bias sputtering from a W(Si) 60 at% target in an Ar plasma. The resistors can be trimmed by reactive ion etching using a CF_4/H_2 gas composition.

The pin PD with a large photosensitive area of $3x10^{-5}$ cm^2 exhibits a low dark current below 10 nA at a reverse bias of - 10 V. The insertion loss of the OEIC without antireflection (AR) coated WG facet is 10 dB. The WG propagation loss is 2.5 dB/cm and decreases to 1.8 dB/cm after annealing. JFETs with a gate length of 1.5 um and a gate width of 100 um have a maximum transconductance of 160 mS/mm and a cut-off frequency of 10 GHz.

To determine the performance of the WG photoreceiver OEIC the signal-noise ratio was measured in the frequency range from 10 MHz to 300 MHz. Fig. 4 shows the measured frequency response and the equivalent input noise current spectral characteristic whereby in this measurement set-up the PD was front illuminated. A 3 dB bandwidth of 190 MHz was determined and a receiver sensitivity of -28.5 dBm at a BER of 10-9 was estimated at for a 400 Mbit/s NRZ signal at a wavelength of 1.3 um.

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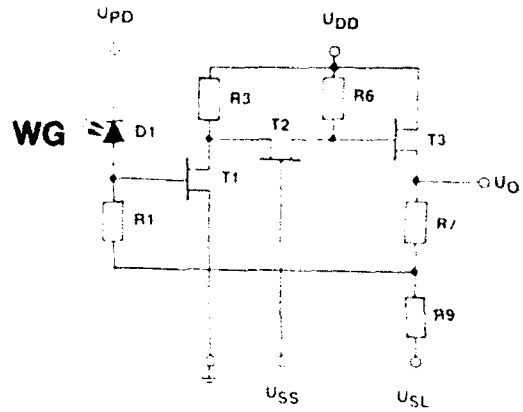


Fig. 1 Circuit diagram of the waveguide transimpedance receiver

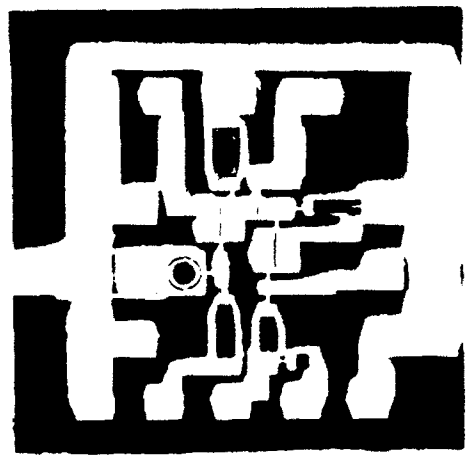


Fig. 2 Micrograph of the waveguide OEIC receiver chip

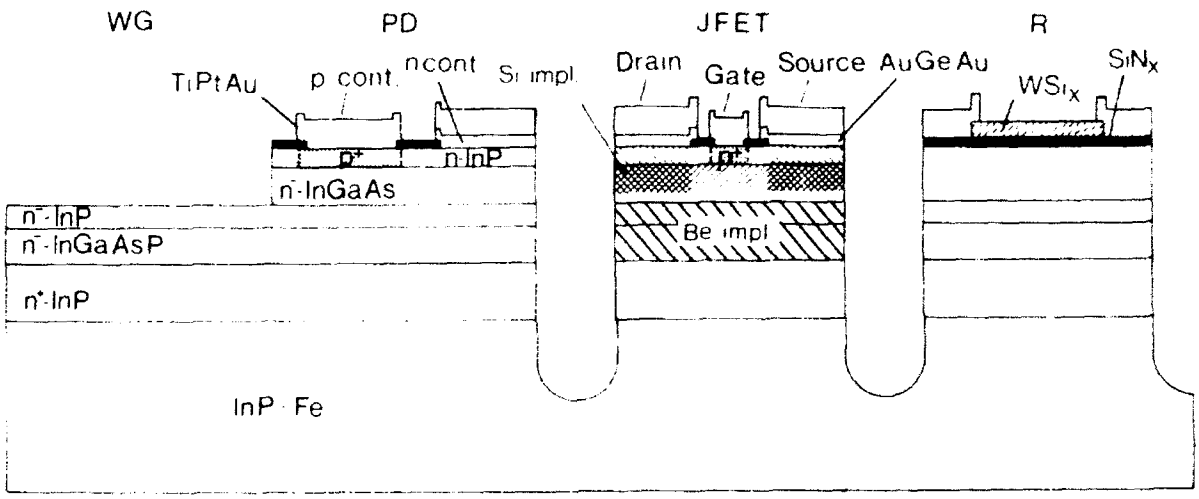


Fig. 3 Schematic cross section of the receiver OEIC layer structure with a waveguide (WG), a pin photodiode (PD), a field-effect transistor (FET), and a WSi_x resistor (R)

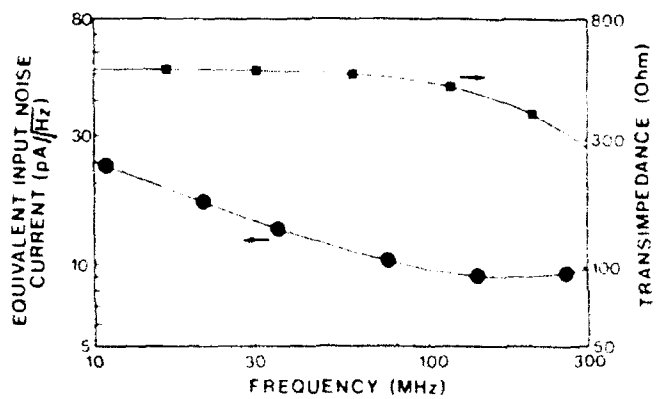


Fig. 4 Equivalent input noise current spectral characteristic and transimpedance of the waveguide-OEIC

WD1

OPTO-ELECTRONICS TECHNOLOGY FOR AVIONIC AND SPACE APPLICATIONS

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Over the last several years it has become widely recognized that electromagnetic interference(EMI) electromagnetic pulse(EMP), high intensity radio frequency(HIRF) and new threats such as directed-energy weapons, can jeopardize the flight safety of aircraft/rotorcraft that use Fly-by-Wire(FBW) flight control systems, unless adequate shielding precautions are taken. In addition, the long term trend in the aerospace industry is the increasing use of more composite materials in airframes. This will minimize the inherent electrical shielding compared with the metal skins used in the past. Lastly, the demand for computers and high speed data networks within aircraft/rotorcraft/space vehicles, will present new shielding and maintenance problems. The use of an electrical wiring system for flight control applications leads to weight and maintenance penalties. Preliminary estimates by a variety of sources suggest a weight penalty of approximately 250-1500 pounds for a transport aircraft having a FBW system compared with the use of an analogous Fly-by-Light(FBL) system. In the FBL system, the electrical lines and position sensors are replaced by equivalent optical fibers and position sensors. Multiplexing of sensor and data signals can be more readily implemented using fiber optics compared with electrical wiring. The assurance of maintaining the integrity of the shielding will incur additional maintenance costs. The weight penalties are sensitive to the assumed level of threat. For space vehicle systems, fiber-optic technologies offer the potential for significant weight savings and correspondingly reduced launch costs.

Thus, there are strong technical and economic incentives for the development of fiber-optic based systems for both military and commercial aerospace vehicles. Such systems would be primarily used in the area of avionic data communications at the beginning, and gradually evolve to the more demanding areas of flight and engine control.

The presentation reviews key opto-electronic technologies that enable the implementation of fiber-optic data communication and flight control systems for aerospace vehicles.[1] Technologies which will be discussed include: fiber-optic position sensors using laser radar; sensor

interfaces and multiplexing; fiber-optic Gigabit per second data transceivers, and networks; high reliability semiconductor lasers operating over wide temperature ranges; and optical interconnection technologies. lastly, some of the major engineering problems and limitations of the technology will be discussed.

With the increasing demand for higher information bandwidth within aerospace vehicles, fiber optics and the enabling opto-electronic technology appears positioned for future significant growth over the next 20 years. Such systems will provide more fault tolerant architectures with higher information bandwidth and reduced maintenance costs.

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WD2 FABRICATION OF MSI LEVEL TRANSMITTER OEICs: A COMPARISON BETWEEN Epi-in-a-Well AND THE PLANAR MULTIFUNCTIONAL EPISTRUCTURE (PME) APPROACHES

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Progress in the fabrication technology for manufacture-compatible monolithic transmitter/transceiver OEICs has been minimal due to the lack of demand and complexity in processing. Simple cost/yield benefit analysis of fabrication approaches [1], however, indicate that monolithic transmitter OEICs may be manufactured with significant cost advantage over hybrid versions provided the OEIC fabrication sequence makes use of well developed, standard IC fabrication processes (e.g., using GaAs ED-MESFET, C-HFET or HBT).

Monolithic transmitter/transceiver OEICs for 830 nm have been developed and fabricated for two different application scenarios using standard 3-inch GaAs MSI/LSI ED-MESFET processes (Figure 1). The first, aimed at free space optical interconnects and optoelectronic processing, consists of 64 surface emitting LEDs, 64 photodetectors, 1300 FETs and 500 thin-film resistors [2]. The 21 mask fabrication sequence involves embedding the epilayers within an etched well (epi-in-a-well), planarizing the wafer and the processing of FETs and OE devices.

The second, aimed at optical interconnects in time division multiplexed computing applications, consists of 2 linear electro-optic waveguide modulators, 3 photodetectors (lateral MSM, PIN and phtoconductive photodetectors), and ED-MESFET circuits (390 FETs/ 6 resistors for the transmitter and 40 FET per PD for the receiver circuits). A novel planar multifunctional epistructure (PME) approach [2], with its associated reduced number of masking steps of 18 (see Figure 2), is used for the fabrication of the transceiver OEICs. The PME approach allows ED-MESFETs to be fabricated on totally planar substrates followed by the creation of the transmitter OE devices. In both the cases, the various photodetectors are made in conjunction with ED-MESFET fabrication.

The paper summarizes and compares the two distinctly different approaches, their suitability for manufacture, and the possibility for long-term growth in terms their amenability for the incorporation of other, state-of-the-art devices/circuits, such as VCSELs, edge-emitting lasers/amplifer-switches, and C-HFET and HBT based electronic ICs.

Acknowlegement : The work was supported by the SDIO/IST Directorate and monitored by ONR under contract no. N000014-86-C-0800, by DARPA under contract no. DASG60-87-C-0078, and by Honeywell IR&D funds.

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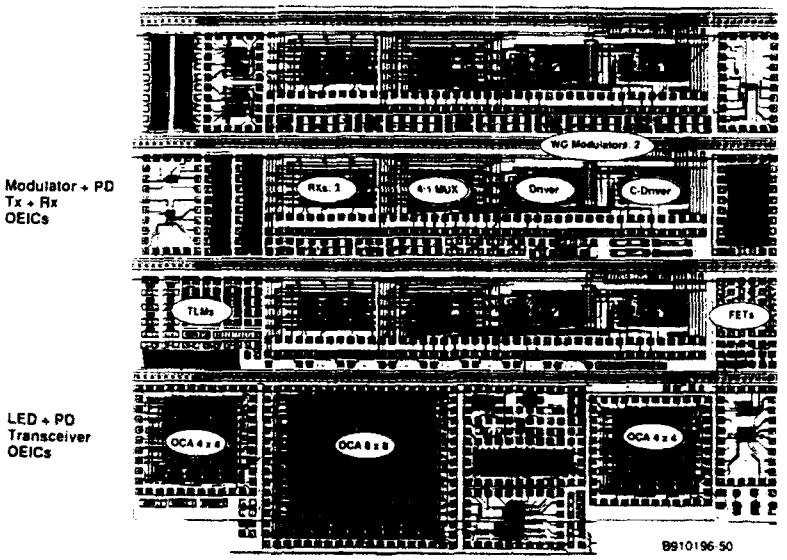


Figure 1. Composite mask layout showing both the OEICs that used standard ED-MESFET standard cells and standard self-aligned-gate (SAG) fabrication process. The two OEICs were fabricated on separate wafer sets.

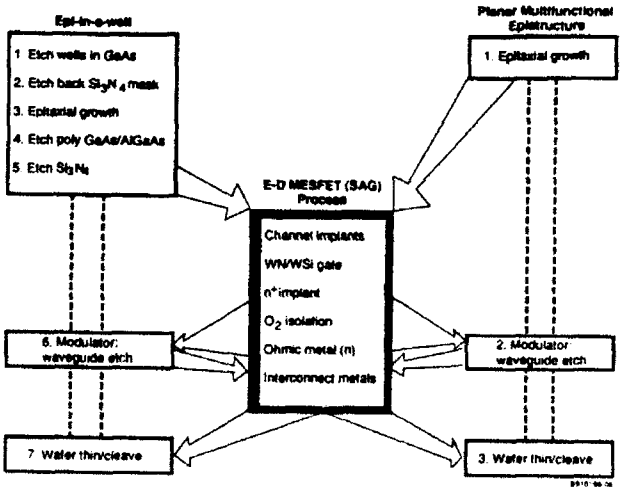


Figure 2. Schematic comparison between epi-in-a-well (left) and the new PME approaches using a common OE device as the device to be integrated with ED-MESFET processes.

WD3

A PSEUDOMORPHIC AlGaAs/InGaAs/GaAs MODFET-BASED OPTOELECTRONIC RECEIVER WITH A 10 GHz BANDWIDTH

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The monolithic integration of electrical and optical devices to produce optoelectronic integrated circuits is very important to the continued development of lightwave communications and optical interconnects for computer communications. A photoreceiver which receives low level light input signal and converts it into an electrical signal is a key component in the communication systems. In particular, a wide bandwidth, low noise receiver is needed in short distance applications, such as computer interconnects and local area networks. A common receiver design to meet these needs utilizes a metal-semiconductor-metal (MSM) photodetector and a FET-based transimpedance amplifier [1]. The major advantages of this approach is the compatibilty of MSMs with standard FET fabrication technology and the low intrinsic capacitance per unit area for MSMs. Using short-gatelength GaAs MESFETs, Harder et al. [2] have fabricated a receiver with a bandwidth of 5.2 GHz. Pseudomorphic AlGaAs/InGaAs/GaAs modulation-doped field effect transistors (MODFETs) with submicrometer gates have demonstrated excellent microwave and noise performance [3] Therefore, receivers incorporating these devices can be expected to better meet the desired properties of wide bandwidth and low noise. In this paper, we present our work on the fabrication and characterization of a photoreceiver design incorporating pseudomorphic MODFETs and an MSM operating at 0.85 μm wavelength.

The AlGaAs/InGaAs/GaAs MODFET heterostructure used in this work was grown using molecular beam epitaxy (MBE) on an undoped GaAs substrate. From the substrate up, the layer consisted of GaAs/AlAs superlattice followed by 1 μm GaAs MSM absorbing layer, a 500 Å $Al_xGa_{1-x}As$ graded to a 70 Å $Al_{0.35}Ga_{0.65}As$ MSM barrier enhancement layer, a 500 Å GaAs buffer layer, a 170 Å $In_{0.2}Ga_{0.8}As$ channel layer, 20 Å undoped $Al_{0.17}Ga_{0.83}As$ spacer layer, a Si planar-doping layer, 200 Å $Al_{0.17}Ga_{0.83}As$ layer, a 15 Å AlAs etch stop layer, and a 600 Å n^+-GaAs cap layer. The etch stop layer is to obtain uniform recess depth with either a selective wet chemical or reactive ion etching process [4]. The circuits were fabricated using a direct write electron beam lithography process for the mesa isolation, 0.25 μm T-gates, and SiN_x dielectric crossovers/passivation.

The receiver circuit is shown in Fig. 1 consists of an MSM and a transimpedance amplifier with all active components including a variable feedback resistor which is a common-base FET [5]. The dark current of an AlGaAs/GaAs MSM identical to the one used in the receiver is compared in Fig. 2 with devices fabricated on GaAs with and without SiN_x passivation. The passivated AlGaAs/GaAs MSM has the lowest dark current; this is expected to have an impact on the noise properties of the receiver. Discrete MODFETs exhibited dc g_m's over 500 mS/mm and f_t's of 70 GHz.The 3 dB bandwidth of the amplifier is measured to be 10 GHz at a transimpedance gain of 300 Ω resuling in a transimpedance-bandwidth product of 3 THz-Ω. At lower gains, 3-dB bandwidths as high as 14 GHz have been measured. Optical measurements conducted on the receiver indicate a receiver bandwidth up to 10 GHz as shown in Fig. 3. These results are among the highest ever reported for optoelectronic integrated circuits.

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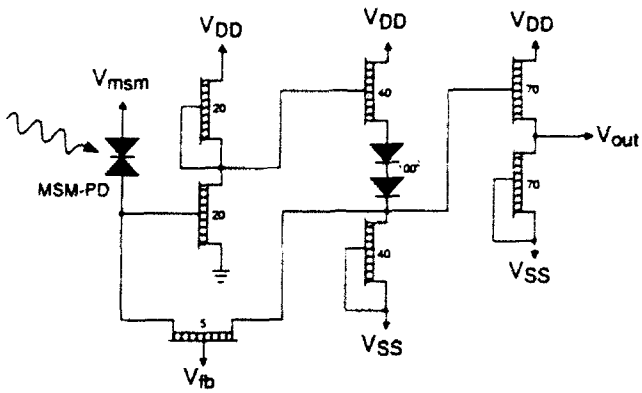


Fig. 1 Optoelectronic receiver circuit with an MSM and a transimpedance amplifier with an active feedback resistor.

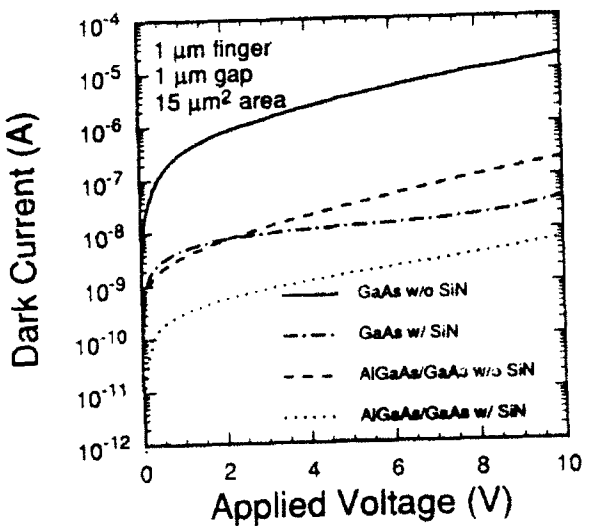


Fig. 2 Dark currents of MSMs fabricated on GaAs and AlGaAs/GaAs layers with and without SiNx passivation.

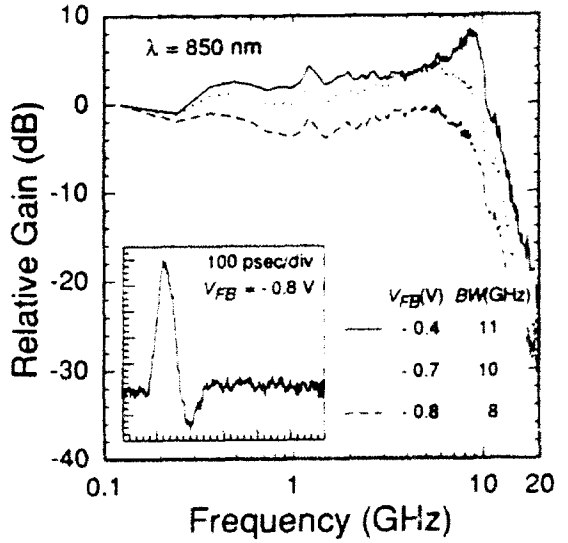


Fig. 3 The frequency response of the receiver obtained from optical measurements at 0.85 μm.

WD4

HIGH SENSITIVITY InGaAs MSM/HFET MULTI-STAGE INTEGRATED RECEIVER

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This article details our recent progress to monolithically integrate a long-wavelength photodetector with 3-stage FET-based transimpedance receiver. Our approach [1]-[2] uses lattice-matched InAlAs/InGaAs/InAlAs heterojunction FETs (HFETs), a schottky metal-semiconductor-metal InGaAs photodetector (MSM) on a InP semi-insulating substrate. The epitaxy is grown via MBE on 2-inch semi-insulating InP wafers. Figure 1 shows the cross section structure of the HFET and MSM detector. The HFET has a nominal 1 μm gate length. The depletion-mode HFETs have peak transconductance of 310 S/m and a nominal pinchoff threshold of -1.0 V. The HFET unity-gain cutoff frequency, an important figure of merit for receiver sensitivity, is shown in Figure 2. F_t ranges from 25 - 31 GHz wafer-to-wafer and, for the devices used for these receivers, was measured at 25 GHz (Figure 2). F_{max} is typically above 50 GHz for this process. The MSM detectors were 30 x 30 μm with 1.5 μm metal fingers and 3.0 μm spacing. For top-illuminated MSM detectors, the finger width/spacing is a tradeoff between bandwidth versus responsivity at a given bias voltage. The

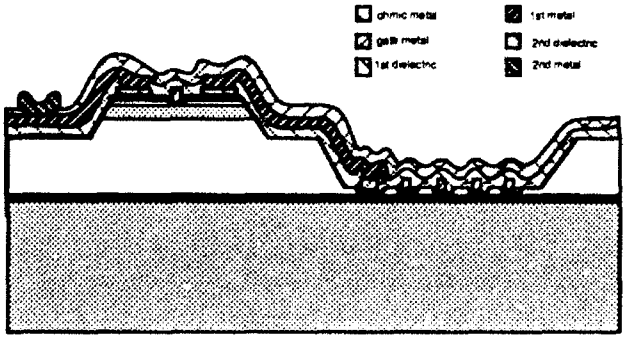


FIG. 1. OEIC receiver cross section of HFET and MSM detector.

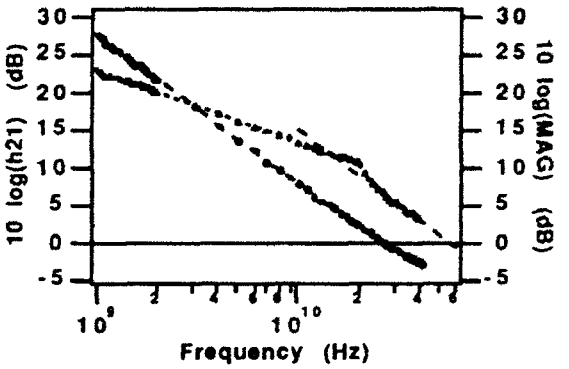


FIG. 2. Current and power gain for 1x100 μm HFETs.

MSMs for these receivers had a measured 3 dB (electrical) bandwidth of 1.1 GHz into 50 Ω at 5 V bias with a responsivity of 0.25 A/W at the 3 dB point. The dark current for the detectors was typically below 10-20 nA at 5 V.

The first stage receiver circuit schematic is shown in Figure 3. The design uses a cascoded transimpedance first stage, followed by two stages of post amplification, and a 50 Ω output stage. The feedback element is 1x5 μm FET with a separate gate bias line to control the feedback resistance. The various gain stages are dc coupled. Including the level-shift diodes, the 3-stage receiver has 70 HFET devices plus the MSM photodiode. To our knowledge, this

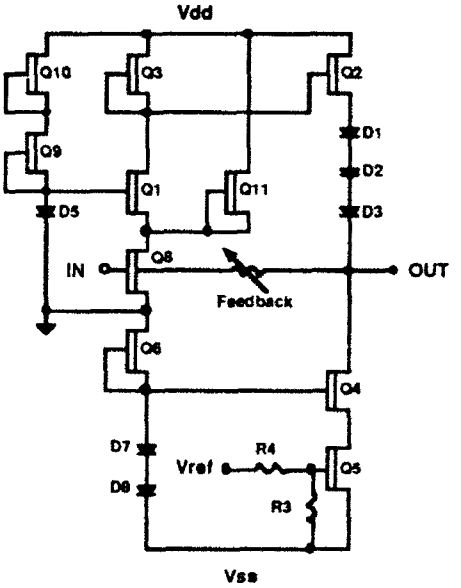


FIG. 3. Schematic of the transimpedance amplifier first stage with cascode.

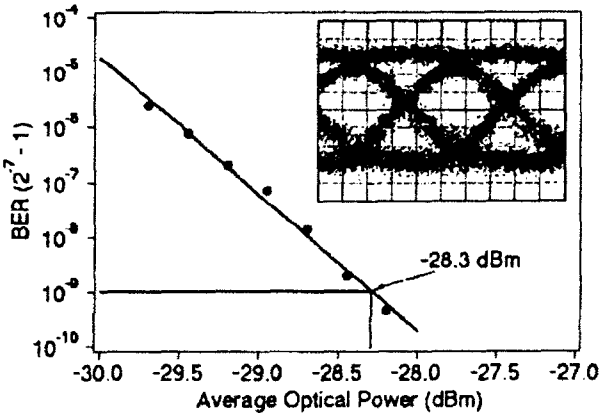


FIG. 4. Receiver senstivity at 1.2 Gbps. Inset shows the eye pattern at -24 dBm, 1.2 Gbps (10 mV/div).

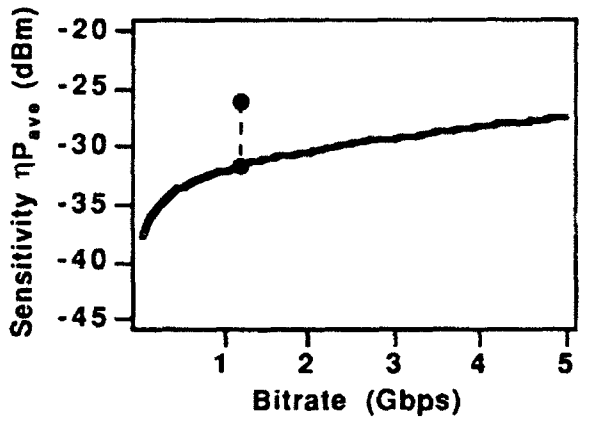


FIG. 5. Calculated receiver sensitivity as a function of bit rate for an ideal photodetector. Elevated point at 1.2 Gbps shows penalty for $\eta = 0.28$ MSM corresponding to *measured* sensitivity. The curve is calculated assuming 0.75 A/m gate leakage and 310 S/m transconductance from device measurments. The feedback resistance used was 2000 Ω and the total input capacitance was 0.2 pF, close to the actual reciver values. The receiver input HFET is 1x50 μm.

is the highest level of integration yet achieved for a monolithic receiver on InP.

The receiver sensitivity was measured using a directly modulated 1310 nm commercial laser. All measurements were made on-wafer with rf probes and using a microscope to focus the optical input onto the MSM detector. Figure 4 shows the bit error rate as a function of the average incident optical power. The pattern was pseudo-random with a word length of 2^7-1 bits. For 1.2 Gbps the receiver has a measured best-case sensitivity of -28.3 dBm (typical value across the wafer -26 dBm) with no post filtering or equalization. This result includes a correction for non-ideal laser extinction ratio for the directly modulated laser source. The receiver responsivity was 6000 V/W at 1.2 Gbps.

Figure 5 shows the expected sensitivity as a function of bit rate for these devices. The calculation was based on average *measured* values of the gate leakage, transconductance, and an estimated feedback resistance of 1800 Ω. The graph shows that the expected sensitivity at 1.2 Gbps for this receiver should be -26.2 dBm which is very close to the observed value. Although the best sensitivity is 2 dB better than predicted (Figure 5) this is primarily due to the device variations across the wafer. For this relatively low bit rate, the main constraints limiting the sensitivity are the input leakage current (from the input HFET gate) and thermal noise from the feedback resistor. At higher data rates noise from the input HFET channel would become more important. The graph shows that, if the external detector efficiency were improved, e.g. by using backside illumination, receivers using this process would be expected to approach -25 dBm at 5 Gbps.

In summary, we have fabricated a 3-stage, 70 active device, receiver with an integrated MSM detector on an InP substrate. We believe this is the largest monolithic receiver circuit built on InP. The best measured sensitivity, -28.3 dBm at 1.2 Gbps, is the best result to date for a receiver using a MSM.

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Thursday

August 6, 1992

ThA: PICs II

ThB: Components

ThC: PICs III

ThA1 InP BASED OPTOELECTRONIC INTEGRATED CIRCUITS FOR SUBSCRIBER ACCESS AND OTHER APPLICATIONS

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Abstract
We describe the fabrication and performance of high functionality OEICs (or PICs) for use in subscriber access systems. Devices incorporating DFB and DBR lasers, monitor diodes, waveguides and WDM components may be prepared using a common process technology.

Introduction.

Over recent years, the fabrication of OEICs (or PICs) as a route to achieving low cost, high functionality devices for local access links and other applications has received increased attention and a number of different routes for achieving laser-waveguide integration have been reported including butt, twin guide and contoured substrate [1,2,3,4] approaches. We have in particular explored the butt coupling approach which we believe offers a wider choice of active and passive sub-component device design and hence allows a more flexible approach to achieving the optimisation of different, multifunction OEICs.

Examples of device functionality

Two examples of OEICs [5,6] designed and fabricated at GMMT, Caswell, using a common, butt join process technology but serving different functions are shown in figures 1 and 2. In figure 1, a DFB laser is integrated with an unbalanced Mach-Zehnder wavelength duplexer and monitor diode to form the basis of a 1300/1530nm bi-directional link. Figure 2 shows a schematic of a narrow band add-drop optical multiplexer based on a DBR laser integrated with Bragg grating folded coupler within a Mach-Zehnder interferometer.

In the latter device, the Bragg and laser feedback gratings are fabricated at the same time and in the same waveguide material. Hence with the DBR approach, accurate matching of the laser and Bragg reflector operating wavelengths are assured. In the former device, a semi-insulating substrate design is used with polyimide bridged laser contact tracks and deep etched isolation slots to provide efficient electrical isolation between laser and monitor functions. Both device types may be prepared on either n-or semi-insulating substrates but the use of a semi-insulating substrate approach is seen as the most favourable approach for incorporating increased device functionality in future devices.

Outline of process technology and device results.

The OEICs described here are based on a common, butt join, selective area MOVPE growth approach employing buried ridge lasers (and monitor diodes) integrated with strip loaded waveguides. The butt join approach also allows alternative active and passive device designs to be used. Device fabrication is designed to be compatible with full 2 inch wafer processing and employs standard photolithography, etching and contacting techniques together with material and process tolerant designs for the active and passive components - in particular the novel coupler design [7]. The OEICs feature first and second order gratings produced by laser interference techniques on up to full 2 inch diameter wafers. E-beam techniques may also be used. Non-selective and selective wet etching is employed in non critical areas. However, extensive use is made of Methane/Hydrogen dry etching for critical process steps such as in forming the waveguide and laser stripes, and in forming the vertical sidewall isolation trenches in semi-insulating substrate design OEICs. The use of dry etching allows accurate process control and uniformity over large area wafers and leads to enhanced device yields.

Process steps are aimed to be self compatible, for example, devices similar to that shown figure 1 but, incorporating additional 3dB couplers for bidirectional 1300nm/uni directional 1530nm traffic, based on n-type substrates have been evaluated by GPT in the 1991/92 PON system field trials established by BT in Bishop's Stortford, UK. The same structures but based on the more advanced semi-insulating substrate design are currently being prepared. Higher functionality devices, allowing a further receive channel, by the addition of an add-drop wavelength multiplexer, are currently in progress.

Both bi-directional link and add-drop OEIC s have been successfully fabricated. Bi-directional link OEIC s have been prepared for both 1300 and 1530nm transmit wavelengths, with receive wavelengths of 1530 and 1300nm respectively. Network facet output powers of these devices were in excess of 6mW at 100mA drive current and threshold currents as low as 10mA. These relate to in excess of 300μW coupled power into monomode fibre at Ith + 20mA. The bandwidth of the add-drop wavelength multiplexers was in the range 2-3.5nm with a grating extinction ratio at the operating wavelength of >23dB. Chip through losses for both OEICs were as low as 2.5dB.

Summary

The fabrication and performance of different, multi functional InP based OEIC s using a common, butt join process technology has been described. The growth and process technology has been designed to be high yield and compatable with full 2 inch processing as a route to high volume manufacture. Different processes have been designed to be mutually compatable to allow 'building block' like manufacture of higher functionality devices in the future. This work was supported by, in part GPT LIMITED, and in part by RACE R1012 and R1064.

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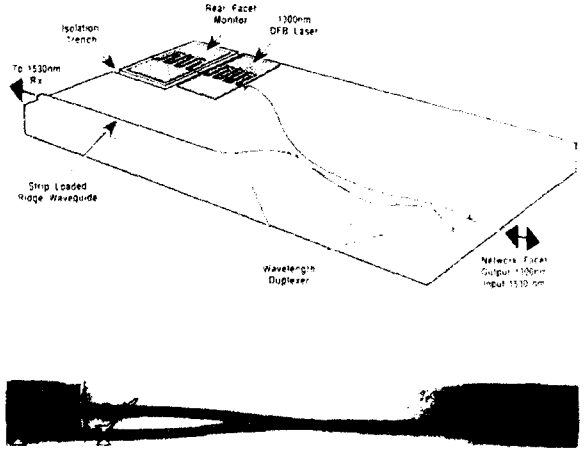


Figure 1

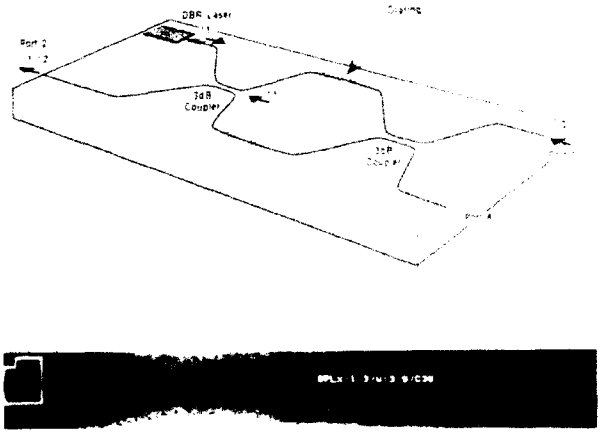


Figure 2

ThA2

LOW-LOSS, ULTRA-COMPACT MONOLITHIC INTEGRATION OF HIGH-SPEED POLARIZATION-DIVERSITY PHOTODETECTORS

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Polarization-selective optical devices are required for polarization-diversity coherent lightwave receivers.[1] Monolithic integration of such devices with photodetectors improves detector functionality and eliminates package complexity by reducing part count and hybrid optical interconnects. Compatibility with high III-V materials' cost, however, requires simple, high-yield processes and compact device size. We previously proposed a simple and compact integration scheme employing metal-loaded vertical couplers for polarization splitting and vertically-coupled photodiodes for O/E conversion. Initial experiments using InGaAsP/InP demonstrated satisfactory *optical* functionality, with 10.6 and 16dB polarization selectivity for TE and TM polarized-light.[2] Here we show how such integrated devices can be modified to achieve suitable *electronic* performance, including wide bandwidth and high quantum efficiency.

Fig. 1 shows a schematic of our device. Photosignals input via a laterally tapered rib waveguide are launched into a pair of coupler/photodetector units, each performing O/E conversion on orthogonal polarization states. The taper is essential for minimizing lateral diffraction in the couplers, to achieve high quantum efficiency with narrow diode mesas (28μm) suitable for high-speed operation. The near-adiabatic, parabolic taper[3] is 177μm long. We use vertical couplers to eliminate coupler gap lithography, reduce coupler length, and increase the optical bandwidth. Regrowth-free integration of short detectors (20μm TE, 34μm TM) is achieved by "impedance matched"[4] vertical coupling to *pin* mesa photodiodes. Metal loading of the first coupler causes phase-mismatch for TM-polarized light, so that only TE-polarized signals are coupled to the first photodiode, while the second coupler/detector pair captures the remaining TM-polarized light. Our design eliminates difficult-to-define lithographic features (coupler gaps, Y-junctions) and epitaxial regrowths. The small size (~400μm) and simple processing of this photonic circuit render it ideal for high yield fabrication.

Photodiodes were passivated with polyimide collars and connected to bond pads placed on the InP:Fe upper coupler cladding (not shown in fig. 1). Leakage was 8-11nA at -4V bias, primarily due to finite resistivity of the semi-insulating guides rather than the junction. Measured capacitance at -4V was 100, 142fF for the TE, TM detectors. A thin (1μm) *i*-InGaAs depletion layer was used to minimize photodiode nonplanarity; twofold capacitance reduction could be achieved with thicker *i*-layers without compromising detector performance. Diode series resistance ≈20Ω was estimated from S-parameter data.

On-chip optical insertion losses (photocurrent output/optical input) at λ=1.52μm were 1.5dB TE and 2.2dB TM. Detection quantum efficiencies of 42% TE and 35% TM, *including fiber input coupling*, were obtained using conical fiber tips. These values arise from on-chip losses plus 1.5dB Fresnel reflection plus 0.8dB input mismatch. Polarization selectivities were 12.7dB TE and 11.3dB TM; for these values, only ≈1dB total IF signal variation due to polarization fluctuation is expected in receiver applications. The bandwidth of the larger TM detectors was ≈13GHz into 50Ω at -8V bias, determined using microwave wafer probes (fig. 2).

R.J. Deri et al., "Low-loss, Ultra-Compact Monolithic Integration of..."

In summary, we have demonstrated compact photonic integration of polarization-diversity photodetectors with low insertion loss and high detection bandwidth. Our results show that such integration can enhance detector functionality, by incorporating high-performance waveguide optics, *without compromising chip size or ease of fabrication.*

This research was performed in part under the auspices of the U.S. Department of Energy by the Lawrence Livermore National Laboratory under contract W-7405-ENG-48.

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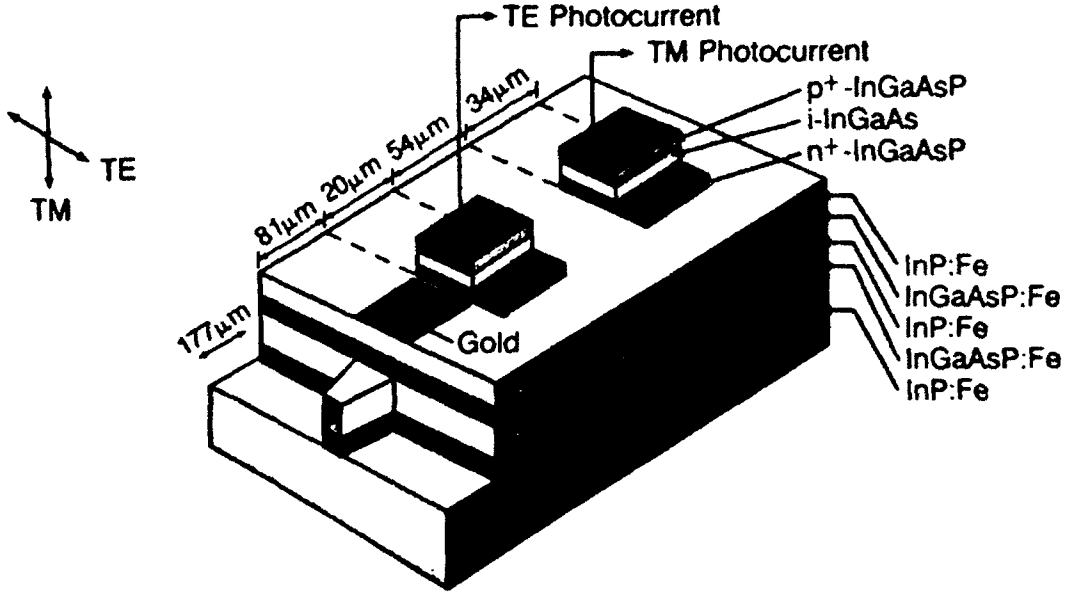


FIGURE 1: DEVICE SCHEMATIC. Detector passivation and interconnect metal not shown.

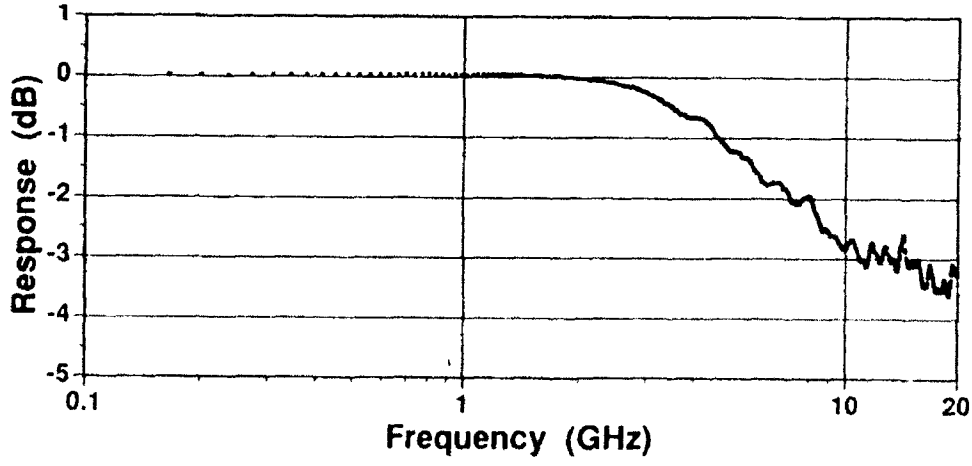


FIGURE 2: TM DETECTOR BANDWIDTH DATA.

ThA3

NOVEL MONOLITHIC INTEGRATION OF InGaAs-QW LASER AND INTRACAVITY ELECTROABSORPTION MODULATOR BY IMPURITY-INDUCED DISORDERING

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Monolithic integration of a semiconductor laser and an optical modulator is very useful for optoelectronic technology. Here we report on such an integration having novel structure using InGaAs/GaAs/AlGaAs QW (InGaAs-QW) material by impurity-induced disordering (IID).

For such an integration using GaAs/AlGaAs QW (GaAs-QW) material, it was found that the modal loss in the waveguide is so large that one has to shift the absorption edge of the non-active sections of the device, including the modulator and the passive waveguide connecting the modulator and the laser, toward shorter wavelength (blue shift) to make the non-active sections become semi-transparent. For this purpose, special treatment such as impurity-induced[1] or impurity-free[2] interdiffusion was employed on the non-active sections. However, this approach adds not only significant fabrication complexity, but also considerable free carrier loss[1] and/or scattering loss[1,2].

However, one might speculated that for InGaAs-QW material the blue shift in the non-active sections is not necessary. It is well known that compared with GaAs-QW material, strained InGaAs-QW material needs significantly lower current injection to become transparent. It then follows that the InGaAs-QW non-active sections, which are actually under optical pumping since they are next to the laser section of the device, would need significantly less photon flux to become transparent. This means that the effective modal loss of InGaAs-QW waveguide could be significantly lower than that of GaAs-QW waveguide. Therefore, for InGaAs-QW material the benefit of the blue shift may not compensate for the fabrication complexity *and* the free carrier and/or scattering loss incurred by the blue shift. If this hypothesis is correct, the monolithic integration of an InGaAs-QW laser and an electroabsorption modulator can be achieved using our well-defined fabrication technology for IID lasers.[3,4]

The fabrication procedure for the integration was exactly the same as that for our high-performance IID lasers.[3,4] except that the top contact consisted of non-continuous sections along the longitudinal direction. This fabrication procedure was considerably simpler than other processes reported.[1,2, 5-7] The finished device has an identical waveguide for both active and non-active sections, significantly different from the analogous integration made on GaAs-QW material.[1,2] The total length of the device was L=300 μm with laser length L_a=220 μm. The span separation and the electrical isolation between the laser and the modulator was 20 μm and ~1.5 kΩ, respectively. The device was put onto a Au-plated copper table with p-side up; no additional soldering and/or heat sinking were needed for testing operation.

Fig.1 shows the L-I characteristics of the device. The threshold current was 3.5 mA when the modulator was in parallel with the laser, and was 6.2 mA when the modulator was floated. This moderate increment of the threshold current was consistent with the results reported recently.[8] We believe that the moderate increment of the threshold current is the direct evidence that the

modal loss in the non-active sections of the device was relatively low. By cleaving regular lasers having different length, we have determined that the residual loss of the laser waveguide created by our processing on the material was 9.7 cm^{-1}. Further research is underway to determine the modal loss of the modulator.

Fig.2 shows the L-I characteristics of the device when the modulator was biased. As the *reverse* bias voltage (V_m) was increased, the threshold current of the device increased monotonically. This threshold increment was due to the electroabsorption induced by the reverse bias on the modulator. Note the abrupt turning on of the L-I characteristics which is the common feature of this kind of devices. From these L-I characteristics, one can see that when the bias voltage on the modulator was varied from 0.0 to -1.8 V while the current injection on the laser was fixed at 22 mA, the on-off ratio was larger than 17:1, normally on operation. Both the threshold value and the on-off ratio shown in Fig.1 and 2 are very promising results compared with other reports.[1,2,5-7] We expect significant improvements of this device performance upon optimizing the structure and the processing of the device.

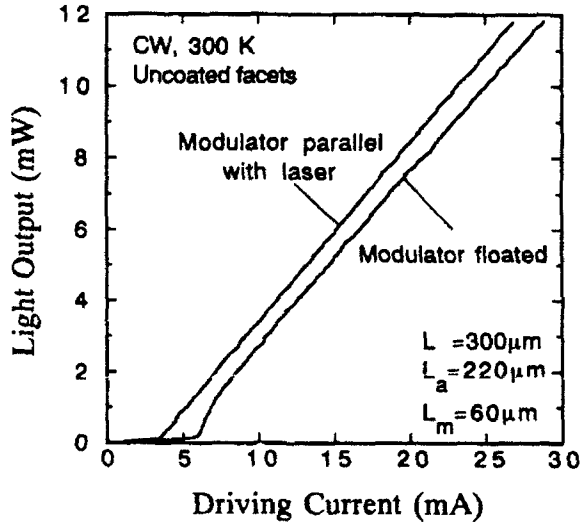


Fig.1 L-I characteristics of the device when the modulator was floated.

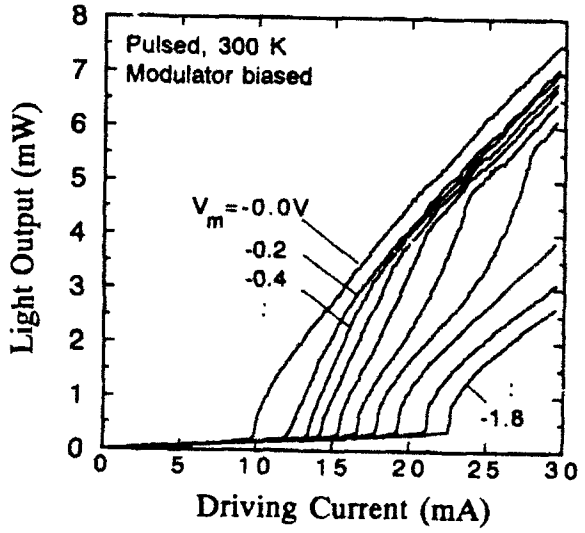


Fig.2 L-I characteristics of the device when the modulator was biased.

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ThA4 SELECTIVE REGROWTH OF A LOW REFLECTIVITY INTEGRATED OPTICAL PREAMPLIFIER

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Selective epitaxial growth is an extremely promising technique for the integration of photonic devices, such as lasers, photodetectors, and amplifiers on InP substrates. By simply patterning a dielectric layer, discrete devices can be combined into integrated photonic circuits with excellent electrical isolation. In this paper we demonstrate the first use of selective epitaxial growth to produce an off axis (tilted facet) integrated optical preamplifier (IOP). Optical preamplification, in which a signal is amplified optically prior to detection, has been shown to be more sensitive than electronic postamplification (i.e.pin-FET receivers) for wide band applications [1]. While monolithically integrated optical preamplifiers have been reported [2,3], none of these devices have had the required facet reflectivity (< -30 dB) and polarization balance (< 3 dB) over a wide optical bandwidth. In this paper the fabrication and performance of a tilted-facet integrated optical preamplifier grown by selective halide vapor phase epitaxy will be discussed. These devices have facet reflectivities of -36 dB, chip gains > 15 dB, and a difference in gain between TE and TM polarizations of < 3 dB.

The integrated optical preamplifiers were fabricated by selectively regrowing a 2.5μm wide p-InP ridge at 7° off axis to the 110 crystal plane, through a window opened in a dielectric mask, on an all n-type epitaxially grown base structure. Unlike the typical on axis results, the off-orientation growth causes stepwise reconstruction of the ridge sidewalls. Since the optical mode is isolated from the edges of the regrown mesa there are little or no scattering losses, as shown by the gain measured below. The base structure consists of an n+ InGaAsP guide layer 0.4μm thick, an undoped InGaAsP active layer 0.12μm thick and a n InP top cladding layer 0.1μm thick. Similar to [2], the p dopant (Zn) diffuses from the ridge into the InGaAsP active region. This forms and confines the pn junction to an area directly below the ridge, thus allowing for extremely low capacitance (and thus extremely high speed) devices. Active sections of 1000 μm (the amplifier) and 30 μm (the photodetector) were separated by 2 μm non-guiding regions (Figure 1). The capacitance of the photodetector was ≈ 0.2 pf, indicating that photodetector bandwidths in excess of 20 GHz can be obtained.

The chip gain was measured by using the entire device as an amplifier (i.e., forward biasing both amplifier and photodetector regions). Once the gain of the device is known, the effective facet reflectivity ($\sqrt{R_1 R_2}$ where R_1 and R_2 are the individual facet reflectivities) can be estimated from the gain ripple (Fig. 2), and was found to be -36 dB. An additional 11 dB in reduction of the facet reflectivity below the -25 dB, due to tilting the facet,was measured for these devices, and is due to absorption of the signal in the photodetector section. Since the reduction in facet reflectivity is independent of wavelength, the usable bandpass of the preamplifier extends over the entire spectrum of the amplifier (the 3dB optical bandwidth is 35 nm).

In summary, for the first time selective regrowth has been used to make tilted facet integrated optical preamplifiers. The device results demonstrate that selective epitaxial growth can be a powerful tool in the integration of optical devices, specifically those devices incorporating tilted or curved waveguides.

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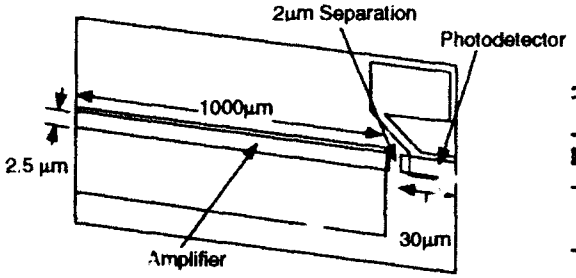


Fig. 1a

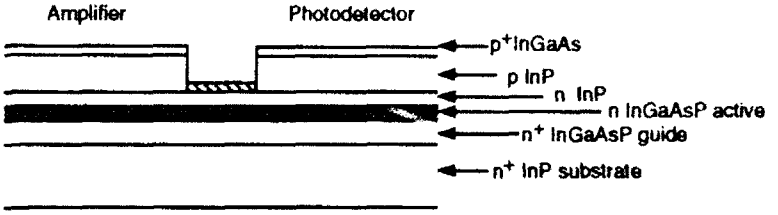


Fig. 1b

Figure 1. a) Schematic of an integrated optical preamplifier .
b) Schematic of a cross section through the amplifier and photodetector ridges.

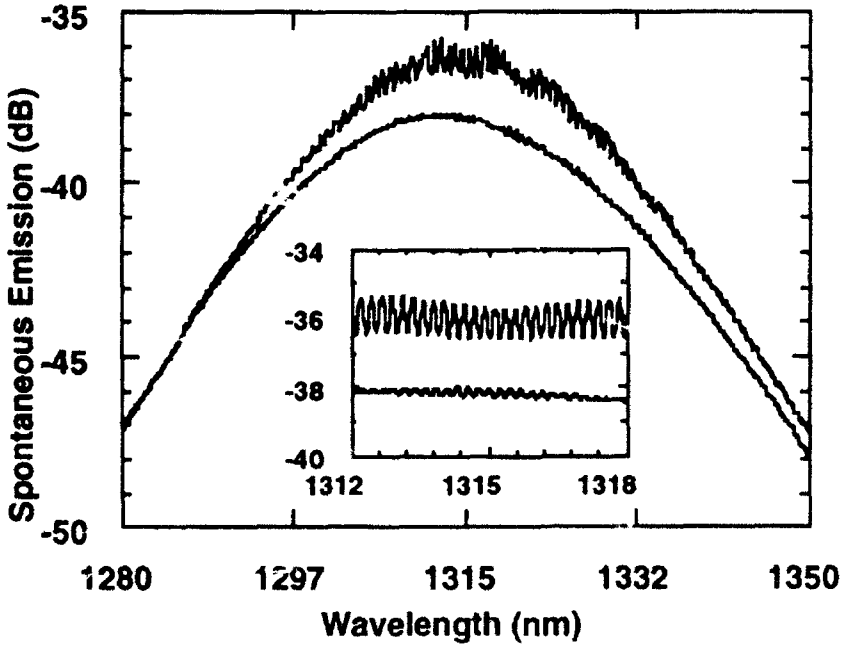


Figure 2. Amplified spontaneous emission spectrum of IOP with the photodetector forward biased, and with the photodetector unbiased.

ThB1 SELF-ALIGNED RIDGE GUIDE LASERS, MONOLITHIC LASER ARRAYS, AND PHOTONIC INTEGRATED CIRCUITS

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Integrated optoelectronic circuits using III-V material systems are attractive for their potential of high functionality [1], high speed [2-5], and low cost. The advantages of monolithic integration over hybrid packaging may become clear as more optical and electronic components are integrated in the future. The scale of optical integration, however, has remained small, while the number of transistors integrated has increased significantly. High density optical integration may require precise waveguide processing techniques and device structures that can simplify electrical interconnects. We report in this paper the use of a self-aligned-contact ridge guide structure [6] for low threshold DFB lasers, monolithic laser arrays, and the prospect of applications in photonic integrated circuits (PIC). This laser structure was also employed in a 5 Gb/s OEIC transmitter which we reported previously [5].

Semiconductor waveguides are commonly processed by either wet chemical etching or reactive ion etching (RIE). Selective wet etching using etch-stop layers is a powerful PIC processing technique, but the control of lateral waveguide dimensions may be poor. RIE permits accurate lateral definition but requires etch depth monitoring and may introduce electrical and optical damage to the etched surface. We show here the combined use of RIE and selective wet etching for precise process control and demonstrate its importance for waveguide analyses and device design for integration.

Figure 1a shows the structure of the self-aligned ridge guide laser. It is grown by MOVPE with an InGaAs/InGaAsP/InP separate confinement heterostructure, multiple quantum well (four wells) active region. The DFB laser has a first order grating and emits at 1.55μm wide wavelength. A 2.5μm AuZn/Au metal stripe is used for the p-side contact and as a self-aligned etching mask. RIE with a CH_4 and H_2 mixture, followed by selective wet etching of InP that stops at the InGaAsP layer is used to fabricate ridge guides of very low loss ($5cm^{-1}$). The most important result, however, is the well controlled MQW waveguide structure that permits us to calculate accurately the effective index and the Bragg wavelength for the integrated gratings. We were then able to match the Bragg wavelength with the quantum well gain peak to reproducibly fabricate DFB lasers of low thresholds, from 10 to 15 mA. Figure 1b shows the L-I curve of a typical DFB laser, which operates in a single mode with 40 dB side mode suppression.

As an example to demonstrate the use of the self-aligned-contact structure for high density integration, both Fabry-Perot laser arrays and DFB arrays of 1.5μm wavelength were fabricated. Figure 2a illustrates the schematic of a twelve-emitter array. The same RIE-wet etch method was used. All of the closely spaced (6μm center to center) ridge waveguides have vertical and flat side walls. The self-aligned AuZn/Au stripes can be used for individually accessing the 12 lasers. In the present experiment, the 12 emitters are electrically connected on top to form a high-power phase-locked array. The L-I curve in Fig. 2b shows output power of 0.45w from a FP laser array with uncoated facets under pulsed operation at 25°C. Phase locked DFB arrays (200 mA threshold) with single-line high power emission have also been demonstrated.

Straight waveguide PICs that consist of active-passive and active-active multiple sections have also been fabricated. The self-aligned metal stripe on top of the waveguide was chemically etched to introduce a higher than 5k ohm electrical isolation between integrated elements without affecting the waveguide continuity. Our results indicate that the self-aligned ridge guide may also be a useful structure for PICs.

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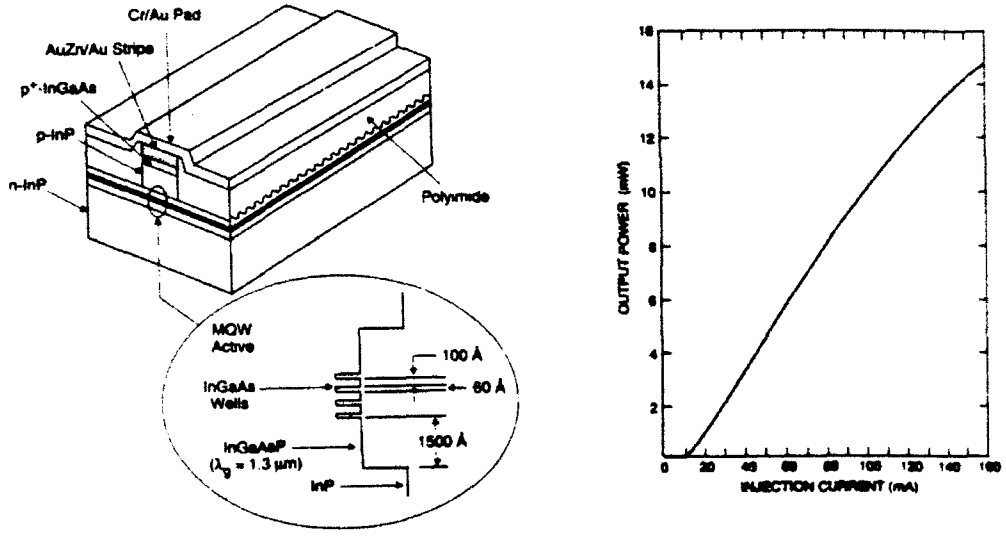


Figure 1 (a) schematic of a self-aligned-contact ridge guide laser, (b) L-I curve of a DFB laser under CW operation at room temperature.

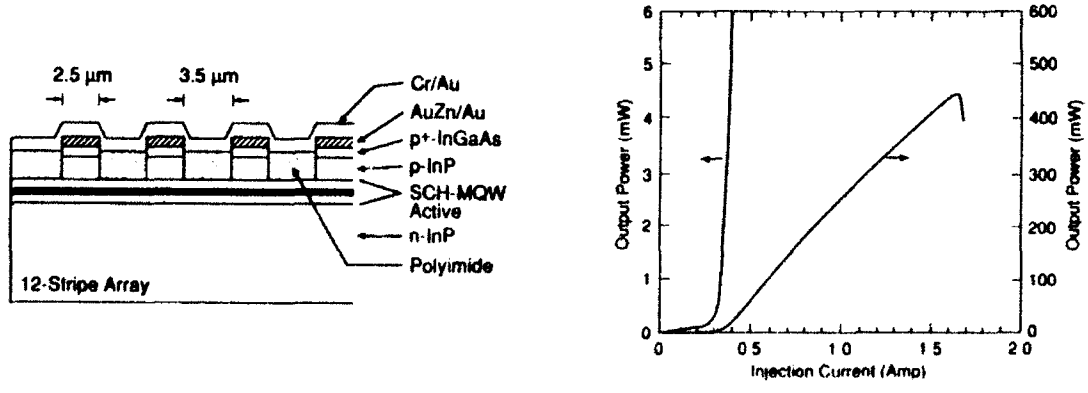


Figure 2 (a) Schematic of a monolithic 12-element laser array, (b) L-I curve of a high power FP laser array under room temperature pulsed operation.

ThB2

MONOLITHIC TWO-DIMENSIONAL SURFACE-EMITTING HORIZONTAL-CAVITY DIODE-LASER ARRAYS WITH UP TO 66% DIFFERENTIAL QUANTUM EFFICIENCIES*

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We report the fabrication of monolithic two-dimensional surface-emitting horizontal-cavity diode-laser arrays with low threshold current densities and high differential quantum efficiencies. In this work we investigated two types of arrays. The first used folded cavity lasers with two 45° internal deflecting mirrors and two top-surface facets,[1] while the second used etched vertical-facet lasers with external parabolic focusing/deflecting mirrors.[2] Optical pattern generator masks, optical projection printing, and chlorine ion-beam assisted etching were used in key fabrication steps.

The folded-cavity design is shown schematically in Fig. 1. The InGaAs/AlGaAs and AlInGaAs/AlGaAs structures were grown by organometallic vapor phase epitaxy (OMVPE) and contain a single InGaAs or AlInGaAs strained quantum well symmetrically positioned in an optical cavity. The laser emission wavelengths ranged from 980 to 790 nm, depending on the In and Al content of the well. Since total internal reflection occurs at the surface of the folding mirrors, high-reflectivity coating of the mirror surfaces is not required. Emission occurs through window regions in the top-surface facets at the ends of each laser element. More detailed descriptions of the array design[1] and laser structures[3,4] are provided in earlier work.

Figure 2 shows the pulsed (500-ns, 1-kHz repetition rate) near-field pattern taken at about twice threshold for a 584-element folded-cavity InGaAs/AlGaAs array consisting of eight rows of 73 elements each, all bonded in parallel. We expect this array to perform as well as smaller arrays reported earlier.[1] These AlInGaAs/AlGaAs and InGaAs/AlGaAs arrays (under 100 elements) were operated pulsed with differential quantum efficiencies over 50%, while the threshold current densities of individual laser elements were estimated to be in the 160 to 240 A cm^{-2} range.

Figure 3 shows the design with etched vertical-facet lasers and parabolic focusing/deflecting mirrors. The AlGaAs/AlGaAs structures used for these arrays were also grown by OMVPE and contain a single AlGaAs quantum well symmetrically positioned in an optical cavity. The emission wavelength was 804 nm. Maximizing collection efficiency at the parabolic deflectors is most important to overall array performance. Figure 4 is a scanning electron micrograph showing a parabolic deflector and etched laser facet. The etched curve is designed to optimize the *f*-number (design goal 0.8), taking into account the passivation and metal overlayers, the depth of the junction, and the tolerances in the lithography used to form the etch masks.

Figure 5 shows the pulsed near-field pattern taken at about twice threshold for a parabolic focusing/deflector array consisting of five rows of 75 elements each, all bonded in parallel. Smaller arrays were evaluated during pulsed and quasi-cw (100 μs at repetition rates up to 100 Hz) operation. The pulsed light output power vs current for a smaller array (3 rows of 24 elements each) fabricated simultaneously with the large array is shown in Fig. 6. This array exhibited a differential quantum efficiency of 63%. An array of 23 elements taken from the same chip as the large array was measured under quasi-cw conditions and found to have a differential quantum efficiency of 66%. All arrays had extrapolated laser threshold current densities in the 220 to 270 A cm^{-2} range.

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* This work was supported by the Department of the Air Force.

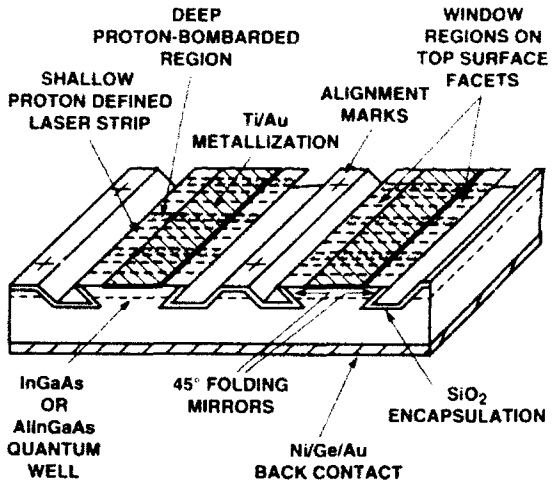


Figure 1. Schematic diagram of a monolithic two-dimensional surface-emitting folded-cavity array of strained-layer diode lasers.

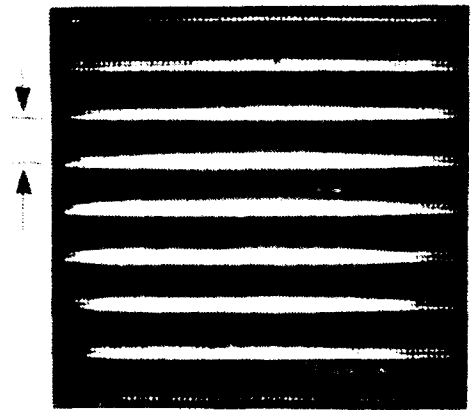


Figure 2. Near-field pattern of a 584-element InGaAs/AlGaAs folded-cavity array at about twice threshold.

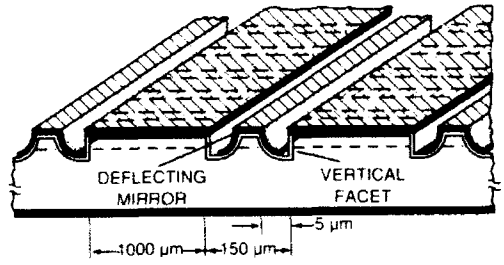


Figure 3. Schematic diagram of a monolithic two-dimensional surface-emitting parabolic focusing/deflecting mirror array.

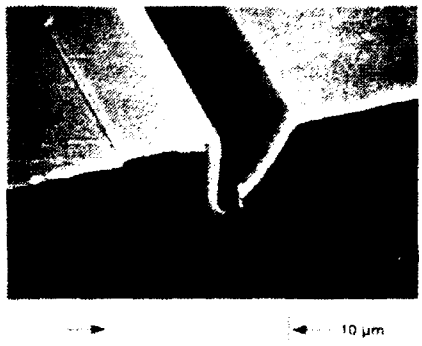


Figure 4. Scanning electron micrograph showing a portion of a vertical-etched facet and parabolic focusing/deflecting mirror.

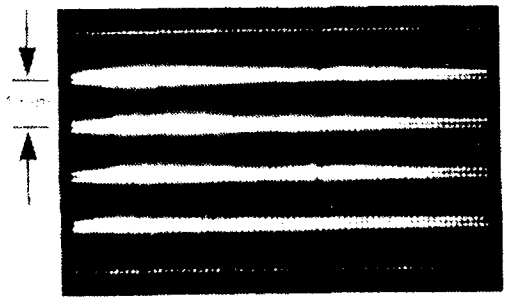


Figure 5. Near-field pattern of a 375-element AlGaAs parabolic focusing/deflecting mirror array at about twice threshold.

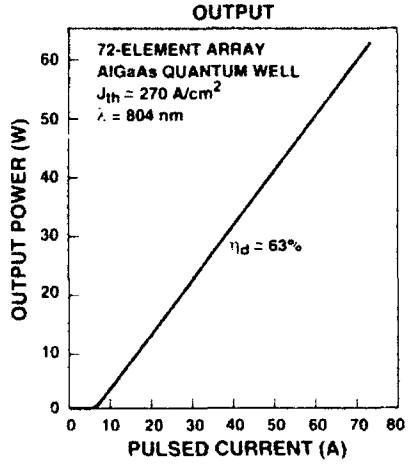


Figure 6. Pulsed light output power vs current for a 72-element AlGaAs parabolic focusing/deflecting mirror array.

ThB3

SELF-ALIGNED STARK-LADDER WAVEGUIDE COMPONENTS FOR OPTOELECTRONIC INTEGRATION

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Successful optoelectronic integrated circuits require active elements such as modulators and switches interconnected by low-loss passive components. The composition of the active elements usually introduces substantial loss per unit length over short lengths, making such material unacceptable for the longer interconnecting waveguide components. This loss is often dealt with in the passive interconnect regions with methods such as simply keeping the interconnects very short (not always possible), using impurity-induced disordering, etching back of the active material, or regrowing low-loss interconnect or active regions. We present work on a straightforward alternative approach that we are exploring for massive parallel optical processing which uses a coupled-quantum-well Stark-ladder material[1] (see fig. 1). Voltage-induced Stark-ladder modulation effects can be substantial even for photons well below the bandgap energy of the material for which the waveguide losses may be very small in the unbiased condition. The use of such material allows for the fabrication of useful active and passive waveguide elements from one waveguide material.

The MBE-grown waveguide material consists of a 0.25 μm thick $Al_{0.2}Ga_{0.8}As$ core region with $Al_{0.4}Ga_{0.6}As$ cladding layers of 0.5- and 1.25-μm thickness above and below the core region, respectively, on an N^+ GaAs substrate. Ten coupled quantum wells consisting of 2.5-nm GaAs wells with 2.5-nm $Al_{0.4}Ga_{0.6}As$ barriers (total thickness, 52.5 nm) are embedded in the waveguide core. The P-I-N structure is defined by P^+ and N^+ doping in the cladding layers above and below the core, respectively, and spaced 125 nm from the core region (to reduce free-carrier losses). A 50-nm P^+ GaAs capping layer is grown on top to passivate the $Al_{0.4}Ga_{0.6}As$. This structure has the attractive feature of an opaque substrate for a wavelength band at which the epitaxial waveguide transmits well, suppressing the substrate optical leakage path that might otherwise limit observed modulation depths and might otherwise allow a crosstalk pathway between waveguides. This consideration is particularly important for optical processing because a processing dynamic range greater than 50 dB is often required. Conventional metal lift-off processing was used to define 5-μm-wide gold-chrome contact stripes on top of the waveguide material. Contact pads were electrically coupled to the stripes with 10-μm stripe connections. This metalization was used as a self-aligned mask for the wet etching of a rib relief in the top cladding layer to provide lateral confinement of the propagating optical modes. Small breaks introduced along the 5-μm-wide metalization stripe and resultant localized etching away of the P^+ layer can be used to electrically isolate different sections of the optical waveguide for separate functions, with minimal effect on the optical properties in this self-aligned structure.

The waveguide components were characterized over a band of wavelengths from 777 to 810 nm by butt coupling a tunable titanium sapphire laser into the waveguides through a strain-free polarization-preserving 20× microscope objective. Modulation of transmission as a function of applied voltage is shown in figure 2 for a 2.2-mm-long waveguide for optical polarization parallel to the layers for several test wavelengths. The observed prominent peak in each curve is in good agreement with the calculated energy of the n = −3 heavy-hole transition in the superlattice[1] (see fig. 1). The maximum modulation of 50 dB was observed at a wavelength of 785 nm. The maximum modulation slope was 170 dB/Vcm. Similar results were obtained for the polarization perpendicular to the layers, but with a shift in the location of the observed peak feature. This peak shift is expected since only electron-light-hole transitions are expected for this polarization. The observed planar waveguide loss is as small as 10 cm^{-1}, which is still quite large for waveguide interconnect components. However, the MBE growth of a similar waveguide structure in which the uniform alloy regions were replaced with analogous $GaAs/Al_xGa_{1-x}As$ superlattice composites provided higher quality waveguides in which the planar waveguide losses were reduced to 1 cm^{-1} or less at zero bias. Rib waveguide losses of less than 2 cm^{-1} were observed in this modified structure. Work is under way to further reduce these waveguide losses and optimize modulator

performance. The length of the modulator necessarily limits device speed, but this may be outweighed in some massively parallel optical processing applications by ease of integration and achievable dynamic range.

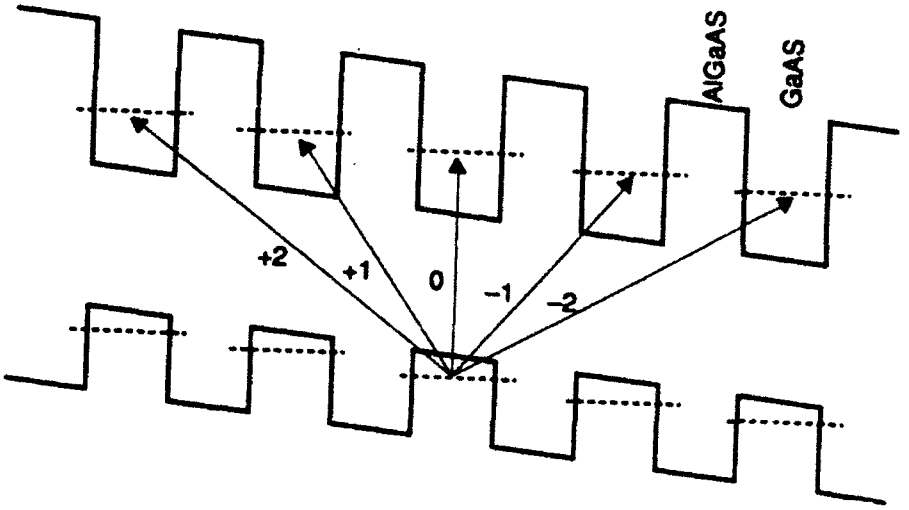


Figure 1. Stark-ladder interband transitions in a coupled-quantum-well superlattice.

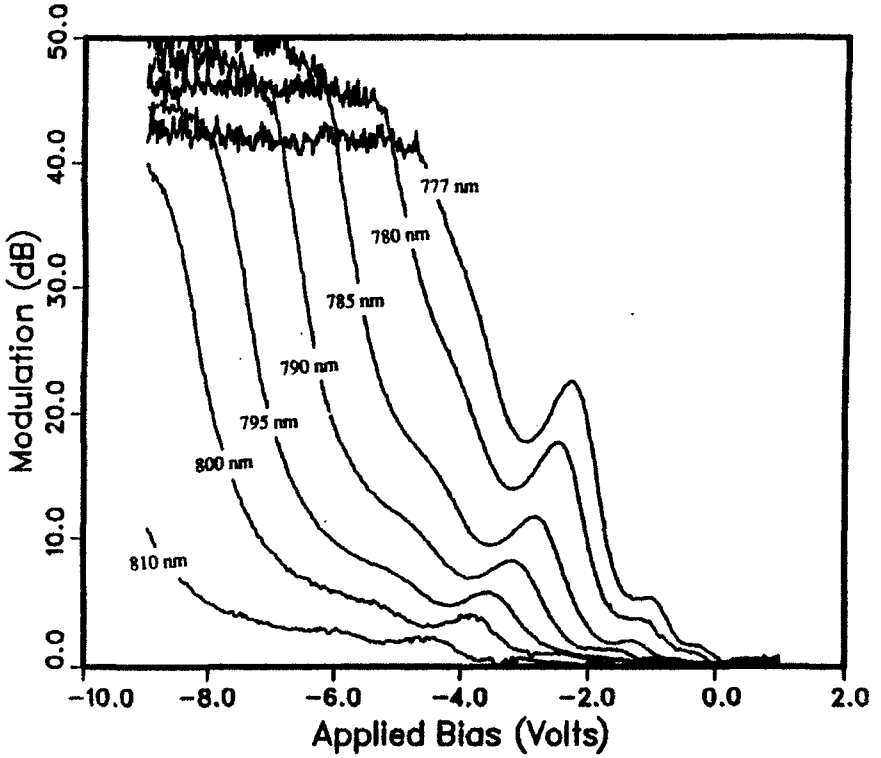


Figure 2. Modulation of transmission of a 2.2-mm-long Stark-ladder waveguide relative to zero-bias condition as a function of applied bias for optical polarization parallel to the layers.

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ThB4

THERMAL EFFECTS IN MONOLITHICALLY INTEGRATED TWO-DIMENSIONAL ARRAYS OF ETCHED-WELL SURFACE-EMITTING DIODE LASERS

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In spite of the remarkable progress achieved over the last two years, the performance and integration scale of vertical-cavity surface-emitting lasers (VCSELs) continues to be seriously limited by their thermal behavior. To date, VCSEL arrays can be operated only if the array elements are excited sequentially, one at a time. In this paper we present results of the first comprehensive thermal analysis of individually addressable two-dimensional (2D) arrays of VCSELs.

The analysis incorporates a new self-consistent thermal-electrical model of VCSELs, featuring a realistic distribution of heat sources and 2D current- and heat-flux spreading[1]. Interactions with all neighbors (near and distant) are included, applying the superposition principle combined with Kirchhoff transformation. Self-consistent solution is found by numerical iteration, taking into account temperature-dependence of device parameters.

Due to symmetry of quadratic arrays, it is sufficient to consider a single octant of non-equivalent emitters, contained between a principal diagonal and a major axis parallel to the array side. Within a single loop of self-consistent solution, contributions from all neighbors are added to individual temperature profile of each element of the octant. All elements are therefore treated simultaneously, with the center element used to test the self-consistency condition.

The arrays under consideration consist of double-heterojunction GaAs/AlGaAs etched-well VCSELs mounted *p*-side down, with lasing radiation collected through openings etched in the substrate[2]. Here, we give examples of two types of square ($N \times N$) arrays: typical-size arrays (active-region diameter $D = 10$ μm, center-to center spacing $S = 20$ μm) and closely spaced arrays of small-size emitters ($D = 4$ μm, $S = 6$ μm) that might be considered as candidates for phase-locked arrays. For brevity, these arrays are designated as 10/20 and 4/6.

Fig. 1 shows calculated temperature profiles for 10/20 arrays at twice the pulsed threshold,

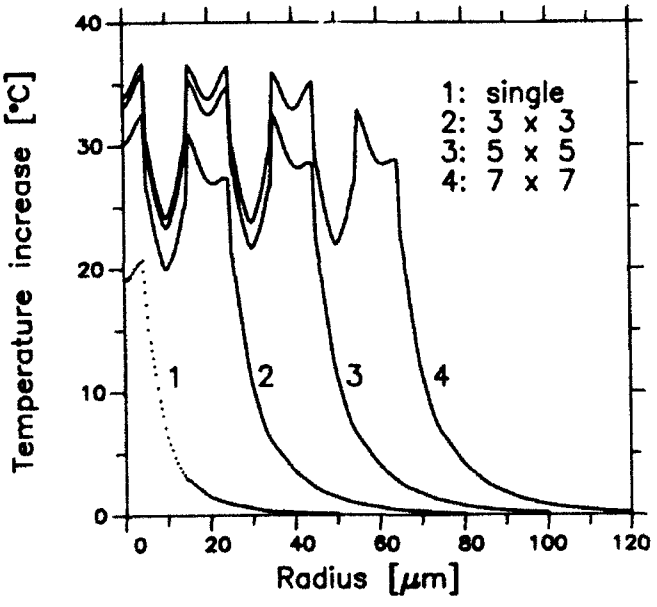


Fig. 1. Distributions of temperature profiles in the GaAs layer containing the active region in arrays of etched-well VCSELs ($D = 10$ μm, $S = 20$ μm) driven at $I = 2I_{th,p}$. Dotted line - temperature profile of a single emitter.

taken along a bisecting line parallel to the array side. For comparison, the temperature profile of a single emitter is also shown. It is clear that even at a relatively low current thermal crosstalk effects are very severe. In addition to an overall increase of active-region temperature throughout the array, temperatures of individual emitters can differ by as much as 10 °C for a 7 × 7 array (central and corner elements, not shown in Fig. 1). Characteristic nonuniform temperature profiles of single emitters[3] become skewed in 2D arrays. Emitters located at the edges of the array experience the strongest asymmetry. Breakdown of cylindrical symmetry may be especially important for phase-locked arrays as it opens up a new possibility of thermally engineered asymmetric waveguides/antiguides that could in principle enhance the in-phase operation of the array, in a way analogous to asymmetric ("chirped") linear arrays[4]. Lack of azimuthal symmetry in the central element of the array offers a promise of polarization control, analogously to polarization-maintaining optical fibers[5].

Thermal crosstalk problems are considerably more acute for 4/6 arrays (see Fig. 2). The relative temperature of the central emitter (with respect to the heat-sink maintained at 300 K) increases from ~7 °C for a single emitter to ~32 °C for a 7 × 7 array. The center-to-corner temperature gradient in the 7 × 7 array is as large as 15 °C.

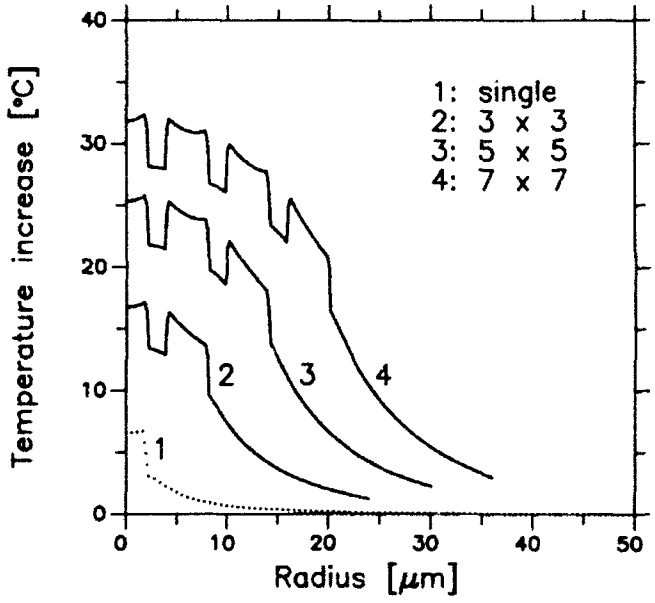


Fig. 2. Distributions of temperature profiles in the GaAs layer containing the active region in arrays of etched-well VCSELs (D = 4 μm, S = 6 μm) driven at $I = 2I_{th,p}$. Dotted line - temperature profile of a single emitter.

Our results indicate that thermal crosstalk represents a severe problem in individually addressable 2D etched-well VCSEL arrays with high packing density. On the other hand, thermal effects can be utilized constructively to influence supermode selection in phase-locked arrays, where all emitters are excited simultaneously.

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ThB5 REDUCING THE EFFECTS OF TEMPERATURE ON THE THRESHOLD CURRENT OF VERTICAL-CAVITY SURFACE-EMITTING LASERS

by
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In integrated optoelectronic applications, the issue of how excess heating affects the performance of on-chip light sources is of very practical concern. For example, thermal cross-talk can create drifts in the threshold current of on-chip lasers, which in the extreme case would need to be compensated for by complex driver circuitry. Reducing or eliminating the threshold drift with temperature would lead to simpler, more reliable designs. Vertical Cavity Surface-Emitting Lasers (VCSEL's) are becoming increasingly attractive alternatives to standard in-plane lasers (IPL's) in integrated optoelectronic applications due to their inherent small size and "no-cleave" cavity design. In addition, for applications requiring coupling to optical fibers and other "small" components, VCSEL's have clear advantages due to their fiber-compatible output beams which require minimal (if any) focusing optics. Thus, with VCSEL's moving into the spotlight, it is important that we begin to characterize, understand, and attempt to optimize, if possible, the temperature-related performance of VCSEL's. In this work, we specifically address the issue of miminizing the drift of the threshold current with temperature.

The behavior of the threshold current with temperature in a VCSEL is distinctly different from that in a standard IPL, due to the dramatic difference in cavity lengths. In an IPL, as temperature increases, the laser can track the shifting gain peak by *hopping* successively across the closely spaced longitudinal modes of the cavity. In this way, the minimum threshold current for a given temperature is always maintained. In addition, the threshold current increases exponentially simply because the gain peak decreases ~exponentially with temperature for a given current. In a VCSEL, the lasing mode is locked to the one single longitudinal mode of the cavity which exists within the gain bandwidth. Thus, as temperature increases and the gain peak shifts, the lasing mode will effectively scan across the gain spectrum, shifting through the gain peak toward higher energies (relative to the gain spectrum). Therefore, the threshold current in a VCSEL as a function of temperature is expected to reach a minimum near the temperature at which resonance between the lasing mode and the gain peak occurs (as illustrated in Fig.1, the actual minimum occurs at a temperature slightly lower than the "resonant" temperature since the gain peak is falling exponentially with increasing temperature).

Experiments we have performed on strained InGaAs/GaAs quantum well substrate-emitting VCSEL's [1] have demonstrated this interesting behavior, shown by the dots in Fig.2. Other researchers have also observed this effect [2]. From our experimental results, we see that the threshold current remains essentially flat over a range of ~30°C. This unique characteristic of VCSEL's has exciting ramifications for applications where threshold drift could create problems, for example, with on-chip driver circuitry.

While a 30°C temperature-insensitive range is useful, it would be worthwhile to explore ways in which we could extend this range further. For this we have developed a new theoretical model which is based upon gain calculations [3] of InGaAs/GaAs quantum wells. These calculations take into account the complex valence subband-mixing effects, which are essential to estimating

the effects of strain on the performance of quantum well gain. Using this model, we have simulated the effects of temperature on the threshold current of the above mentioned VCSEL, shown by the solid curve in Fig.2. The details of the simulation will be discussed more thoroughly in the talk. As can be seen, the agreement between theory and experiment is relatively good.

To broaden the minimum in the curve, we require the gain spectrum near the gain peak to be flatter with a wider range over which there exists a gentle slope increasing toward higher energies. Using the theoretical model, we have explored a number of ways of accomplishing this including: (1) varying the quantum well width to change the energy spacing between the first and second quantum states, (2) using different width quantum wells in a multi-quantum well active region to stagger the gain spectrums of the individual quantum wells, and (3) using bulk material as the active region. We find that improvements over the behavior shown in Fig.2 can be obtained with proper active region and cavity design, which could be important for applications where thermal cross-talk and threshold drift are of concern.

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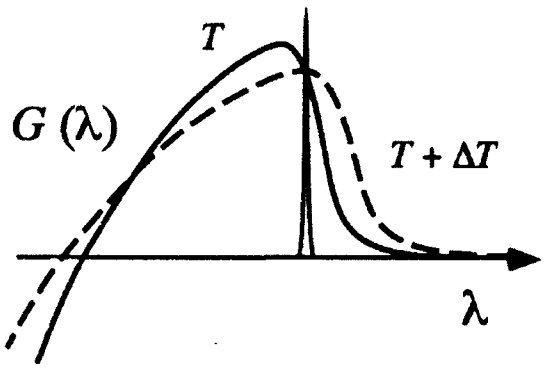


Figure 1 - Illustration of how the gain remains constant (for a given current) as temperature is increased if the lasing mode is positioned correctly. For this case, the effects of the shifting and flattening of the gain spectrum cancel each other out.

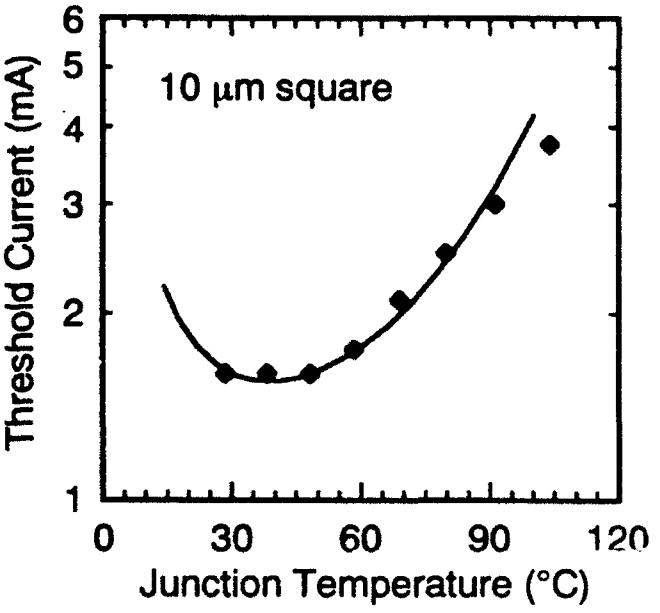


Figure 2 - Threhold current as a function of temperature for an $In_{0.2}Ga_{0.8}As/GaAs$ 3 QW VCSEL. The solid curve is a theoretical fit to the experimental data shown by the dots.

ThC1 INTEGRATED OPTICAL TRANSMITTERS AND RECEIVERS USING MULTI-SEGMENT LASER PROCESSES

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Research on integrated optical devices has often focussed on complex structures and complicated processing techniques [1,2]. However, a variety of integrated optoelectronic devices can be fabricated from a simple semiconductor laser diode waveguide process. Several important functional components can be obtained by splitting the top contact in a laser process into several segments allowing for non-uniform pumping. When forward biased, the device has gain allowing for amplification, direct current modulation of the gain, and modulation of the index of refraction. When reverse biased, the segment functions as a p-i-n photodetector, saturable absorber, and electro-absorption modulator. With these simple functions, many useful integrated optoelectronic devices can be formed. Figures 1a and 1b show example transmitter and receiver devices which have been fabricated with our process.

Figure 1a shows a three-segment monolithic cavity mode-locked semiconductor laser [3] with a waveguide saturable absorber, gain modulation segment, and gain segment. Devices with repetition rates as low as 5.5 GHz (7mm device length) and as high as 80 GHz (0.5 mm device length) have been fabricated. Figure 2 shows an autocorrelation trace for a 1.55 μm wavelength monolithic cavity mode-locked laser operating at a repetition rate of 21 GHz. Device structures similar to that of Figure 1a have been used for a 3-section gain-switched laser in which two saturable absorbers near the laser facets are used to obtain shorter pulsewidths than are possible with single-section gain-switched lasers. The device of Figure 1a can also be used as a two-segment superluminescent LED. A short reverse-biased segment acts as an optical termination to absorb spontaneous emission in one direction with a power reflection coefficient below 10^{-4}. The reverse-biased optical termination segment also serves to monitor average power from the superluminescent LED.

Figure 1b shows a 3 segment pre-amplified photodetector in which one segment is used as an optical amplifier, the second segment is used as a switch to turn the signal to the detector on or off, and the third segment is the p-i-n photodetector. Figure 3 shows the impulse response of the waveguide photodetector with a mode-locked semiconductor laser as the pulse source. The full width at half of maximum is 33 ps limited by the capacitance of the photodetector. The switching segment can be turned on and off in 200 ps using a step-recovery diode drive signal. The switching segment can also be used as a saturable absorber in pulse amplification applications. The entire spontaneous emission output from the amplifier does not reach the photodetector between optical pulses. Pump-probe measurements of the saturable absorber section were made to measure the absorption recovery time constant. The saturable absorber can recover to the highly attenuating state in less than 10 ps after the passage of the optical pulse through the absorber demonstrating that the saturable absorber can be effective in reducing the spontaneous emission reaching the photodetector.

An outline of a low capacitance multi-segment laser process is shown in Figure 4. A silicon nitride layer is deposited and patterned to outline the waveguide. The silicon nitride is used as an etch mask to define the waveguide for wet or dry chemical etching. Next, a polyimide layer is deposited and cured. In order to planarize the polyimide layer, a thick layer of photoresist is spun over the entire wafer. Both the polyimide and the photoresist layers are then etched in an oxygen plasma until the top of the mesa slightly protrudes through the polyimide layer. The silicon nitride layer is then removed and the wafer is ready for metallization. The multi-segment p-metal is evaporated, lifted off and annealed. The metal contacts are used as a 3-way self-aligned mask to 1) etch the contact layer between electrodes, 2) etch cleave marks for precise positioning of facet cleaves, and 3) remove the excess polyimide in order to promote good facet cleaving. Finally, the wafer is thinned, a backside metal is deposited and the devices are cleaved.

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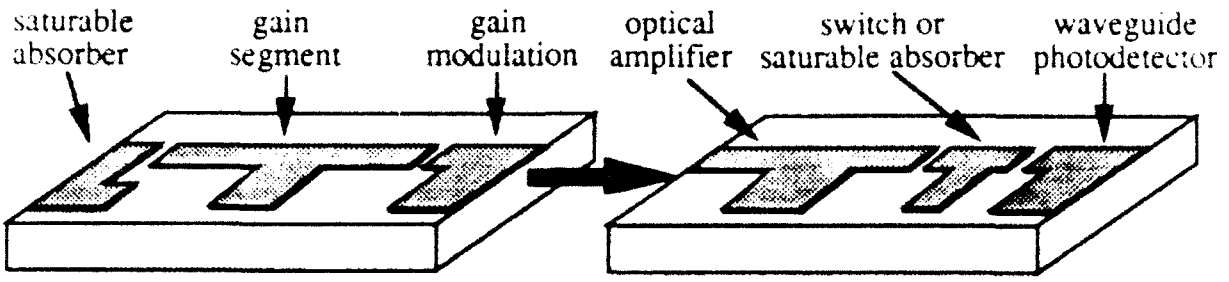


Fig. 1a. 3-section monolithic cavity mode-locked laser

Fig.1b: 3-section preamplified photodetector with switching segment and saturable absorber

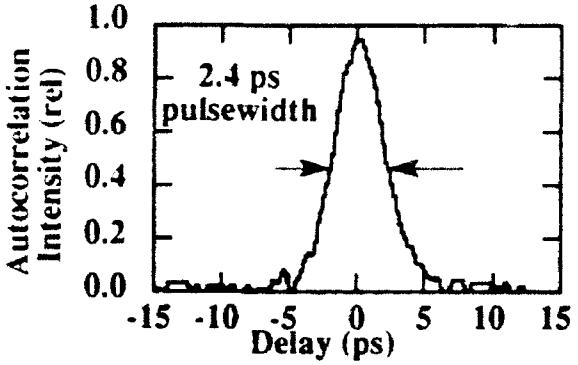


Fig. 2. Mode-locked laser autocorrelation

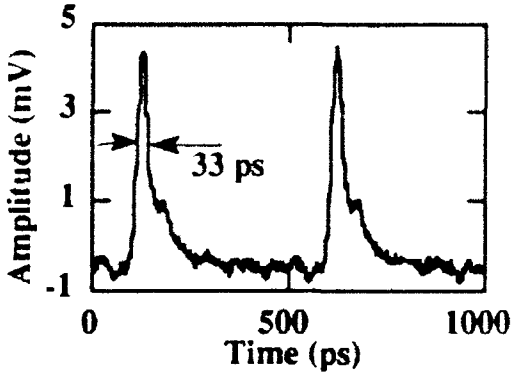


Fig. 3. Waveguide photodetector response

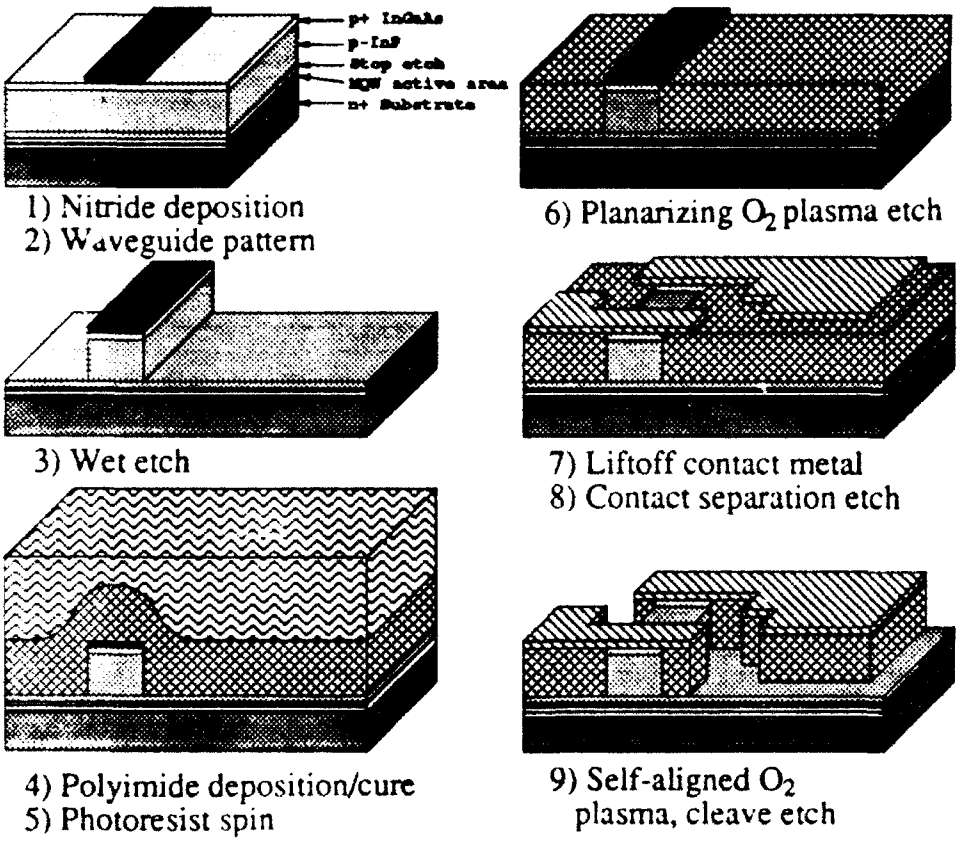


Fig. 4 . Low capacitance multi-section integration process

ThC2

PROGRESS ON THE DESIGN AND FABRICATION OF A NOVEL DIRECT-DIGITAL OPTICAL PHASE MODULATOR

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The direct-digital optical phase modulator is a key element in a photonic integrated circuit called COMPASS,[1](Coherent Optical Monolithic Phased-Array Steering System). This circuit can be used to control large phased-array microwave antennas. Steering such an antenna requires highly linear digital phase control of the individual emitters to produce the appropriate far-field radiation pattern. A fully digital, inherently linear, segmented, optical waveguide phase modulator was announced earlier this year.[2] This design uses the additive properties of phase delay along the length of a waveguide-type pn-junction to distribute phase delay between N individual elements or bits. The total phase delay is the sum of the individual delays. If the length of the bits is increased in a binary way, such that each bit is twice the length of the previous, then a direct digital phase modulator is achieved. The electrical bias value applied to each bit is also binary (0 or1), so that either V_0 or V_0+V_1 is applied. Therefore the operation of the device should be fully linear, within the accuracy of photolithography.

In the first fabrication of this device, no attempt was made to electrically isolate the bits. The result was that current spreading between the elements caused them to appear longer than their geometric length.

In this design,(Fig. 1) three methods are used to separate the device. These are: (1) mesa isolation ; (2) proton ion-implantation ; and (3) insertion of a common ground guard-band between each bit. In the first method, modulator segments are isolated from other devices and the surrounding material by means of an etched mesa. The mesa is 18 μm wide, or about 5 μm/side bigger than the metal p-contact over the waveguide. This limits the spreading current in the lateral direction, perpendicular to the waveguide. In the second method, a proton ion implant is performed at the perimeter of each bit. The implant mask brings the protons within 3 μm of the p-contact metal. The implant dose is $5x10^{13}/cm^2$ at 25KeV for mass 2. This dose and energy is sufficient to increase the resistance of the AlGaAs cladding layer, without disturbing the waveguiding properties of the pn-junction waveguide. The last separation method, ground guard-bands between each bit, greatly reduce the inter-bit spreading resistance. The details of this technique can be seen in Figure.2. Full isolation data will be presented.

This device is fully packaged, using polarization -preserving fiber and polarization preserving connectors. It has been tested in a fiber Mach-Zehnder test fixture. This test allows for complete information on the operation of each

bit. Data will be presented on phase linearity, Figure of Merit,(in degrees/volt-mm) Vπ, and frequency response.

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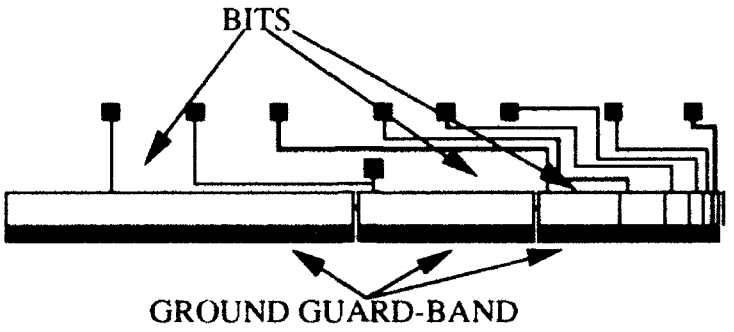


Fig. 1 Improved 8-Bit Digital Phase Modulator

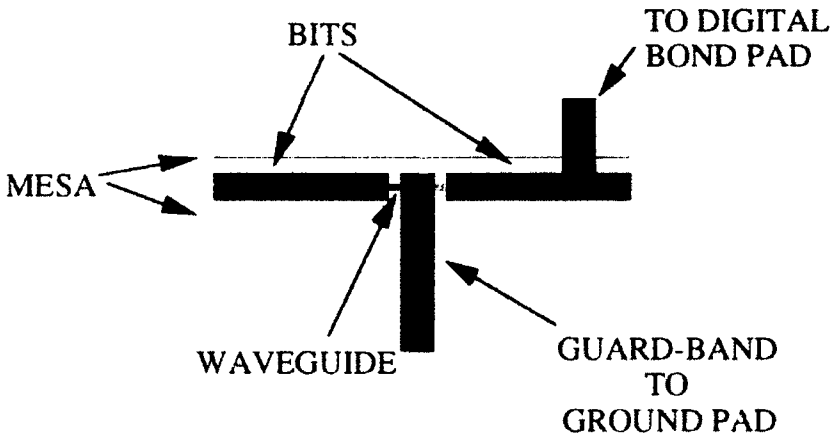


Fig. 2 Detail of 8-Bit Digital Phase Modulator

ThC3 TAPERED WAVEGUIDE INTERCONNECT BY ZINC DIFFUSION INDUCED LAYER DISORDERING OF QUANTUM WELLS

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Summary

Introduction :

Impurity induced layer disordering (IILD) of quantum wells has received considerable attention recently in the integration of optoelectronic devices, as it eliminates the need for regrowth in the fabrication process. Integration of various optoelectronic components on a single chip requires not only the tailoring of band gap energies of various components at different locations on the chip but also interconnecting various devices of different mode sizes. In this paper we demonstrate a novel waveguide taper transition where the energy from a multi quantum well (MQW) waveguide is coupled to a single quantum well (SQW) waveguide. IILD using zinc diffusion through a tapered SiO_x mask has been used for the fabrication of the taper.

The multi-to-single quantum well waveguide taper :

The taper interconnects a MQW waveguide and a SQW waveguide. The MQW waveguide consists of a guiding region of 15 pairs of 19 nm thick $Al_{0.35}Ga_{0.65}As$ barriers with 6.5 nm thick GaAs wells, surrounded by a cladding region of $Al_{0.22}Ga_{0.78}As$, on either side. It is a symmetrical waveguide with a 1.26 μm wide guiding region with an effective index of 3.586, a cladding index of 3.527, and a V number of approximately 5.73. The guide is designed to support the fundamental and the first order mode so as to help us identify the mode of the MQW guide besides its physical location by the identification of the energy in the mode. The SQW waveguide (n_{GaAs} = 3.619, n_{cl} = 3.527) was designed to be a weakly guiding structure whose evanescent tails effectively overlap that of the well guided modes of the MQW waveguide. The taper is achieved by disordering a section of the MQW region and tapering it gradually to the undisordered region so that the effective index of the tapered region increases gradually from 3.527 to 3.586.

Epitaxial growth of the SQW and the MQW waveguide sections, in addition to the necessary buffer and cap layers, illustrated in Fig. 1, was performed in a single growth sequence in an atmospheric pressure Metalorganic Chemical Vapor Deposition (MOCVD) system at a temperature of 725° C using TMG, TMA and AsH_3 as the precursors. The free carrier concentration of the unintentionally doped layers was $\sim 5 \times 10^{15}$ cm^{-3} ,obtained from C-V measurements. A typical low temperature photoluminescence (PL) spectrum is shown in Fig.2. It is dominated by the transitions related to the $Al_{0.22}Ga_{0.78}As$ cladding and the 6.5nm GaAs/19nm $Al_{0.35}Ga_{0.65}As$ MQW. The longer wavelength peaks are related to the GaAs/$Al_{0.22}Ga_{0.78}As$ SQW, GaAs bulk and dopant related peaks such as carbon and selenium.

The process of taper fabrication consists of (a) deposition of a SiO_x layer with thickness varying linearly from 80nm to 320nm, (b) sputter deposition of 320 nm ZnO/Zn, (c) cap SiO_x layer deposition, and(d) diffusion of Zn over a lateral distance of a few mm, into the MQW section via annealing. It is observed that Zn diffusion through the SiO_x barrier is more dependent on variations in the annealing temperature than on the diffusion time. Annealing was performed in an open tube furnace under nitrogen flow. Anneal temperatures ranged from 600 to 700° C and annealing time was varied from 12 to 30 minutes. For an 80nm SiO_x barrier, annealed at 625° C for 30 minutes, produced no changes in the MQW energy levels. However, the top cladding layer Al fraction was reduced by 0.7 % with a minute increase in the waveguide Al fraction, suggesting negligible zinc diffusion into the MQW region, with some interdiffusion of Ga and Al at the top waveguide-cladding interface. At temperatures above 650° C, noticeable changes were observed in the MQW PL peak positions. For a 20 minutes anneal at 700° C the top cladding layer Al fraction

decreases by 2% and the MQW energy increases by 5 meV due to intermixing of the $Al_{0.35}Ga_{0.65}As$ barriers and GaAs wells.

A schematic of the taper is shown in Fig. 3. Typical lengths of the taper were 2-3 mm. The near field intensity profiles of slab waveguides with and without zinc diffusion were measured by endfire coupling TE polarized light of λ = 895 nm into the unaltered MQW waveguide section of a 3 mm long taper. The output profile, shown in Fig. 4, without the Zn diffusion shows the presence of energy in the normal mode of the composite structure comprising of the fundamental and the first order modes of the MQW guide and the single mode SQW guide. However,with Zn diffusion, the first order MQW mode is entirely suppressed and the energy content in the SQW region has increased, showing the transfer of energy. We will present further details of the diffusion conditions on the performance of the taper, the losses associated with the taper as well as optimization of the same. The work was supported in part by the DARPA/ARO program under contract No. DAAL03-91-C-0042.

Undoped	GaAs	25 nm
Undoped	$Al_{0.35}Ga_{0.65}As$	500 nm
Undoped	$Al_{0.22}Ga_{0.78}As$	100 nm
15 period	Undoped	
19nm $Al_{0.35}Ga_{0.65}As$/65nm	GaAs	MQW
Undoped	$Al_{0.22}Ga_{0.78}As$	700 nm
Undoped	10 nm GaAs	SQW
Undoped	$Al_{0.22}Ga_{0.78}As$	200 nm
n - doped	$Al_{0.35}Ga_{0.65}As$	1200 nm
n - doped	GaAs buffer	300 nm
n - doped	GaAs substrate	

Figure 1 : Schematic of integrated MQW and SQW structure.

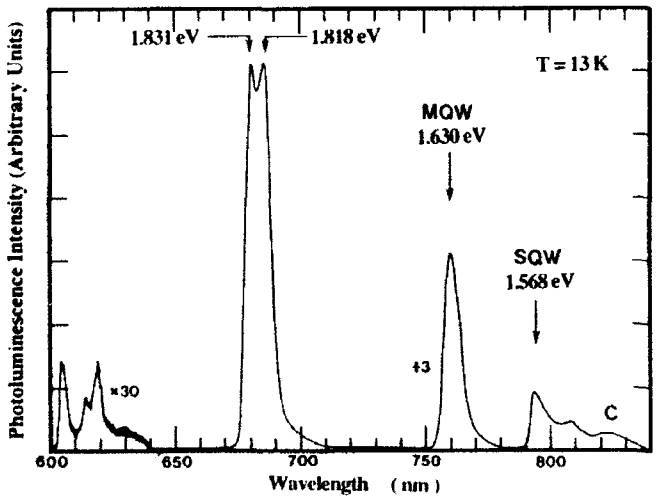


Figure 2 : 13K photoluminescence spectra of the integrated structure. 'C' represents the carbon related transition.

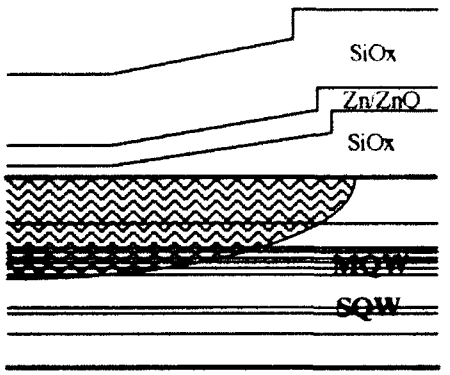


Figure 3 : Schematic of the formation of the taper by zinc diffusion

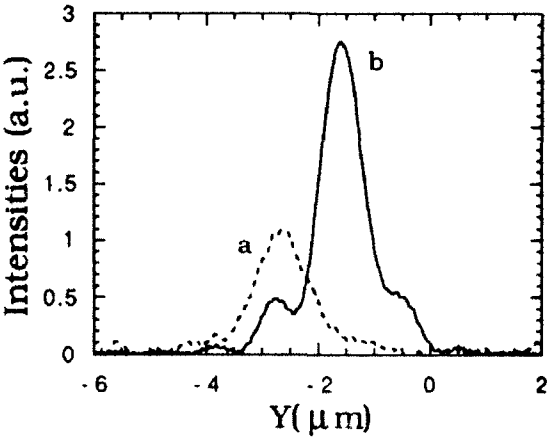


Figure 4 : Output near field intensity profile for light coupled into the undisordered MQW waveguide (a) with and (b) without, Zn diffusion.

ThC4 EFFICIENT 1X16 RADIATIVE OPTICAL POWER SPLITTER BASED ON InP

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Transparent, linear networks based on optical wavelength-division multiplexing are believed to be the most practical solution for very large bandwidth communication. One key device in such a network is an optical 1×N power splitter[1]. N×N multiplexers and star couplers based on a radiative design have been successfully fabricated with Si/SiO_2 based glass waveguides[2]. Here, we present a 1×16 radiative power splitter fabricated with InP-based waveguides. The high refractive index of compound semiconductors makes possible the use of tight bends which considerably reduces the overall size of the splitter as compared to Si/SiO_2 based devices. The possibility of integration with other optoelectronic components such as detectors, gain sections or lasers makes this approach attractive.

The arrangement considered here is illustrated in Fig. 1. The 2.5μm wide input waveguide radiates its power into the planar free-space region, which is a dielectric slab placed between the input waveguide and the receiving array of 16 waveguides. In order to produce equal power distribution in all 16 waveguides, the receiving apertures are increased from 3μm for the central waveguide to 10μm for the outermost waveguide. The receiving waveguides fan out to the 16 output ports which are spaced by 250μm to allow fiber coupling. In a first, straight section, the waveguide width is tapered down to the width of the S-bend. The bend radius of the outermost waveguides is 1.6mm and increases gradually in each successive waveguide toward the central waveguides, so that the end-points of all S-bends are aligned. To reduce the bend losses, the waveguide widths of the outer waveguides is increased up to 4.5μm from the 3μm widths of the central S-bends. Also, offsets at the straight-to-bend and bend-to-bend interfaces have been included[3] in the 6 outer waveguides. The total length of the device is 4.4mm.

We used a buried-rib waveguide structure. The lateral confinement is provided by a 400Å lattice-matched quaternary loading rib spaced by 150Å at InP on a 3000Å quaternary guiding layer of the same composition. The straight waveguide losses are well below 1 dB/cm as determined by measuring the Fabry-Perot (FP) contrast ratios in a straight test section.

The power splitters were tested with 1.48μm light from a semiconductor laser diode. The light is coupled into the waveguide through a lensed fiber. The output light is collected by a 40x microscope lens and coupled simultaneously into a multimode fiber for absolute power measurement and onto an IR-camera for mode monitoring. The small aperture of the multimode fiber acts as a filter effectively discriminating against any stray light.

In Fig. 2, we display the excess loss (in excess of 12 dB splitting loss) of the 16 output ports. The worst case excess loss for TM polarization is 4.6 dB. The average excess loss is around 2 dB which is expected from the design calculation. The results show that the aperture increase for the outermost waveguides overcompensates for the weaker field. This may be due to over-etching which affects the narrower central waveguides more than the wider outer ones. The two outermost waveguides suffer from some bend losses. This is in agreement with the

bend-losses measured on test structures with single waveguides.

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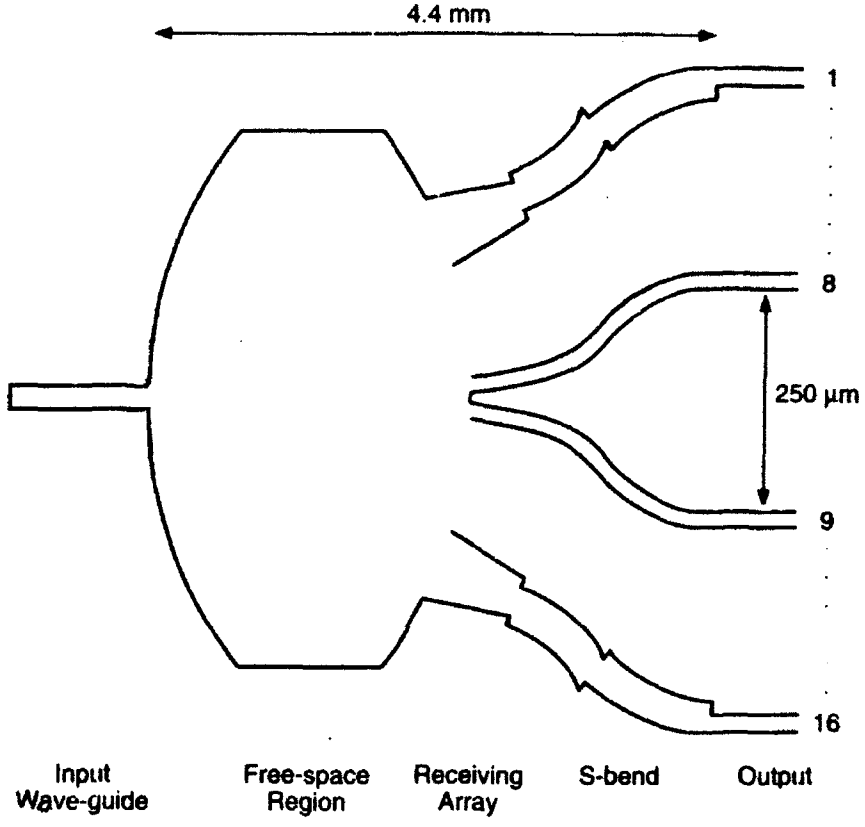


Figure 1 Schematic design of the 1×16 optical power splitter.

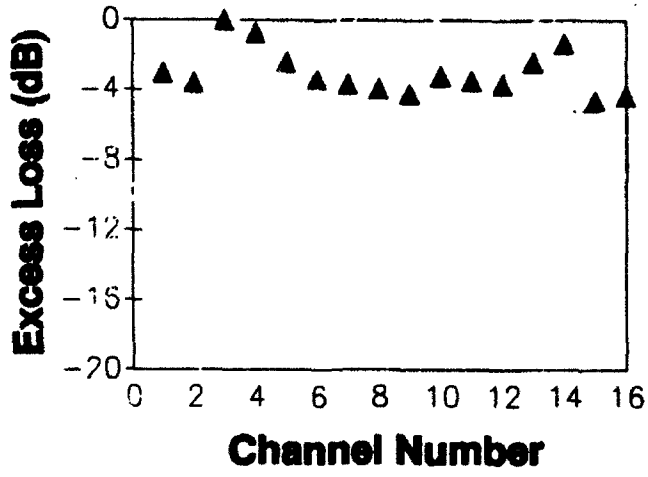


Figure 2 Excess loss for TM polarized light for the 16 output ports.

ThC5

A LOW LOSS BEAM SPLITTER WITH AN OPTIMIZED WAVEGUIDE STRUCTURE

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Integrated beam splitters and turning mirrors in III-V compound semiconductors are important components for the realization of compact integrated optical circuits due to their ability to split the beam or change its direction in a very short distance[1-4]. For the realization of beam splitters, either a partially grooved geometry[4] or a splitting mirror at the center of a tapered waveguide have been employed[3]. In the partially grooved beam splitter geometry, the calculated excess radiation loss is always larger than 3 dB. The reported experimental results also showed too high excess radiation loss eliminating this structure from practical use[4]. In the tapered waveguide structure with a splitting mirror[3], the incoming optical field has its peak at the tip of the splitting mirror. But most fabricated beam splitters do not have ideal sharp tips but rather have unintentionally formed round tips resulting in high scattering loss. This loss can be significantly reduced if one reduces the optical field intensity at the tip of the splitting mirror. In this paper design, fabrication, and characterization of such novel beam splitters with optimized waveguide structures are reported.

The geometry and the basic principle of operation of the new beam splitter based on optimized waveguide structure is shown in Fig. 1. It is basically an improved version of the tapered waveguide geometry with a splitting mirror. The single mode input waveguide excites the two even modes of the triple moded waveguide in front of the splitting mirror. If these modes are excited with equal amplitude and if the length of the triple moded waveguide is chosen such that these modes go 180° out of phase at the beginning of the splitting mirror, the field amplitude will be very small at the tip of the mirror. Hence the roundness of the tip will not contribute a significant loss. With this design the incoming field distribution is divided into two lobes, hence into two halves at the beginning of the splitting mirror. When these halves are reflected from the two sides of the splitting mirror, the reflections will overlap very well with the fundamental modes of the single mode output waveguides.

The lateral dimensions of the pattern on the mask as well as the cross sectional profile are shown in Fig.1. The epitaxial layers are grown on semi-insulating GaAs using molecular beam epitaxy. In the fabrication first a 5000Å PMMA layer is spin coated onto the wafer and a 700 Å-thick Si layer is electron beam evaporated on top of it. Then regular liftoff technique is used to generate a 1000Å thick Ni pattern, which is the etch mask for the waveguide geometry. Then photoresist is spin coated and openings in the mirror areas are formed using standard photolithography. Next Cl_2 based RIE is carried out to form the mirror etch to a depth of 4μm. For the mirror etch the mask that defines the mirror interface is the Ni layer patterned by lift off. The thick photoresist layer protects the sample from being etched everywhere except in the mirror openings. After the mirror etch O_2 based RIE is done to remove photoresist. Then Cl_2 (*to etch Si*), O_2 (*to etch* PMMA), and Cl_2 (to etch the semiconductor) based RIE are sequentially used to etch waveguides. This way the waveguide geometry and the mirror plane are defined by the same Ni mask, hence the process is self aligned. The waveguides are etched 0.5 μm deep and during waveguide etching, HeNe laser interferometry is used to monitor the etching depth *in situ*. After the formation of the mirror and the waveguide, the etching mask is removed by soaking the sample in acetone. For this waveguide design, the proper length of the 12 μm-wide waveguide is about 250 μm based on an effective index analysis.

The scanning electron microscope picture of a fabricated beam splitter as well as the detail of a splitting mirror are shown in Fig. 2. The transmission characteristics of the beam splitters are measured both for TE- and TM-polarizations. In the measurements, a 1.15 μm He-Ne laser output is end fire coupled and the output of the waveguides are measured using both an IR-vidicon camera and a Ge detector. By comparing the output power of the waveguide with a beam splitter with those from the straight waveguides, the excess radiation loss is measured. The characteristics of the beam splitters with perfect mirrors are also simulated using two-dimensional FD-BPM combined with effective index approximation[5]. The results of both experiments and calculations are shown in Figure 3. The calculations show that the excess radiation loss of the beam splitter can be as low as 0.2 dB for an optimum length if the mirrors are perfect. This loss is due to deviations in the modal interference and mode overlap from the ideal. The minimum measured excess radiation loss is about 1.2 dB for TE mode and 1.8 dB for TM modes for L = 250 μm. These values are the lowest among the measured values reported. These results combined with the theoretical analysis indicate that mirror losses for these structures could be as low as 0.5 dB/mirror. As seen in Fig. 3, TM polarization has always higher loss than TE polarization. Due to Goos-Hanchen phase shift upon total internal reflection, optimum mirror position is slightly different (difference being 0.2 μm for the particular case) for TE and TM polarizations. In the mask design mirror position was

optimized with respect to TE polarization so it was off about 0.2 μm for TM polarization. But after the photolithography, lift off, and etching the mirror plane turned out to be about 0.3 μm off from its intended position. The direction of the error was such that it increased the displacement error for TM polarization to about 0.5 μm. This approximately results in an 0.35 dB more loss for TM polarization. Additional loss is due to a combination of several factors, such as mirror surface roughness and the tilt of the mirror plane in the vertical direction. Further improvements and optimization in photolithography and etching could reduce these factors resulting in better turning mirrors.

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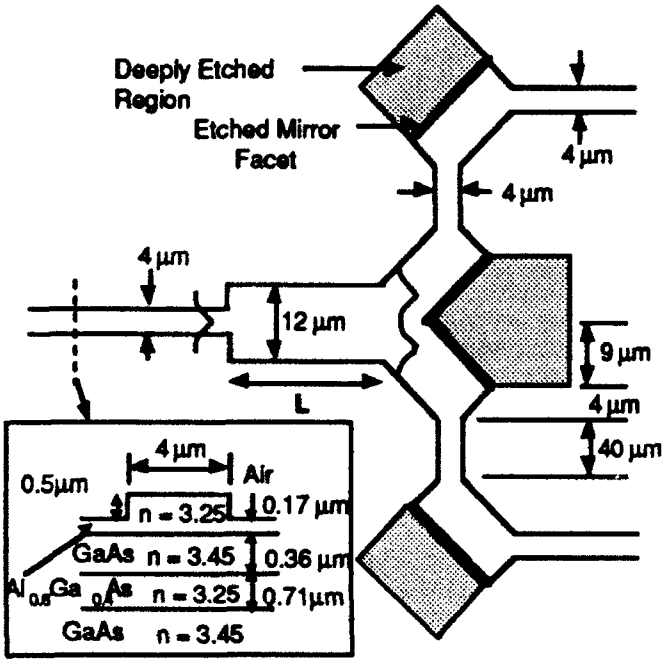


Fig. 1 The geometry and basic principle of operation of the beam splitter with optimized waveguide geometry. L varied from 100 to 400 μm. Inset shows cross sectional profile of the 4 μm wide single mode rib waveguides. Epitaxial layers are undoped.

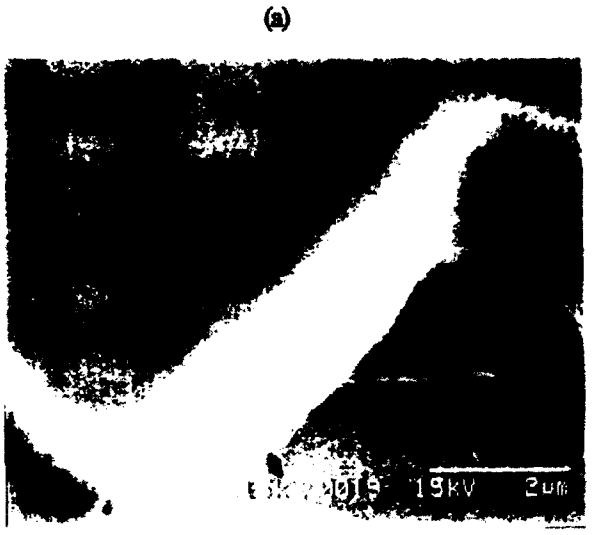


Fig. 2 (a) Scanning electron microscope picture of a fabricated beam splitter. (b) Enlarged view of the tip of the splitting mirror.

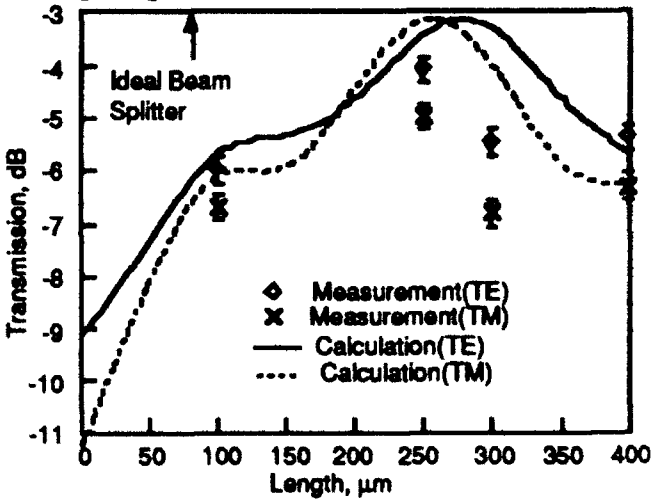


Fig. 3 The simulated and measured transmission characteristics of beam splitter with optimized waveguide structure. Points show the experimental results and continuous curves are the results of simulations assuming perfect mirrors.

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HIGH-EFFICIENCY LONG LIFETIME AlGaAs/GaAs LIGHT EMITTING DIODES ON Si SUBSTRATES

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We have recently reported the long lifetime light emitting diodes (LED's) utilizing the UCGAS (undercut GaAs on Si) structure in which a part of the GaAs layer is separated from the Si substrate.[1] The thermal stress and the dislocation density in the UCGAS were found to be less than those in the conventional planar GaAs on Si. [2,3] This paper describes the LED's grown on the UCGAS which have both the high efficiency and long lifetime.

Fabrication procedure was described in the previous papers.[1-3] The LED has 300 μm outer diameter and the laterally etched distance is 100 μm. Following three types of LED's were fabricated to provide different defect density; as fabricated UCGAS LED, the UCGAS LED annealed at 800 °C and the LED grown on the pre-fabricated UCGAS. The photoluminescence (PL) dark spot density (DSD) in GaAs was counted to evaluate the crystal quality. The DSD's of the above three types of the LED's are more than 2×10^8 cm^{-2}, about 1×10^8 cm^{-2}, and about 1×10^7 cm^{-2}, respectively. The DSD counted in this way is normally higher than the etch pit density, and this method is capable of detecting very small (less than 1 μm in diameter) defects.

The internal quantum efficiency of the LED is given by $\eta = (1 + \tau_r / \tau_n)^{-1}$ where τ_r and τ_n are radiative and non-radiative lifetime of the injected minority carriers, respectively. Assuming the carriers recombine non-radiatively through the defects, the non-radiative recombination lifetime can be expressed as $\tau_n = (\sigma v_{th} N_d)^{-1}$, where $v_{th}=10^7$ cm/s is the thermal velocity of the carriers, σ is the capture cross section, N_d ($=n_d^{3/2}$) is the bulk density of the recombination center, and n_d is the in-plane density of the recombination center and corresponds to DSD. Therefore, $\eta = (1 + C N_d)^{-1}$, where $C = \sigma v_{th} \tau_r$. Calculated and the experimental relative efficiencies are shown in Fig.1. Since the internal efficiency is difficult to measure, the relative efficiency is adjusted to give the best fitting to the calculated values. The best fitting is obtained when $C = 5 \times 10^{-12}$ cm^{-3}. Assuming the radiative recombination lifetime of 1 ns, the recombination cross

section is obtained to be 5 x 10^{-10} cm^{-2} ($\sqrt{\sigma}$ = 0.22 μm) which is in the same order of the PL dark spot area showing that the DSD determines the internal efficiency. Figure 1 also indicates that the efficiency is almost unity if the DSD is less than 10^6 cm^{-2}.

The output power of the LED grown on the UCGAS is shown as a function of the aging time in Fig.2. The thermal stress is measured by the PL spectrum at 55 K to be less than 5 x 10^8 dyn/cm^2 in the UCGAS-LED. The result for the mesa-LED which has the stress more than 3 x 10^9 dyn/cm^2 and DSD more than 10^8 cm^{-2} is also shown for comparison. The reduction of the stress and the dislocation density is quite important for the long term operation of the LED. The UCGAS-LED has very small degradation rate even after the operation of more than 2000 hours. This operation lifetime is the longest among any AlGaAs/GaAs LED's fabricated on Si substrate.

In summary, high efficiency and long lifetime UCGAS -LED has been fabricated, and the operation more than 2000 hours is demonstrated for the first time.

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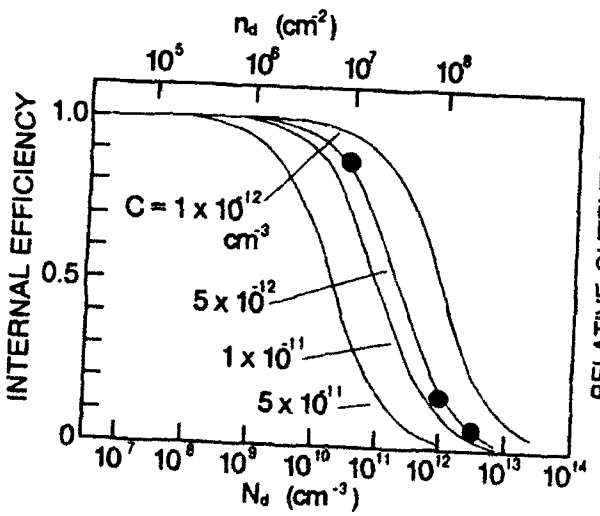


Fig.1

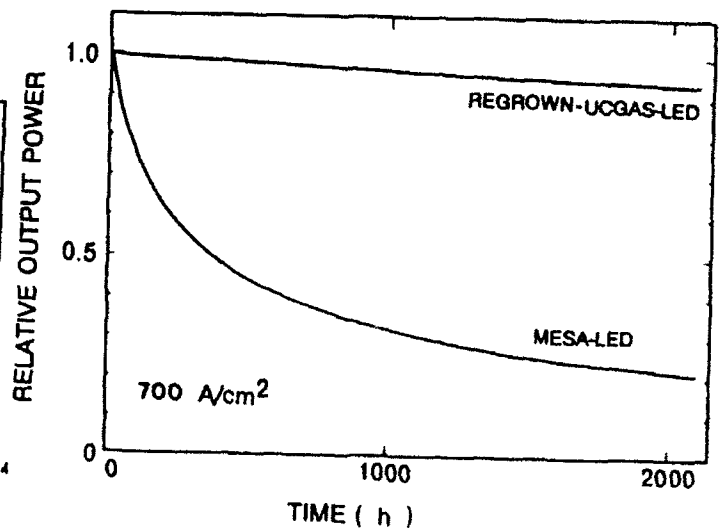


Fig.2

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>30 GΩ ISOLATION OF GaAs DEVICES ON DOPED Si VIA UNDOPED BUFFER LAYERS; APPLICATION TO SYMMETRIC SELF-ELECTRO-OPTIC EFFECT DEVICES

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There has been a reemergence of interest in GaAs-on-Si devices during the past few years for the application to optical interconnections between integrated circuit chips. This is due to the finding that reliable, long-lived GaAs surface-normal modulator/detectors may be grown on silicon.[1,2] These devices may be placed throughout the surface of the chip, producing thousands of optical access pads. This then frees the I/O bottleneck of silicon VLSI chips.

Prior to this work, p-i(multiple quantum well [MQW])-n GaAs modulator/detectors have been grown n-side down with n-doped buffers on a n^+ silicon substrate, which formed the n-contact. Clearly, sophisticated circuit designs will require that independent contacts be made to the devices, rather than having all the n-contacts connected. An example is a "totem pole" receiver input in which two detectors are placed in series and the center pin connected to the gate of the input transistor. This allows differential-type optical inputs where the receiver is sensitive to the ratio of two light beams rather than to their absolute value, drastically reducing on-off contrast requirements in the beams. Note that this "totem pole" (minus the transistor) is a symmetric self-electro-optic effect device (S-SEED).[3]

We demonstrate here that by using undoped buffer layers (Fig. 1), extremely effective isolation of high-quality GaAs modulator/detectors is achieved. We achieve n-n resistances greater than 30 GΩ. An S-SEED device is made, demonstrating the isolation. We obtain a bistable contrast of 2.9 for a 7 volt supply.

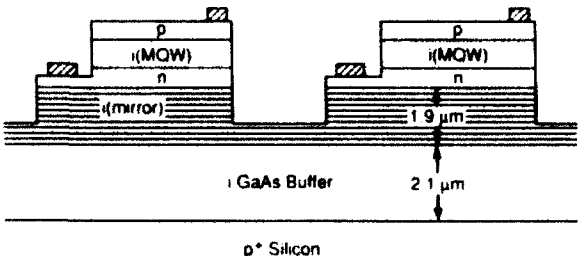


Fig. 1: Schematic of our GaAs/AlGaAs modulator/detectors grown on doped silicon.

The sample was grown on a p^+ silicon substrate oriented 3° off the (100) axis. Gas-source molecular beam epitaxy (GS-MBE) was used for the crystal growth. After a 850 °C oxide desorption, 0.5 μm of intrinsic GaAs was grown at a substrate temperature of 350 °C. This was followed by 1.6 μm of intrinsic GaAs at a substrate temperature of 550 °C. Subsequently, the i AlAs-AlGaAs mirror (designed for 850 nm), n contact, i(MQW) (1 μm total thickness) and p cap are grown as shown in Fig. 1 at 600 ° C. After depositing the p-contact pads, 200×200 μm square mesas were etched down to the n-layer. Then n-contact pads were made, and 200×300 μm mesas etched down to about the middle of the mirror.

In Fig. 2, a typical current-voltage characteristic across two adjacent n-contact

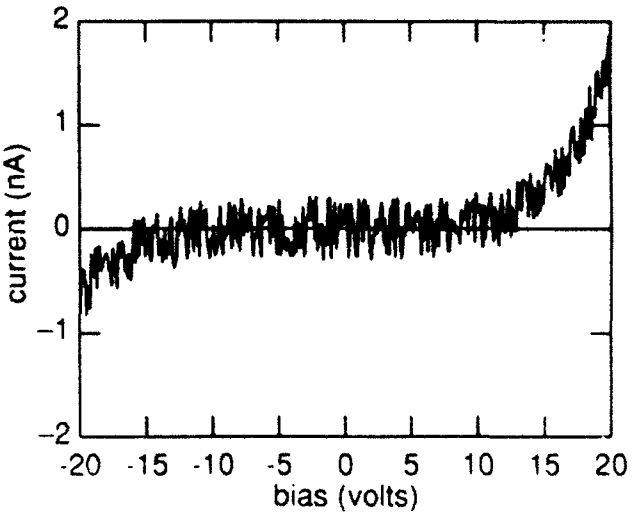


Fig. 2: Typical current-voltage characteristic between n-contacts of adjacent (100 μm apart) mesas of Fig. 1, showing device isolation > 30 GΩ at 10 volts bias.

pads is shown. At 10 volts bias, the current is under 0.33 nA, yielding a resistance greater than 30 gigaohms. The leakage becomes higher at 20 volts bias, but the DC resistance remains above 10 GΩ. The low leakage is aided by the fact that the substate is p-type. This reduces the current path through the substrate, since a diode forms between the n-contact and the substrate, and this path is modelled by back-to-back diodes. It is remarkable that the reverse bias leakage of these diodes is so low considering the amount of defects present in the GaAs buffer. There is another current path, through the buffer/mirror itself. The mesas are 200 μm wide, and the distance between mesas is 100 μm. Since the current through the buffer is even lower than 0.33 nA at 10 volts, we may assign an average resistivity $\rho = RA/l$ greater than 2.4×10^{7} Ωcm. Undoubtably the mobility through this material is much lower than single-crystal GaAs due to the defects which act as scattering centers. If we assume an average mobility of 10 $cm^2/(volt-sec)$ (one-thousandths that of electrons in pure single-crystal GaAs), the average carrier density is less than 2.6×10^{10} cm^{-3}, i.e., an incredibly pure material.

A change in reflectivity from 12 to 42 % was obtained for 0-8 V modulation on the devices. To test whether the devices could be arranged in a totem pole circuit we formed an S-SEED. The p-contact of modulator 1 was connected to the n-contact of modulator 2. The n-contact of modulator 1 was connected to the positive terminal of the power supply and the p-contact of modulator 2 was connected to ground. This circuit is bistable depending upon the ratio of light powers on the modulators.[3] Note that if leakage existed between the n-contacts modulator 1 is effectively short-circuited and the S-SEED would not function. The amount of leakage determines how low the optical power may be. In the following experiment the average beam power was 100 nW. A Ti:sapphire laser was tuned to the exciton wavelength, and split into two beams, one of which was modulated by an acoustic-optic modulator. The beams were focused on the modulator/detectors. Fig. 3 shows the intensity of the modulated beam after transmission through the modulator/detector. Clear bistability is observed for supply voltages as low as 2 V. A bistable contrast of 2.9 was obtained for a 7 V supply.

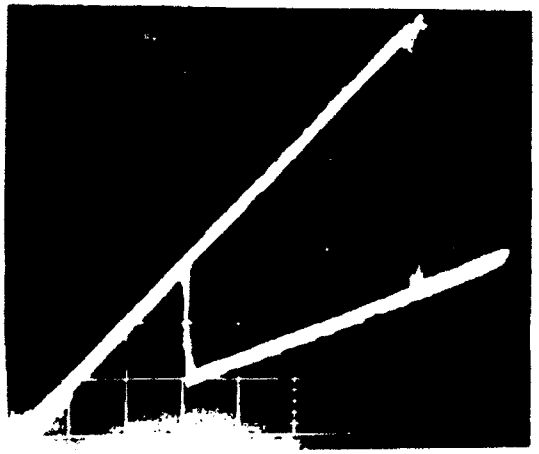


Fig. 3: Transmitted vs. reflected power of S-SEED. If leakage existed between the n-contacts this device would not function.

In conclusion, we have demonstrated that high-quality GaAs devices (in this case modulator/detectors) may be grown on doped silicon substrates with > 30 GΩ isolation by using undoped buffer layers. This is of importance for optical interconnects of silicon chips since independent contacts to the modulator/detectors enable far more flexible and superior circuit designs compared to if the modulator/detectors had a common contact. We demonstrate one circuit that requires independent contacts, the symmetric SEED, and obtain a bistable contrast of 2.9:1 with 7 volts bias.

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FB3 FLIP-CHIP, SELF-ALIGNED, OPTOELECTRONIC TRANSCEIVER MODULE

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ABSTRACT

A compact, planar-processed optoelectronic transceiver package is described for monolithic arrays of self-aligned, flip-chip mounted OEICs coupled to arrays of multimode optical waveguides and fibers.

Introduction

The high cost of telecommunications fiber optic links when used in data communications applications is prompting a renewed interest in 0.85 μm wavelength, low-cost optoelectronic technology [1]. Extensions of this technology into monolithic arrays of AlGaAs lasers, GaAs OEICs (optoelectronic integrated circuits) and multimode optical fibers is being explored for use in high-speed, short distance (≤ 1 km) computer interconnections [2]. For this technology to be pervasive, optoelectronic packaging, which today involves robotically aligned and assembled precision machined components, must be adapted to a high volume, low-cost manufacturing environment. Compact, planar-processed, optoelectronic packages, utilizing batch fabrication and assembly techniques, would be a significant advance provided the added processes are compatible with high-performance, high-density electronic packaging. Elements of these concepts are being explored elsewhere [3, 4]. We describe here the application of these concepts to an optoelectronic module, containing both a 4-channel laser array chip and a 4-channel receiver chip on a single substrate.

Package Overview

Figure 1 shows a schematic view of the 4-channel, duplex module. It consists of an electronic carrier, about 8 mm x 12 mm, with electrical wiring and planar processed optical waveguides. To attain very high density, the laser transmitter and receiver chip are packaged on the same substrate with the optical waveguides providing fan-in/fan-out of the optical signals from the O-E chips to the edge of the module where a de-mountable multi-fiber ribbon connector interfaces the module to the system cables. To facilitate assembly and minimize electrical parasitics, the O-E chips are flip-chip solder-bump attached to the package substrate. During solder reflow, the surface tension of the molten solder automatically aligns the O-E components to the optical waveguides. The optical waveguides are fabricated using a CVD flame-hydrolysis process [5]. The optical waveguides not only provide space transformation, but also optical feed-through for a hermetic seal, access to the photodetector on the flip-mounted OEIC receiver chip, and micro-mechanical structures, patterned simultaneously with the waveguides, which facilitate the optical alignments.

Flip-Chip O-E Alignments

The use of solder bumps to automatically align optical components has been explored elsewhere [3]. However, in the case of optoelectronic chips, where the numbers of solder bumps are small (less than twenty) variations in the solder volume of each bump (a few tens of percent using typical manufacturing processes) can lead to variations in the height of the attached chip, corresponding to variations in coupling efficiency between the O-E component and waveguide. This is a particularly serious problem in the alignment of the laser array chip.

The laser chips have been fabricated using the recently developed "FUll WAfer" (FUWA) technology. The concept is based on high quality dry-etched mirrors and allows for full wafer processing and testing as well as integration of other electronic and photonic devices. Besides the four lasers, the chips

have four integrated monitor photodiodes located at the back facets of the lasers. Details on the FUWA technology are reported in Reference [6].

To insure the laser array is positioned at the proper height, standoffs, formed at the same time and with the same material as the optical waveguides, are used at four corners of the chip (Figure 2). In addition, etched trenches are formed in the laser chip, which lower it so the light output launches into the center of the waveguide core. These 20 μm deep rectangular alignment trenches are etched by chemical assisted ion beam etching (CAIBE) which is the same technique as used for the etching of the laser mirrors. The depth of these trenches is controlled by etch time only.

The use of standoffs, however, presents another problem. The restoring force of the molten solder ball during chip attach becomes vanishingly small when the pads on the chip and package are aligned. If the chip is resting on the standoffs, the resulting frictional forces can overcome the small surface tension forces which can lead to misalignment. To overcome this difficulty, the edges of the stops and trenches are used to align the laser. In addition, the pads are purposely offset, to insure that there is sufficient force provided by the molten solder to overcome the frictional forces and to establish contact between the aligning surfaces. The combination of these concepts allows one to pick and place the chip with misalignments as great as ± 25 μm which are then removed automatically during solder reflow.

The alignment accuracy of the laser chip to the optical waveguides is determined by the etch tolerance of the waveguides and standoffs on the package, the overlay tolerance of the etched trench (both depth and lateral placement) relative to the laser output and the tolerance in the thickness of the waveguide core. Etch tolerances for the optical waveguides have been found to be ± 1 μm. The depth of the trenches on the laser chip is 20 μm ± 1 μm (measured on two completed wafer runs) and located relative to the laser output to within ± 1 μm. Variations in the thickness of the waveguide core are about 2% corresponding to about ± 0.75 μm. Therefore, worst case misalignment (aside from contamination during assembly) is ± 1.75 μm in the vertical direction and ± 2.0 μm in the lateral direction.

Laser array chips have been flip-chip soldered to substrates using Pb/Sn eutectic solder. Figure 2 shows an SEM photograph of a 4-channel laser array chip coupled to an array of waveguides whose core dimensions are 20 x 36 μm. The total glass thickness is 80 μm. Mechanical alignment is estimated to be better than 2.0 μm which is consistent with the measured outputs from the coupled waveguides: coupling losses are between 3.9 and 4.2 dB for all four channels.

The attachment of the GaAs receiver array chip is similar to that of the laser array, except that the coupling tolerances of the waveguide to the detector are much larger, thus eliminating the need for lateral alignment stops. However, to couple the optical signals in the waveguides to the photodetectors, a reflecting bar is included, which deflects the light vertically upward onto the surface of the photodetector (Figure 3). The reflector bar is bonded to the receiver chip prior to attaching the chip to the package. The diameter of the sensitive area of each detector is 80 μm. Coupling losses, estimated from the electrical outputs of the receiver chip, are about 4.0 dB. This loss includes fiber/waveguide coupling, Fresnel reflections, waveguide propagation and bend loss, and waveguide/detector coupling loss.

Module Connector

The 4-channel, transceiver module is interfaced to system cables with a modified, commercially available 8-fiber ribbon connector [7]. The connector consists of a precision plastic molded ferrule containing the fibers which is normally mated to a similar ferrule with precision metal guide pins and a spring clip retainer. In the connector developed here, one of the ferrules is replaced with the module, and by appropriately modifying the guide pins, the fibers can be made to align to the optical waveguides. As was done for the O-E chip alignment, glass registration features are fabricated at the same time the waveguides are formed, thus allowing photolithographic alignment of the guide pins to the optical waveguides in the lateral direction. Precise vertical positioning of the optical fibers to the waveguides is obtained by precision grinding of the guide pins.

The average coupling loss between transmitter waveguides (20 x 36 μm core dimension) and 50/125 μm fibers is 1.2 dB including two Fresnel reflections (0.3 dB). The average coupling loss between re-

ceiver waveguides (55 x 36 μm core dimension) and 50/125 μm fibers is 0.6 dB including two Fresnel reflections. The mechanical alignments are estimated to be around 2 μm.

Link Tests

Measurements have been carried out operating the packaged receiver arrays with a commercially available reference laser source at a data rate of 1 Gb/s. The receivers operate at a minimum sensitivity of -17.6 dBm as measured at the module connector (i.e., including Fresnel reflections, waveguide coupling and propagation losses, and detector/waveguide coupling losses). The lasers have been demonstrated at modulation rates in excess of 2.4 Gb/s. An "optical wrap" has been demonstrated, where the output of one of the lasers is coupled to the input of one of the receiver channels, both on the same substrate, using a 5 meter multimode fiber jumper. Error free operation has been observed at 1 Gb/s.

Summary

In summary, a compact, planar-processed package using flip-chip, self-aligned optoelectronic components has been described. The packaging concepts are compatible with existing high-speed, high-density electronic packaging materials and processes and therefore have the potential for high volume, low cost manufacturing.

Acknowledgements

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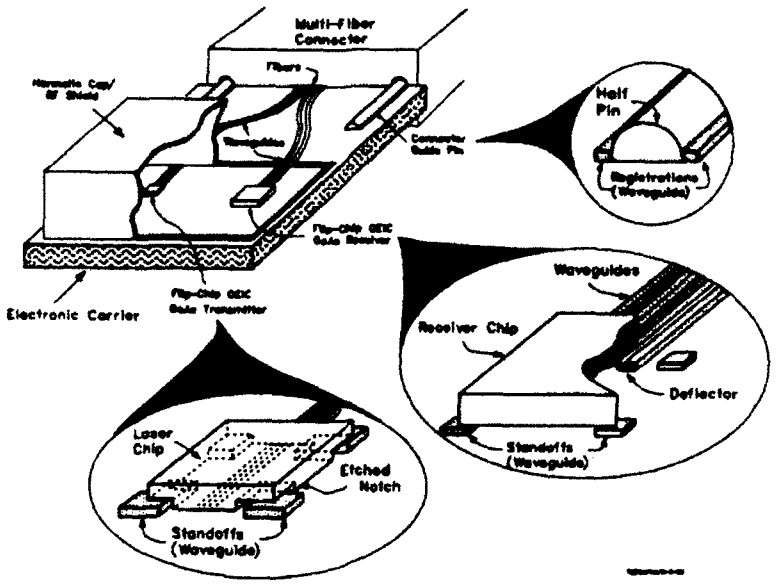
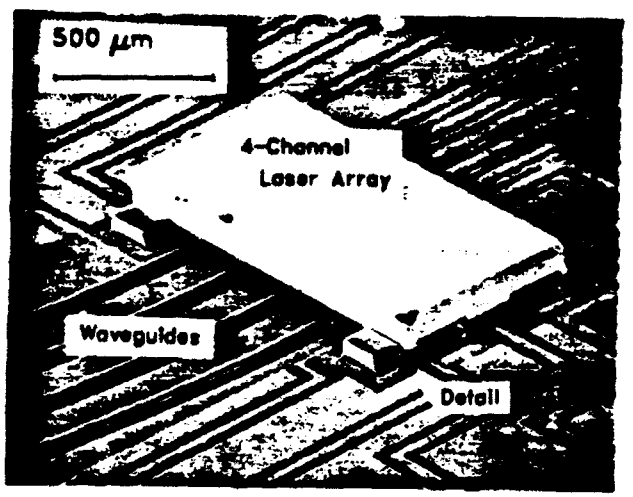
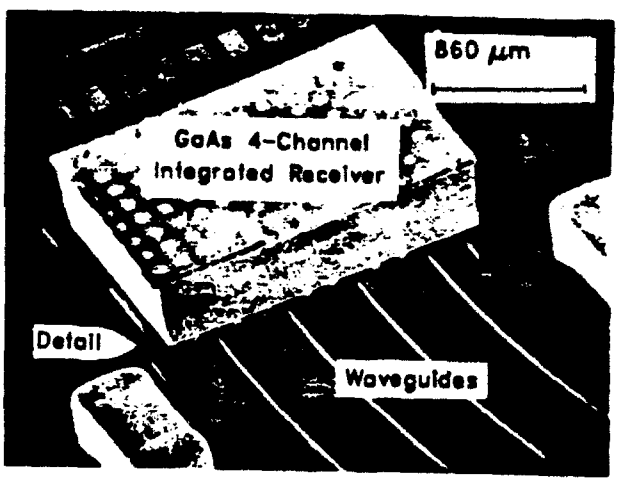


Figure 1: Schematic representation of the 4-channel transceiver module.





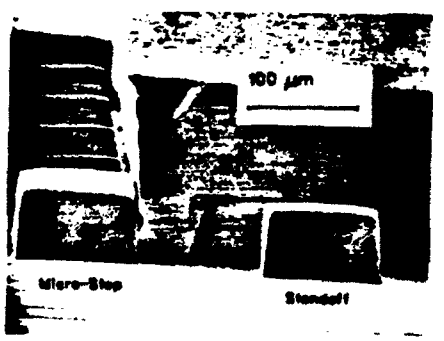


Figure 2: SEM photographs showing 4-channel, AlGaAs laser array chip with integrated monitor photodiodes attached to the package.

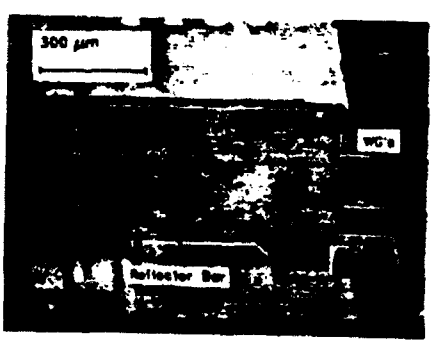


Figure 3: SEM photographs showing flip-chip solder bump attachment of 4-channel, MESFET, integrated MSM detector/pre-amp receiver to package.

FB4

A SILICON WAFERBOARD APPROACH TO OPTOELECTRONIC PACKAGING

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Widespread use of fiber-optic technology in high volume applications such as telecommunications and computer interconnects is largely dependent on the availability of low-cost optoelectronic component subsystems. Systems using optical interconnects require many parallel optical channels, each consisting of a receiver and transmitter operating at speeds up to 1 Gb/s. This use of a silicon substrate for optoelectronic packaging applications has received much attention by various researchers (1,2). The range of active and passive, optical and electronic chips involved in these multichannel subsystems requires a new versatility in the approach to the integration of these parts for optimum functionality and minimum cost. Some of the special requirements of these optoelectronic subsystems, including high speed, high density, and precise mechanical positioning, are particularly amenable to handling with "Silicon Waferboard" technology. In this paper, we describe the use of silicon as a substrate in a hybrid technology for the integration of these disparate elements.

In our presentation, we will review the process challenges arising during the fabrication of three different subsystems based on silicon waferboard technology. The first subsystem, shown in Fig. 1, is an example of a four-channel transmitter design incorporating a GaAs laser driver chip and an InGaAsP/InP laser array coupled to four single-mode optical fibers. In this system, we have demonstrated passive alignment of the laser array to single-mode fibers achieving butt-coupling efficiencies of 7%. This was accomplished via the incorporation of precisely etched silicon and polyimide standoffs to control the laser placement and orientation etched v-grooves for fiber placement (3). Using the processes developed for this transmitter waferboard as basic building blocks, we will describe the fabrication of a photodetector module subsystem designed for a balanced heterodyne receiver (Fig. 2). This module provides a compact platform(0.5 in. substrate) for the integration of two single-mode optical fibers positioned in etched v-grooves with respect to two high-speed photodetectors. Included on this module are two 90 pF polyimide bypass capacitors in addition to bias and signal-line connections for each detector. The detector DC responsivities measured at 1.3 μm on this waferboard were 0.75 A/W. This was improved to 0.8 A/W by injection of an index matching fluid between the dectector and the optical fiber. The third subsystem, shown in Fig. 3, is a waferboard design incorporating a dielectric waveguide between a high N.A. optical fiber and a ridge waveguide laser. This subsystem uses a one-dimensional active alignment of a 0.98 μm laser to the waveguide and provides a v-groove passive alignment of the high N.A. fiber to the output end of the waveguide. The waveguide which has an oxy-nitride plasma deposited core embedded in silica provides close to a 40% improvement in coupling efficiency vs that obtained via standard butt-coupling of the fiber to the laser.

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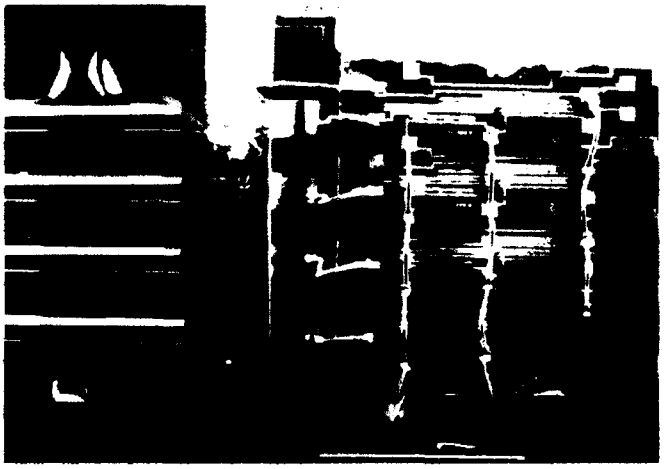


Fig. 1. Transmitter subsystem.

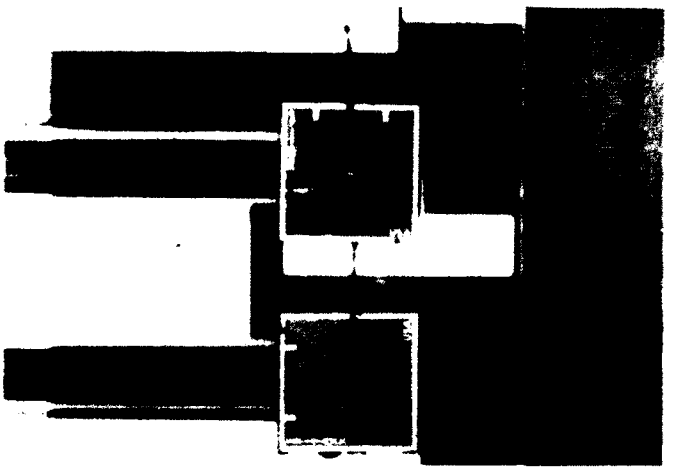


Fig. 2. Detector subsystem.

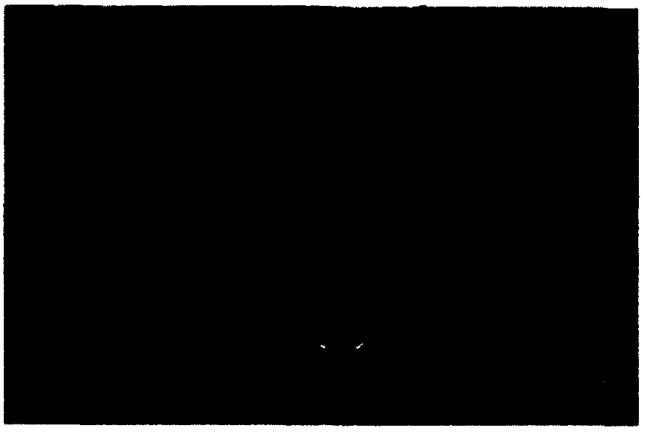


Fig. 3. Waveguide subsystem.

FB5

OPTICAL COMMUNICATION THROUGH STACKED SILICON WAFERS USING MONOLITHIC THIN FILM EPITAXIAL LIFTOFF InGaAsP EMITTERS AND DETECTORS

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Summary

Through wafer optical interconnects will enable the development of high density three-dimensional stacked silicon circuitry, leading to massively parallel signal processing systems. We have demonstrated communication between two stacked silicon wafers using monolithically integrated thin film InGaAsP emitters and detectors. The InGaAsP devices operate at λ = 1.3 μm, a wavelength to which silicon is transparent. A thin film InGaAsP pin photodiode (4.5 μm thick) was monolithically integrated on the surface of a nitride-coated polished silicon wafer which was then aligned and stacked onto another nitride-coated polished silicon wafer on which a thin film light emitting diode (LED) (4.5 μm thick) was monolithically integrated.

The thin film InGaAsP pn junction LEDs and pin photodiodes are fabricated from InGaAsP/InP lattice matched material grown using a standard liquid phase epitaxy system. The devices are formed using a pair of selective etches which etch mesas in the InGaAsP/InP structures to define 250 μm x 250 μm emitters and detectors and a second etch which releases the epilayers from the substrate. The resulting thin film LEDs and pin photodiodes are transferred, aligned and deposited onto the host silicon substrate using a transparent polyimide diaphragm [1,2]. The silicon wafers were polished on both sides to reduce optical scattering losses and then coated with silicon nitride to electrically isolate the stacked wafers. The thickness of the silicon wafers was 650 μm.

Using this epitaxial lift off technique, a single LED was aligned and deposited p-side down on a gold pad evaporated on the silicon wafer. After planarizing the LED using polyimide, a top ring contact was patterned and deposited. Similarly, a thin film pin photodiode was aligned and deposited p-side down with its ohmic contact annealed to a windowed gold contact pad on the wafer surface. Then, the pin photodiode was aligned with the LED on the other wafer, resulting in the stacked architecture depicted in Figure 1.

The InGaAsP LED was driven by a 55 mA pulsed current source and the pin photodiode signal was detected using a low noise transimpedance amplifier and oscilloscope. Figure 2 shows the measured current pulse input to the LED (lower trace) and the photodiode response (upper trace). In this first demonstration, no attempt was made to optimize the emitter, detector or optical coupling between the emitter and detector.

For the first time, optical communication through stacked silicon wafers using monolithically integrated ELO thin film emitters and detectors has been successfully demonstrated. Three-dimensional optical interconnects through silicon circuitry layers will ease the high density of in-plane interconnects which threatens to limit processing density as well as potentially reducing the input/output bottleneck and increasing processing speed.

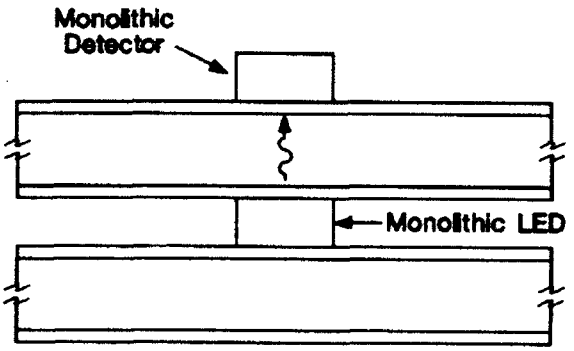


Figure 1: Schematic of stacked silicon wafers with monolithically integrated LED and pin photodetector.

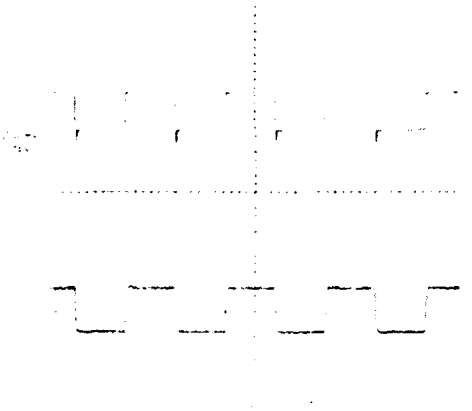


Figure 2: Light emitting diode excitation (lower trace) and measured pin photodetector response (upper trace).

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FB6 OPTIMIZATION AND RELIABILITY OF EPITAXIAL LIFT-OFF FOR OEIC FABRICATION

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Epitaxial lift-off (ELO) is becoming an interesting technique for integrating high-quality devices onto dissimilar substrate materials. It is an integration technique which combines the advantages of both monolithic and hybrid integration [1], and it is very powerful and flexible since it permits that ELO devices are fabricated before or after transplantation (preprocessing and postprocessing). Our work is focusing on the preprocessing strategy, having the advantages that (a) fully optimized ELO devices can be integrated with other optimized devices, (b) devices can be tested before integration, and (c) that after transplantation only an interconnection step is required. This integration approach could be very promising in near-term future, since one can make use of foundry services for both ELO and other devices before the ELO grafting. For example, for fabricating an optical receiver, it should be possible to use on one hand a foundry service for GaAs MESFET amplifier circuits and on the other hand a fabrication service for optical switches. In the final phase, the two devices can be integrated together by ELO. In this way ELO devices have performances similar to those used in hybrid circuits, with the additional advantages of monolithic integration (high speed and low noise). This kind of integration strategy is currenty under investigation in two European RACE projects on broadband communication systems based on photonic switching. In the RACE OSCAR and ATMOS projects, ELO GaAs MESFET circuits, fabricated by a foundry service, will be integrated with an InP Passive Access Node (PAN) optical switch [2], forming a key component in the Very High Speed Optical Loop (VHSOL) [3]. To our knowledge, this is the first time that a foundry service is used for OEIC fabrication with ELO. In this paper we present results on MESFET behaviour before and after ELO. We also describe the optimized ELO procedure that is used, and some initial stability and reliabilty tests.

In the foundry, ELO MESFET's were fabricated by Philips Microwave Limeil, a division of the Laboratories d'Electronique PHILIPS (PML/LEP-Limeil Brevannes-France) on a 400 μm GaAs substrate and using a 20 nm AlAs layer. The total thickness of the ELO epitaxial layers was about 0.7 μm and the MESFET technology made use of a dielectric isolation between 3 interconnection levels. Epitaxial lift-off was done using a HF:DI (1:5) solution at 0 °C and a tensile wax layer [4], and ELO samples were Van der Waals (VdW) bonded on the InP host. We discovered however that the environment in which the transfer of the thin ELO devices to the new substrate takes place, plays a very critical role on the VdW bonding quality, as well as cleanliness and flatness of the bonding surface of the host. This lead to an optimization of the ELO technique. First of all, we used an 'under water processing' in the transplantation phase. This means that after lift-off etch, the etchant is removed while continously adding fresh DI water. After sufficient rinsing, a vacuum pencil was used to transfer the ELO film to the new host, without leaving the water. The vacuum pencil is mechanically driven by translation tables, which makes that the transfer can be done with sufficient reproducibility and yield (≈ 100 %). The other important issue, the cleanliness and flatness of the host, was greatly improved by using a thin (≈ 300 nm) polyimide (PI) layer bonding assisting layer on the InP substrate. The deposition was done by spinning, followed by the bake-out at 350 °C. A great advantage of this procedure is that the PI is planarizing the InP top surface. This is very interesting in our preprocessing approach, since small irregularities, difficult to avoid in substrate device processing, can be allowed on the host. The combination of the 'under water processing' and the PI bonding assisting layer results in a bonding morphology which in most cases is bubble-free. Bonding strength of this VdW bonding on PI is investigated as a function of bake-out temperatures in vacuum with the 'Scotch tape-test'. Yield, i.e. the fraction of the ELO film that is still on the host after tape-test, is zero when no bake-out is

used while a nearly 100 % yield is obtained after a bake-out to 170 °C. Causing no process incompatibilities, this low temperature is very interesting for our preprocessing.

The foundry MESFET's (gatelength 0.7 μm) were transferred in this way to PI-coated InP, and their performances were compared with those from MESFETs still on their growth substrate. Measurements showed nearly no difference in DC operation, as is illustrated in Table 1 and Fig. 1.

	g_m (mS/mm)	$-V_T$ (V)
before ELO	157.9 ± 3.1	1.60 ± 0.05
after ELO	152.5 ± 3.9	1.56 ± 0.06

Table 1 : Comparison of DC behaviour (V_{GS} = 0 V and V_{DS} = 3 V) of foundry GaAs MESFETs (0.7 μm gatelength) before and after transfer to InP.

In Table 1, mean value and spread of transconductance g_m and pinch-off voltage V_T are compared. All MESFETs originated from one wafer, and MESFET's were on several ELO films. This prooves very good our ELO reproducibility. In Fig. 1 the transconductance g_m is compared as a function of V_{GS}. As can be seen, both curves are very close and only a small deviation is shown in the high V_{GS} region. Similar results were also obtained in RF measurements (differences in unity gain cut-off frequency were less than 10 % before and after ELO and were typically about 14 GHz) and in gate leakage measurements. We did further on some initial stability measurents, however not on the foundry MESFET's, but on home-made MESFET's (gatelength 2 μm). These tests concern the stability of I_{DS} (V_{DS}=3V, V_{GS}=0V : power consumption 60 mW) and of I_{GS} (V_{DS}=5V, V_{GS}=-1.5V : in nearly pinch-off) as a function of time and is given in Fig. 2.

In conclusion, we have reported some results on the optimization of the ELO technique, and its application to foundry GaAs MESFET's. Important issues in the transplantation of preprocessed ELO films are the environment in which the transfer takes place and the PI bonding assisting layer. DC, RF, gate leakage measurements on the foundry MESFET's showed nearly no difference in operation before and after transplantation. Initial tests on home-made MESFET's showed stable DC operation. Stability tests, done on the foundry MESFET's will be given at the conference. We will then also present results on further reliability tests.

Acknowledgements : We would like to thank all people of PML/LEP which are involved in the foudry project, especially the epitaxial group, and M. Herreman for RF measurements in our group. Beside the RACE OSCAR and ATMOS project, part of this work is carried out within the U.S. Army project DAJA-90-C-0003. I. Pollentier thanks the IWONL for financial support.

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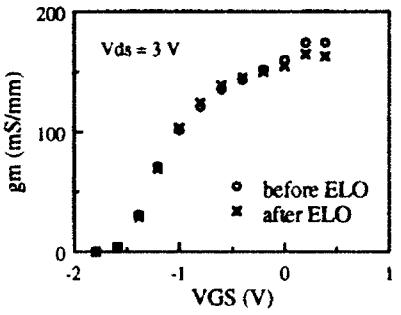


Figure 1 : G_m of foundry MESFETs before and after ELO (see text).

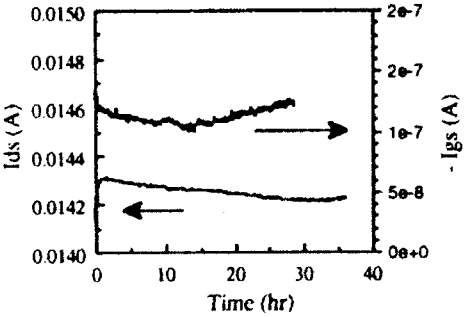


Figure 2 : Stability tests on home-made MESFET's (see text).

FB7

FABRICATION AND CHARACTERIZATION OF AN $In_{0.53}Ga_{0.47}As$/InP PHOTON TRANSPORT TRANSISTOR

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The photon transport transistor (PTT) is a device suitable for optoelectronic integration. Its structure is shown in Fig.1. It consists of a light emitting diode (LED) integrated on the top of a photodiode, with both devices sharing a common contact. This device is similar to a bipolar junction transistor: the LED acts as a light emitter whereas the photodiode forms the light collector. Photons rather than minority carriers are transported through the base region. This structure fabricated using the GaAs/AlGaAs material system was shown to behave as a bipolar transistor with current and voltage gain[1]. This device structure has also been shown to have potential for OEIC's[2] and to reduce the power dissipation within laser diodes[3].

We present for the first time the fabrication and characterization of the photon transport transistor in the lattice-matched $In_{0.53}Ga_{0.47}As$/InP material system, which is of interest for long distance optical fiber communication systems.

The epitaxial layers are grown by gas-source molecular beam epitaxy on a p-InP substrate. The structure consists of (from substrate to top): an undoped $In_{0.53}Ga_{0.47}As$ absorption layer (2μm), an n^+-InP base contact layer (500nm, $1\cdot10^{18}cm^{-3}$), an n-InP cladding layer (1μm, $2\cdot10^{17}cm^{-3}$), the active MQW layer (15 10nm $In_{0.53}Ga_{0.47}As$ wells and 14 10nm InP barriers), a p-InP cladding layer (1μm, $4\cdot10^{17}cm^{-3}$) and a p^+-$In_{0.53}Ga_{0.47}As$ emitter contact layer (30nm, $1\cdot10^{19}$ cm^{-3}). The emitted wavelength of the MQW-LED is 1.55 μm. After growth the device is fabricated by etching down to the base contact layer, etching the isolation trench and then etching a mesa which defines the light emitting region. The etchant used is H_2O:HCl:HBr:H_2O_2 (30:10:10:1). Then the ohmic contacts are defined: first the common n-contact by depositing and alloying a AuGe/Ni/Au layer and then the p-contact to the LED by depositing a Cr/Au layer, forming the base and the emitter contact. Finally a Cr/Au layer is deposited on the back of the substrate forming the p-contact (collector) to the photodiode.

The device measured has a 10μm wide and 1mm long mesa. A current-voltage characteristic is shown in Fig.2. The maximum differential transport factor α ($\approx\Delta I_C/\Delta I_E$) of the device is 0.064. The voltage gain of the device is 450. This results in a power gain of 31. These parameters were measured at I_B=-2.6mA and V_{CE}=-1.5V. The LED has a leakage current of 3nA and an ideality factor of 2.0.

In conclusion, we fabricated and characterized the first InP/InGaAs Photon Transport Transistor. The device has useful voltage and power gain. In addition, we showed that the photon transport transistor concept can be extended to material systems other than the GaAs/AlGaAs material system.

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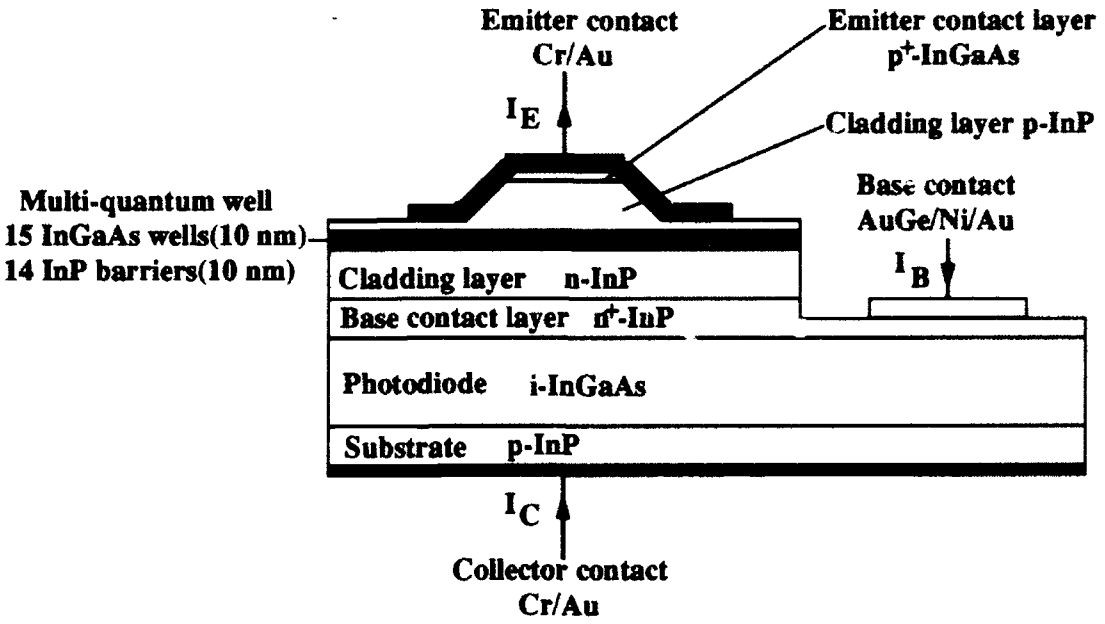


Figure 1. Vertical structure of the Photon Transport Transistor

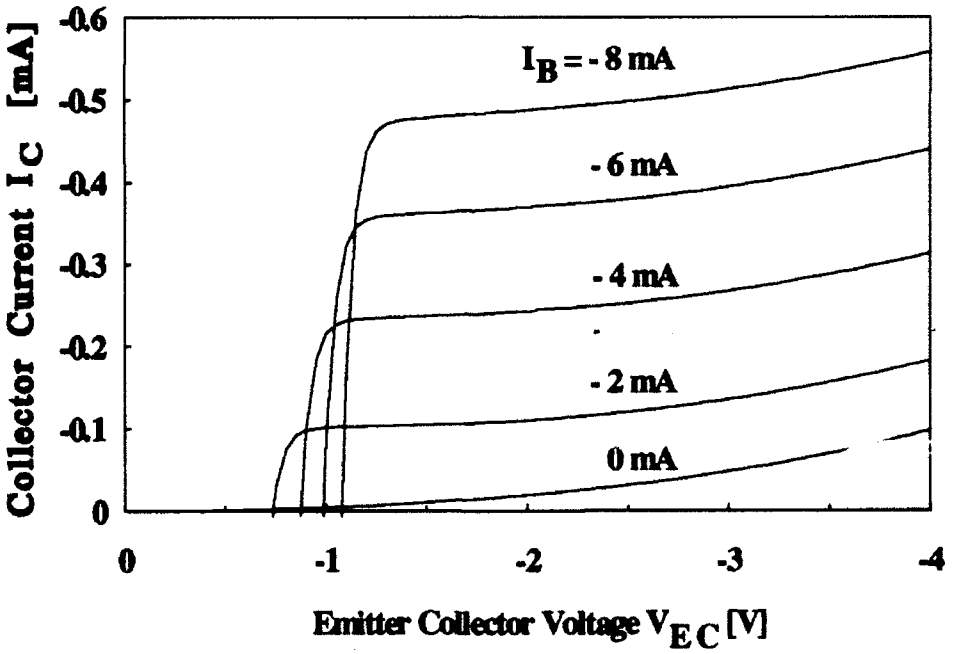


Figure 2. The Current-Voltage Characteristics of the $In_{0.53}Ga_{0.47}As$/InP Photon Transport Transistor.

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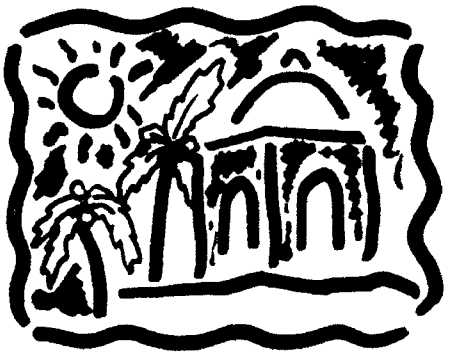
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Smart Pixels

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Monday

August 10, 1992

MA: Smart Pixels

MB: VLSI/Liquid Crystal SLMs

MC: Optical/Electronic Device Integration

MD: Vertically Integrated Devices

MA1

3-D COMPUTERS WITH SMART PIXELS

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Introduction

Traditionally, smart pixel arrays have been viewed as optical source or modulator arrays wherein each source or modulator has some associated electronics capable of performing a limited number of logic operations. This has led to such envisioned applications as smart switching nodes for data communications systems. As more and more electronics is associated with each pixel, a broader range of applications comes into view. One of these is to provide optical interconnections in what is becoming known as 3-D computers, very fine-grained parallel computers consisting of circuits stacked on top of one another rather than side-by-side on printed circuit boards or multi-chip modules. It is this application of smart pixels that is the topic here.

3-D Computers

Three-dimensional parallel computers consist of stacked planar arrays of electronic circuits that are interconnected directly between the planes rather than via boards and backplanes. Since optics can image two-dimensional light patterns from one plane to another, the prospect of interconnecting two planes of electronic circuits via thousands of free-space light beams between the planes is an exciting alternative to electrical connections. However, this excitement must be tempered by the progress that electronics has made in recent years in achieving interconnections in the third dimension (vertical to the boards). A most interesting electronic approach is the 3-D Computer under development at the Hughes Research Laboratories (HRL).[1] By stacking the computational units in the third dimension rather than spreading them out horizontally on a board, the average interconnect length decreases significantly, resulting in reductions in interconnect delays, and alleviating problems associated with memory-access/logic-cycle-time discrepancies. In addition, the 3-D concept avoids costly and space consuming packaging, especially at the board level.

Why Optical Interconnects in 3-D Computers

In addition to the many advantages of optical interconnects in general, such as electrical isolation, freedom from ground loops, independence of drive power and interconnect length, freedom from electromigration, and freedom from capacitive loading, there are the following significant advantages to be gained in the context of 3-D computers.

Hundreds of thousands of crosstalk-free, high bandwidth channels
Greater ease of cooling
Easy replacement of defective arrays
Availability of a wide range of interplane interconnection patterns
Interconnect reconfiguration

The massively parallel interconnection between the planes of a 3-D computer is consistent with the imaging capability of optics to handle hundreds of thousands of parallel channels operating at bandwidths well in excess of 1 GHz without crosstalk. But even more important may be that optics permits the processor planes to be further separated in space since optical interconnects, unlike their electrical counterparts, do not have a speed and power penalty for traversing longer distances. The real payoff is that cooling of the processor planes becomes

easier. Heat removal has been a major problem that has plagued designers of 3-D computers to date, and has lead to unfortunate compromises such as lower operating speeds and less than 100% usage of the available processors at any given time.

In addition, free-space optical connections lead to the easy replacement of defective planes due to the absence of physical plane-to-plane contacts. With 100% free space optical interconnection between planes, realignment is the only major task in replacing processing planes. This is in stark contrast to an electrically connected 3-D computer where hundreds of thousands of electrical contacts need to be broken.

An even stronger argument for using optical interconnects in 3-D computers is the ease with which optics can implement a wide range of interconnect patterns between planes. Due to the minimal space between electrically interconnected planes in 3-D computers, interconnections to date have only involved regular mesh networks. This is very constraining for many applications, especially medium and high level image processing. For example, a recent study[2] found that optical interconnects in the Hughes 3-D Computer could provide a speed-up factor of about 60 for bitonic sorting computations on a 512 x 512 processor array.

Free-space interconnected 3-D computers can be reconfigured by changing the hologram between the planes. Potential schemes for hologram modification include the recording of multiple patterns in optical storage (e.g., on a rotating optical disk) and the use of read/write holographic media such as photorefractives and third-order nonlinear optical materials.

Smart Pixel Arrays for 3-D Computers

Since the 3-D computer application of smart pixels requires what one might call "very smart" pixels, the near-term emphasis is on silicon electronics with its high levels of integration. There are two modulator-based smart pixel arrays with silicon electronics that have been demonstrated - lead-lanthanum-zirconate-titanate (PLZT)/Si and ferroelectric liquid crystal (FLC)/Si. However, for 3-D computer interconnect applications, these smart pixel devices may be too slow with their MHz speeds. On the horizon is an option to replace the electro-optic modulators with vertical-cavity surface-emitting laser (VCSEL) diodes. VCSEL arrays have the potential for realizing optical interconnect speeds for 3-D computers in the multi-GHz range. Optical interconnects running at 1 GHz in a 128 x 128 3-D computer with just one VCSEL per pixel would result in a plane-to-plane data transfer rate in excess of 16 terabits per second.

Combining VCSELs with silicon electronics may prove more difficult than combining the PLZT or the FLC modulators. Although the growth of III-V materials on silicon may eventually lead to monolithic arrays, the nearer-term solution will likely involve the flip-chip bonding of the VCSEL arrays onto VLSI chips. Optical interconnect speeds in excess of 100 MHz should be possible with such hybrid structures, probably more limited by the silicon electronics than the optoelectronic packaging.

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MA2

A SIMPLE, TWO STAGE, TWO DIMENSIONAL OPTOELECTRONIC PROCESSOR/INTERCONNECTION USING SMART PIXELS

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A common problem confronting the realization of optoelectronic processors over the last several years is the ability to both perform logical operations (i.e. computions) and rapid, dynamic reconfiguration of the processor in a compact and simple manner. For example, while optical computers have been demonstrated on several occasions over the last several years, they have suffered from a lack of reconfigurability, thus limiting their ability to solve arbitrary problems. On the other hand, dynamic interconnections which have been proposed generally lack computational power.

In recent work in our laboratory, we demonstrated a fully integrated optically powered, optoelectronic "smart pixel"[1]. This circuit had the ability to operate variously as an optoelectronic amplifier, bistable switch, inverter and latch. By a minor variation of that circuit, we can employ it in a novel, and very simple optoelectronic processor which has the ability to both perform logic and dynamically route large 2D arrays of data. In effect, we discuss an architecture employing 2D arrays of smart pixels which can solve a wide range of computational and interconnection problems at very high rates.

The key to the processor is shown by the circuit in Fig. 1, which is similar to the circuit demonstrated by Brown [1]. By changing the bias states on the 5 control transistors (I_{c1} - I_{c4} and I_{pb}), this circuit has the ability to operate variously as an AND, OR, NAND, NOR, or INVERT gate to optical beams input into phototransistors In_1 - In_4. In addition, as has been shown in past work, providing positive optical feedback to the control transistors allows this circuit to self-latch. Finally, pairs of such circuits can be simply employed to form a bypass/exchange switch. In summary, this single, simple optoelectronic smart pixel can perform all required Boolean algebraic functions as well as routing of data.

Now consider the 2 stage folded optoelectronic system shown in Fig. 2. Such purely optically folded systems have been suggested as a means to efficiently implement optical interconnects in multistage Omega networks [2]. Fig. 2 represents a 2D optical processor that can perform many complex switching or computational functions. In the figure, PA = smart pixel array, L = latching array. Also, M represents mirrors or other optical elements used in directing the array of beams. They may be semitransparent to allow for the insertion of masks or other instruction sets which could optically program the control transistors (which might be optically sensitive as well), or to introduce optical power to the pixel arrays [3]. Whether L and PA are separate arrays or are combined does not change the utility or concept of the system. The purpose of L is to hold the output from the previous stage for 1 clock cycle.

The system works as follows, keeping in mind that any arbitrary digital logic processing function is done by iterative logical steps which are a sequential combination of calculation and routing. First, an array of data is input to PA_1 which is configured to perform the first logical computation on the first clock pulse. Then on the

second clock pulse, the data is advanced to PA_2 (from the latch L_2 which holds the result of PA_1). During this same clock cycle, the "control" reconfigures PA_1 to perform the 3rd computational or routing function, and so on. Thus, during each clock cycle, one array performs a function while the other array is reconfigured (either optically or electronically) for the next computational step. The latches act as short term memory since the calculational time (~1ns) is much longer than the data transfer time (~1ps). As noted, the latch and adjacent PA can be combined in a single circuit with positive feedback.

The number of stages now is reduced from ($n \log_2 N + n$) to only two, no matter how complex or large the system is. Here, n is the number of steps needed for the calculation, and $n\log_2 N$ is the number of interconnection steps required. We note that the same number of cycles is probably needed in a "linear" system as well. However, in the proposed system, the optical alignment problem is greatly reduced, since only two arrays need to be aligned independent of problem complexity.

One requirement for system operation is that $\eta_c G \geq 1$ where η_c is the optical coupling efficiency between stages, and G is the optoelectronic gain of each pixel. As previously demonstrated [1], G = 11 is *easy* to achieve. Ideally $\eta_c G = 1$, otherwise at $\eta_c G > 1$ the system becomes unstable, or the signal attenuates for $\eta_c G < 1$. However, $\eta_c G = 1$ is also easy to achieve for saturating (or limiting) circuits, of which Fig. 1 is an example due to the presence of R_L. It is clear that many variations to this basic concept can be implemented to provide many different functions at different performance levels (i.e., bandwidths, clock rates, etc.), depending on the particular circuit configuration or device technology (including SEED) employed. Some of these variants, and other performance limitations will be discussed in the talk.

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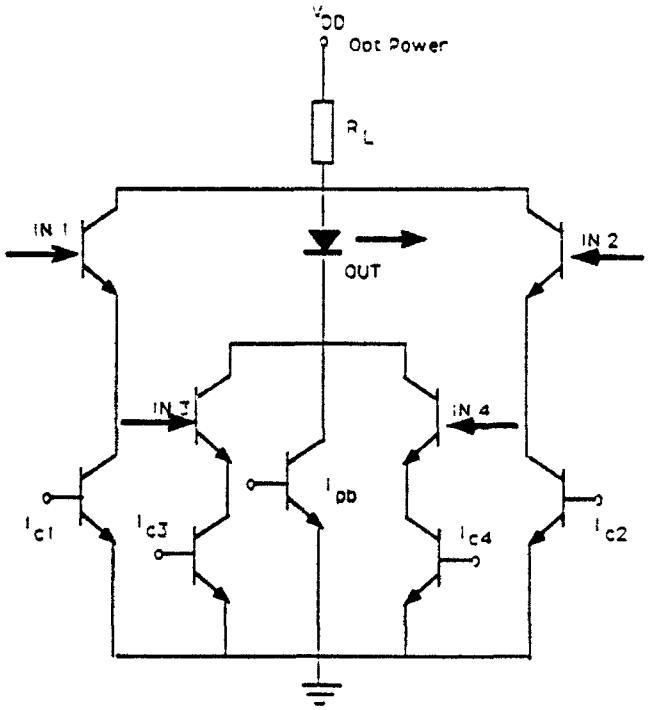


Figure 1

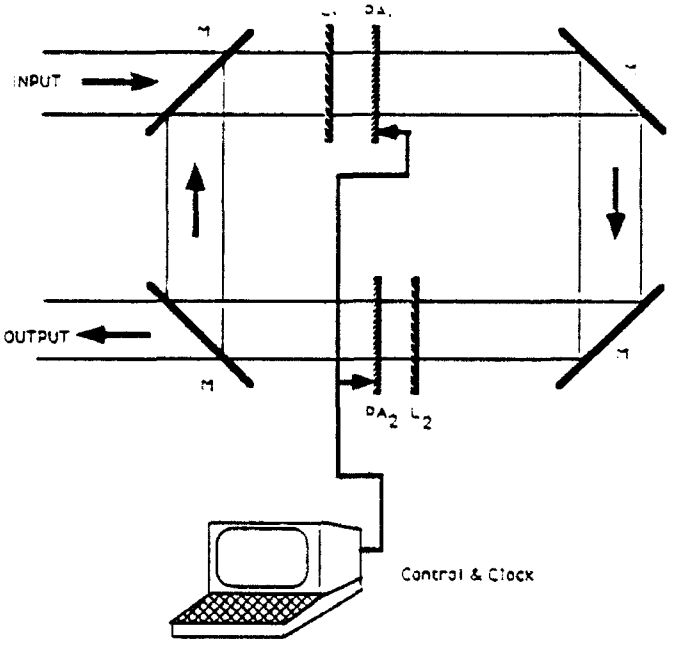


Figure 2

MA3 SMARTER SENSOR PIXELS THROUGH GEOMETRY CONTROL

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Data acquisition in optical metrology is usually performed with linear or two-dimensional regular (rectangular) arrays of photosensitive sites (pixels), such as photodiode lines or CCD image sensors. The extremely regular spacing of the individual detector elements provided by the lithographic step in production allows very accurate localization of image structures on the sensor array with a precision of better than 1% of the pixel-to-pixel spacing [1]. In many problems of optical metrology, however, some *a priori* information about the image image structure of interest is known. In these cases, adaptation of the sensor geometry to the particular problem greatly simplifies image data acquisition and processing.

A first step in this direction was the "low cost smart camera" [2] which, under *software control*, allows to select pixels in an optimum order for rapid processing at video field rate (60/50 Hz).

Much more can be done if the sensor and pixel geometries are tailored to a specific problem. An example of this is active triangulation in the form of light sectioning for the acquisition of the three-dimensional (3-D) shape of objects, where the centroid of light stripes must be determined. If the image is sampled by a conventional image sensor the whole image has to be digitized, stored in memory, and processed. For a high-speed low-cost 3-D camera, a linear photodiode array was modified with a special chrome mask to obtain a linear array of triangularly shaped photodiodes [3]. The signals of two adjacent pixels of this array can rapidly be evaluated with simple lookup-table operations to obtain the center-of-gravity of the line image. Depth maps with 250v×125h pixels and an accuracy of about 3% of the depth range are generated at video rate (CCIR video signal with 50 fields per second)

Smart photodetectors which perform signal processing in the optical domain by their geometric shape can be realized with simple means and at high accuracy as so-called photo-ASICs using standard CMOS process [4]. Photodiodes fabricated with an inexpensive single-metal single-poly CMOS process (SACMOS 3, FASELEC Corp., Zurich) showed a high external quantum efficiency of up to 80% and a good uniformity of sensitivity over the light-sensitive area as documented by a non-linearity of PSDs (position-sensitive devices) of only 0.25%. Virtually all geometrical shapes of the light sensitive area can be realized. The only restriction is imposed by the smallest feature

size defined in the design rules of the semiconductor process. We have found, however, that e-beam produced masks with unusal, non-rectangular structures will in general be reproduced with a precision exceeding the smallest feature size.

This feature was exploited in the realization of an array of four sinusoidally shaped photodiodes performing a complex Fourier transform at a single spatial frequency. The application of the sensor is the high-speed detection of the relative phase of a grating image.

A specially shaped photodiode was designed and fabricated for the application in a single-chip planar triangulation range-finder. Due to its specific shape the detector will produce an output voltage which is linearly dependent on the measured range.

Geometry-controlled smartness of photodetectors can also be made dynamic. We have investigated special CCD image sensors fabricated with the CCD process available from Orbit Inc. (USA). By providing more clock lines in the horizontal and vertical direction, photogenerated charge can be summed over given areas by clocking the lines suitably. In this way the size and shape of the individual pixels can be determined purely electrically. Another CCD has been studied, the "optical lock-in" CCD image sensor, in which the photosensitive pixels are periodically "hidden" under an opaque light shield by applying appropriate clock signals.

In this work various novel photo detectors were realized and are currently under characterization. As shown by others, see for example [5], we are currently adding digital control logic (e.g. multiplexers) on the detector chip as well as circuits for signal processing like integrators, operational amplifiers and A/D converters. The combination of specially shaped photodetectors for optical pre-processing or temporally modulated photo detectors with dedicated analog and digital electronics on a single substrate will be a powerful tool for the realization of low-cost, robust and high precision systems in optical metrology.

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MA4

A HIGHLY LIGHT SENSITIVE MONOLITHIC OPTO-ASIC FOR 128 CHANNELS

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1. Introduction

Optoelectronic is already well established in communication circuits not only for interconnections over long distances *between* data processing systems, but also over short distances *within* data processing systems /1/. It is a useful technology for this application because it handles high data rates, eliminates ground loop problems by isolating transmitters and receivers electrically, avoids crosstalk along the communication line (albeit not at its terminals), allows parallel communications by using imaging systems or fiber bundles and - in the future - will dissipate less energy, thus allowing for higher packing densities than conventional electronics by resolving problems with impedance matching /2/.

From most of the advantages one can only take profit if an *integrated* optoelectronic technology is applied. For the receivers, for example, this technology is necessary to obtain low input capacities in the front end. A monolithic opto-ASIC for parallel receiving of 256 optical channels was developed. It provides high light sensitivity (-40 dBm), a channel data rate of 10 MBit/s at a BER of 10^{-9} and finite state machines for exchange/bypass logic.

Applications both in shortrange, parallel optoelectronic data links and in selfrouting sorting networks are presented.

2. The Optoelectronic Receiver IC (opto-ASIC)

The functional diagram of one logical channel of the receiver chip is shown in Fig. 1. There is an array of 8 x 16 logical channels on the chip each of them including 2 photodiodes, an amplifier, latches and the logic for a finite state machine for two neighbouring channels for the application in sorting networks. At a data rate of 10 MBit/s per channel (worst case), an overall data throughput of about 1 GBit/s through one chip is achieved. The system is also running at higher frequencies, but our setup limited the maximum data rate to approx. 20 Mbit/s/channel.

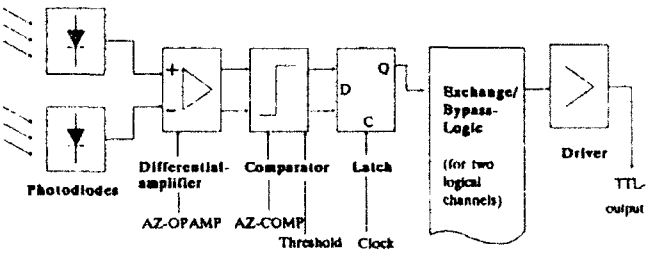


Fig. 1: Block diagram of one channel of the opto-ASIC

To provide high signal-to-noise margins, a differential concept was used both in the optical part and in the receiver. Stray light impinging with the same intensity on both receiver diodes does in principle not affect the performance of the system. In addition to that, drift effects due to thermal shifts can widely be compensated in the receiver electronics.

The complete receiver front end is fully custom designed. So it was possible to achieve a very high sensitivity. We measured a sensitivity of the receiver of 10 fJ/bit correponding to a light power of -40dBm at a bit error rate much smaller than 10^{-9} even under worst case conditions. This corresponds to roughliy 30.000 photons per bit and is only 50 tines larger than the thermal noise margin at room temperature.

The very high sensitivity was only made possible by the use of a completely symmetric, differential input stage and by providing an auto-zero adjustment at every clock cycle. Fig.2 shows the geometrical layout of

two logical channels. The dimensions had been choosen for a simple alignment and for providing direct coupling of a multimode fiber array onto the chip. The four large grey areas are the photodiodes (150 μm x 150 μm, pitch 420 μm).

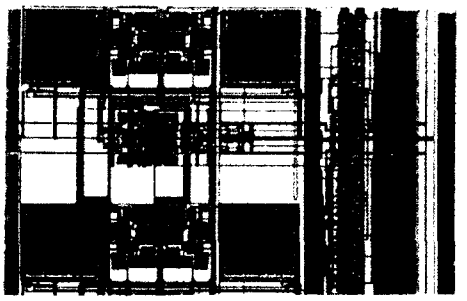


Fig. 2: Layout of a fraction of the opto-ASIC

3. The application for a data link

Using the ASIC, a multimode fiberbundle of 16 x 16 fibers and a light emitter array, we realized a point-to-point interconnection for applications in multiprocessor systems /3/. Both surface emitting laserdiode arrays /4/ and monolithic LED arrays /5/ had been applied. LEDs can be used because of to the high sensitivity of the receiver.

The mechanical tolerances within which a fiber array (NA = 0.21) has to be placed above the receiver photodiodes on the ASIC had been calculated. The geometry is tolerant to some misalignment (± 50μm axial and ± 25μm lateral) even for 100% coupling efficiency. Therefore, a reasonably priced fiber array connector with moderate tolerances can be designed.

4. Application in a selfrouting sorting network

A multistage sorting network /6/ was set up experimentally. It consists of three stages, each with a laserdiode-array, an optical permutation stage (perfect shuffle) with two multifacet-holograms and the opto-ASIC as electronic exchange/bypass (e/b) -boxes. The finite state machine inplemented in the ASIC provide self-routing, e.g. the data packages which have to be fed through the network are preceded by an adress header which switches the e/b boxes and guide the packet correctly through the network.

5. Limits and Perspectives

Such 2-D parallel optoelectronic systems are limited in their overall data throughput per area by two factors: The receiver sensitivity, that is the number of photons per bit that are required to obtain a good BER. With our system, we are fairly near to the physical (thermal noise) limit. Secondly, the light which can be emitted from a source array is limited by the heat which can be removed from a given area. We calculated that with laserdiode-arrays and a point-to-point interconnect, a data throughput in the order of 10^{13} Bit/(s cm^2) may be achieved.

We would like to thank M. Schwab, C. Potrykus, U. Danzer, M. Breunig, J. Evertz and E. Göbel for setting up the optics and electronics.

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MB1

MODULATORS AND DETECTORS FOR VLSI/FLC SMART SPATIAL LIGHT MODULATORS

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By overlaying a silicon die with chiral smectic liquid crystals a range of versatile electro-optic modulators can be embedded in silicon VLSI circuitry (VLSI/FLC). The extensive electronic functionality of silicon VLSI and its ability to be formed into sensitive photodetectors can then be directly combined with modulators that may manipulate the intensity, phase or polarization state of incident light beams.
Here we will discuss various electro-optic effects and some aspects of the charging phenomena and DC balancing requirememts which are associated with the switching of chiral smectic liquid crystals. An account of some addressing schemes appropriate to smart pixel applications and the measured performance of some CMOS compatible photodetector arrays will also be given as will measures to enhance the optical quality of electro-optic modulator mirrors.

Electro-optic effects

Table 1 summarises some measurements of response time and contrast (at 633nm) for a range of electro-optic effects associated with chiral smectic liquid crystals available to us.
The effects listed in column 1 under 'bookshelf', 'high tilt', and 'chevron' are binary effects mainly distinguished by a change in effective tilt angle. The 'distorted helix' and 'smectic A' are analog effects. To a first approximation the liquid crystal behaves like a sheet of optically uniaxial material whose optic axis is in the plane of the liquid crystal layer. Electro-optic switching results in the rotation of the optic axis in the plane of the liquid crystal layer, by an angle 2θ (column 2 of table 1) whenever the polarity of the applied voltage is reversed. This leads to the possibility of both amplitude and phase modulation (columns 3 and 4).

Charge effects in chiral liquid crystal switching

The inherent DC operation of chiral smectic liquid crystal switching and the charge associated with the ferroelectric dipole leads to important limitations when switching is by active backplane devices. In particular the minimum line address time for maximum response (τ) below a critical Ps (dipolar charge per unit area) depends only on the time constant for charging of the pixel and is independent of Ps. Ps^{crit} is given by :-

$$Ps^{crit} = CV/2A$$

where C is the effective total capacitance associated with the pixel, V is the voltage applied to the pixel and A is the pixel area.
If $Ps>Ps^{crit}$ then τ increases. However to achieve small optical response times (t) a high Ps is preferred. A calculated minimum value for t with $Ps<Ps^{crit}$ based on an optimisation of known materials (using a minimum viscosity of 10cP and a Ps of $30nCcm^{-2}$ and a 10V switching pulse) is 5μs. This is for the full optical effect. If smaller tilt angles are acceptable faster operation is possible.
For analog switching and for digital switching where insufficient charge to fully switch the liquid crystal pixel is supplied then the final optical state will not correspond to the maximum response. A range of different behaviours are observed for the various electro-optic effects after relaxation[1].
As for nematic liquid crystals long term stability depends on maintaining charge balance. This is more difficult in the case of chiral smectic liquid crystals as the liquid crystal responds to voltage polarity changes unlike nematic liquid crystals. Schemes to maintain charge balance whilst maintaining optically continuous images may include blanking or alternating inverse polarity scans. The use of bistable electro-optic effects can significantly alleviate the problem.

Smart pixel devices

The elements of a general case smart pixel are shown schematically in figure 1. The main addressing constraint is that DC balance must be maintained. To this end pixels are only addressed when information needs to be changed. Bistable electro-optic effects are required for continuous optical access to the modulators.

Building blocks for smart pixel devices are being designed under a U.K. LINK programme. A typical test structure is shown in figure 2. This device has an optical input via a CMOS compatible photodetector; a transimpedance amplifier to turn the photocurrent into a usable voltage; a controllable threshold circuit; and a liquid crystal modulator. The device is designed to act as a neuron, summing optical inputs, taking a threshold and producing a binary output via the liquid crystal modulating pad depending on whether the optical inputs are above or below threshold.

The circuit illustrated is designed to detect optical signals as small as 10 nW, threshold at one of 64 levels, and operate at a bandwidth of 100 kHz with a bit error rate of less than 10^{-9}. Preliminary measurements confirm that this has been achieved. The design is not optimised and in final devices most of the circuitry will be placed under the modulating pad.

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	Electro-optic Effect				Materials	Measurements			
	Chiral Smectic Effect	Switched Angle 2θ (Approx)	Modulation (Max Transmission)			Switching Speed			Contrast Ratio for Amp. Mod.
			Intensity	Phase		Response Time	Temp	Volts	
1a)	Bookshelf	45°	Binary (100%)	Binary (50%)	BDH SCE13	90 μs	30°C	20	2000:1
1b)					chloroester C8	2 μs	50°C	20	
2	High Tilt	90°	-	Binary (100%)	Chisso 2004	140 μs	25°C	20	-
3	Chevron (Memory)	16°	Binary (28%)	Binary (7.6%)	as 1a)	8 μs	30°C	20	1000:1
4a)	Chevron (With V)	45°	Binary (100%)	Binary (50%)	as 1a)	90 μs	30°C	20	>2000:1
4b)					as 1b)	2 μs	50°C	20	
5	Distorted Helix	0 to 45°	Analog (100%)	Analog (100%)	Roche FLC 6200	30 μs	25°C	1.5	0 to 30:1
6a)	Smectic A (Electro-clinic)	0 to 45°	Analog (100%)	Analog (100%)	as 1b)	θ=20°/3μs	53°C	10	0 to 1500:1
6b)					chloroester A9	θ=2°/0.1μs	78°C	20	

Table 1. Some measurements on chiral smectic liquid crystal electro-optic effects

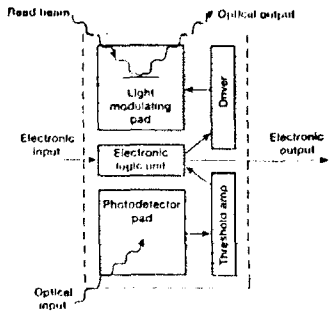


Figure 1. Smart Pixel: General case

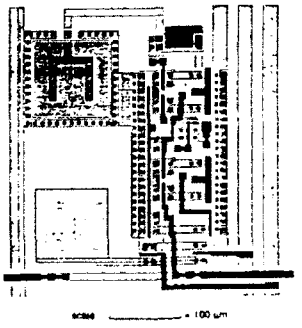


Figure 2. Smart pixel circuit, incorporating a photodiode (top left), transimpedance amplifier and thresholding circuits (right) and modulating pad (bottom left)

MB2 ANALYSIS AND IMPLEMENTATION OF AN OPTICAL PROCESSOR EMPLOYING CASCADED VLSI/FLC SPATIAL LIGHT MODULATORS AND SMART PIXEL DETECTOR ARRAYS

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A variety of VLSI/FLC spatial light modulators (SLMs) have been fabricated [1, 2, 3, 4]. Although the techniques for fabricating these modulators are still being developed, we have used electrically addressed VLSI/FLC devices as the input and filter planes of an optical correlator. We describe a model for studying the influence of non-ideal device characteristics on overall system performance and in addition, we offer a solution to the problem of processing the system output.

The correlator uses amplitude modulation at the input plane and phase modulation at the filter plane. Using Jones calculus (see, for example, Ref. [5]) we can derive expressions for amplitude and phase modulation using an FLC SLM. Assuming an x-polarized input of amplitude E_{in} and a y-oriented output analyzer we find that for amplitude modulation

$$E_{off} = 0 \tag{1}$$

and

$$E_{on} = E_{in} exp[i(\gamma + \pi/2)] \cos\delta/2 \tag{2}$$

with

$$\gamma = 2\pi\bar{n}d/\lambda, \tag{3}$$

$$\delta + \pi = \Gamma = 2\pi\Delta n d/\lambda, \tag{4}$$

where λ = wavelength of illumination, Δn = birefringence, $\bar{n}$ = mean index, and d = thickness of the device. For the case of binary phase modulation,

$$E_{out} = \pm\sqrt{2}/2 E_{in} exp[i(\gamma - \pi/2)] \cos\delta/2, \tag{5}$$

where $-$ refers to E_{off} and $+$ refers to E_{on}. For an ideal device $\delta = 0$ and transmittances of 0 or 1 for amplitude modulation and ± 1 for phase modulation are realized. Real devices have thickness variations that cause δ to vary from zero and γ to change as per Eqn. (3). The types of thickness variations we have observed are small pixel-to-pixel height variations and warping of the silicon chip. We modelled the pixel-to-pixel variations as a normal distribution, and the warping of the chip as a spherical curvature. For an optical correlator system we found that the amount of warping that exists with the current devices severely limits system performance, as shown in Fig. 1.

The actual correlator system using the VLSI/FLC SLMs operates at about 1kHz. Hi-performance CCD arrays can operate at these rates, but the information provided is in a raw format, and must be processed to locate the correlation peaks. We have designed a detector array that uses a winner-take-all function combined with pixel disabling circuitry to locate correlation peaks[6, 7, 8]. The circuit design for a pixel in the detector array is shown in Fig. 2.

The array is designed to be able to sequentially send out the coordinates of multiple peaks present in an image. This technique of only considering the data of interest reduces siginifcantly the amount of data that must be handled and processed beyond the detector.

Acknowledgements:

The authors would like to thank David Doroski for assistance in fabricating the modulators and John Lazzaro for useful discussions concerning circuit design. This work was supported by the National Science Foundation Engineering Research Center for Optoelectronic Computing Systems, CDR862228 and the Martin Marietta Corporation. Graduate Fellowship support from NASA, Johnson Space Center for David Jared is gratefully acknowledged.

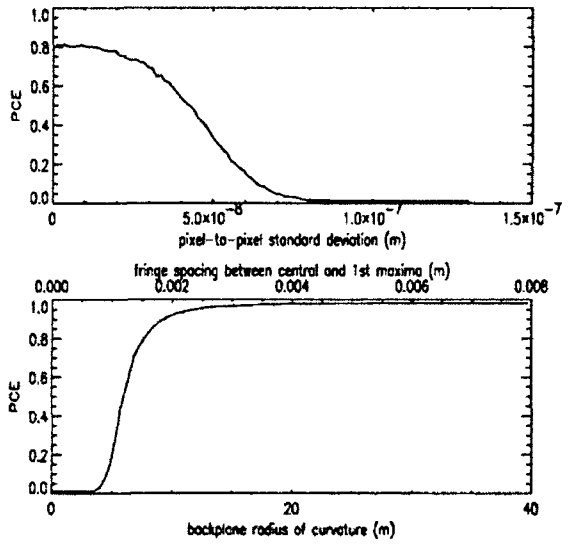


Figure 1: Peak-to-correlation energy plotted against standard deviation of pixel-to-pixel height variation and backplane radius of curvature. Top axis in lower plot indicates corresponding central to first maximum fringe spacing at $\lambda = 632.8nm$.

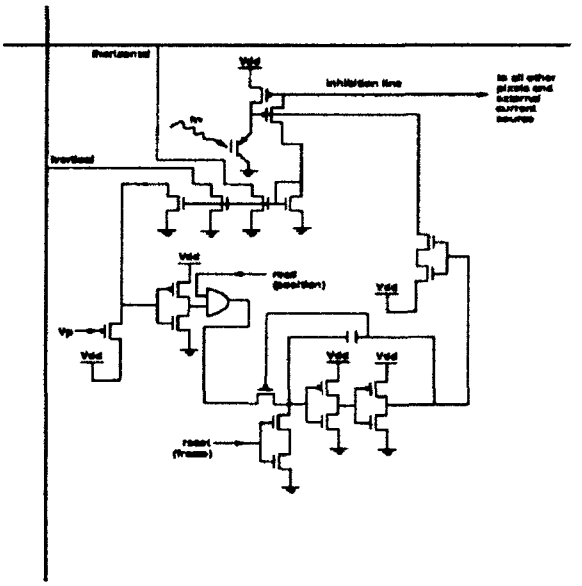


Figure 2: Circuit design for single pixel of peak detector array.

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MB3 EARLY VISION ZERO-CROSSING SPATIAL LIGHT MODULATORS

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This paper discusses several design issues surrounding building an optoelectronic system to perform early vision zero-crossing detection using VLSI, ferroelectric liquid crystal (FLC) spatial light modulators (SLMs). The SLMs consists of a VLSI CMOS backplane and FLC modulators. The FLC is sandwiched between the CMOS backplane and a sheet of glass coated with a transparent conductor.

In 1980, Marr and Hildreth [1] proposed a method of edge detection based upon locating the zero-crossings in an image convolved with the Laplacian operator and a Gaussian: $\nabla^2 g(x,y) * i(x,y)$ (see Figure 1). By examining the zero-crossings resulting from scaled Gaussians, a condensed sketch of the image can be compiled that reflects the information in the image.

Bair and Koch [2] demonstrated a one-dimensional, 64 pixel, analog CMOS chip that performed the "Gaussian" convolutions, and the zero-crossing detection. Two parallel resistive networks were used to perform the "Gaussian" convolutions. A differential amplifier followed by a exclusive-or circuit was used to identify the zero-crossings. The chip was successful, but the design does not readily scale to two-dimensions.

With an optoelectronic implementation, an incoherent or coherent optical correlator can be used to performed the convolutions, and an VLSI, FLC SLM can be designed to identify the zero-crossings. This paper focuses on the design challenges associated with building a "smart" pixel SLM to perform zero-crossing identification. A block diagram of a pixel is shown in Figure 2.

Intensity Detection: An optical correlator can perform the Laplacian of a Gaussian convolution. However, because only intensities can be be detected, it is difficult to represent negative values. The lack of negative values in turn makes it difficult to identify where the output crosses through zero. Negative values are represented by performing the positive and negative parts of the Laplacian of a Gaussian kernel separately and subtracting the resulting convolutions on the chip. The two convolutions can be spatially or temporally separated. A differential pair on the chip performs the subtraction.

Detector Saturation and Large Dynamic Range: From a systems standpoint, it is desirable to have the SLM operate over an input intensity dynamic range of at least 40 dB. However, the dynamic range of input images are usually on the order of 20 dB. An amplifier that operates over the entire 40 dB range will produce a low contrast output. Thus, the difference between the negative and positive convolved images will be small and appear similar to a zero-crossing. On the other hand, if the detector amplifier has a large gain, the dynamic range will be small, and the output will tend to saturate high or low. Again, the difference between the negative and positive convolved images will appear similar to a zero-crossing output.

To solve these problems, we use a detector amplifier with automatic gain control as show in Figure 3. This amplifier can scale its operating range to match the input intensity. If the output does saturate, the zero detection circuit has been designed to shunt off when the inputs saturate as shown in Figure 4.

Acknowledgements. Discussions with Tim Slagle, Richard Turner, John Sharpe and Kelvin Wagner were gratefully appreciated in developing this project. This work was supported by the NFS ERC for OCS, CDR862228. Graduate Fellowship support by NASA-JSC for David Jared is gratefully acknowledged.

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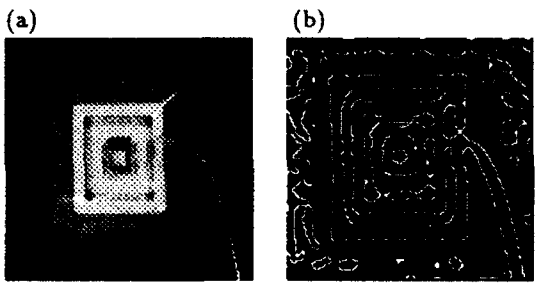


Figure 1: An example of zero crossing edge detection using a simulation. (a) Shows the input image, and (b) shows the zero crossings.

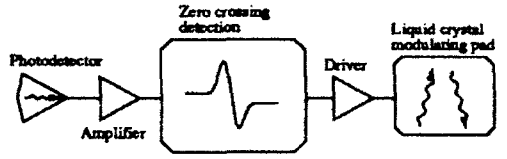


Figure 2: Block diagram of a pixel on a zero crossing SLM.

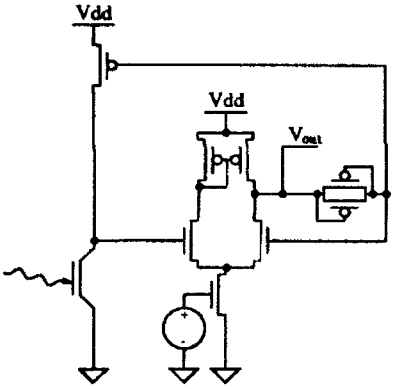
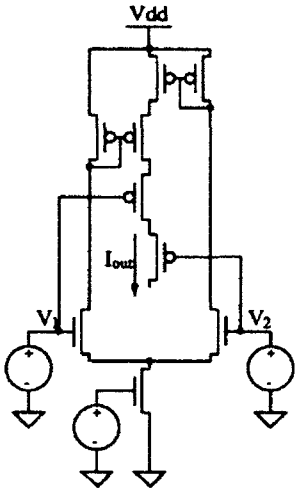
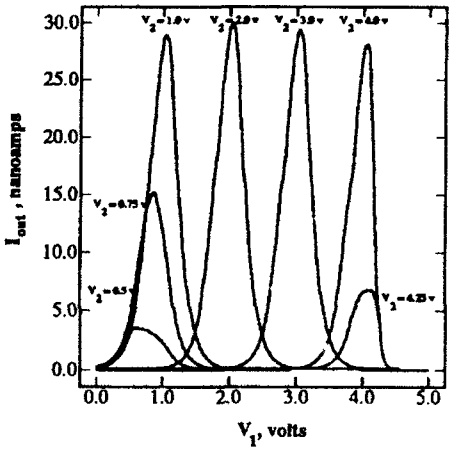


Figure 3: Schematic of an automatic gain control detector amplifier.



(a)



(b)

Figure 4: (a) Schematic of a saturation zero crossing circuit and (b) its I-V characteristics. Essentially, the circuit only generated an output current when $V_2 - V_1$ is near zero. If the detector saturates high or low (i.e. V_1 or $V_2 = V_{ss}$ or V_{dds}, the circuit does not generate an output current.

MB4 THE DESIGN OF SCALEABLE OPTICAL CROSSBAR STRUCTURES USING FELC/VLSI TECHNOLOGY AND FREE SPACE OPTICS

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1) INTRODUCTION.

The origins of the optical crossbar switch (Saw87) in the matrix-vector multiplier architecture(Goo78) are detailed in Dias et al (Dia87). A number of designs have been described (eg Dia87, Fra88). Here we suggest that the performance and compactness of space switches of this type might be enhanced by adopting a two dimensional crossbar architecture (Gro89, Kir91), and that this structure can be implemented using free space optics based on binary phase gratings, and FELC/VLSI spatial light modulators(based on ferroelectric liquid crystals integrated with silicon VLSI (Col89,Cro90,92)). Switch control functions are simplified by the use of a single stage crossbar architecture. Initial suggestions are made as to how they may be integrated into the silicon VLSI backplane of the crosspoint SLM.

Large optically transparent single stage crossbars might offer an alternative in some circumstances to switches using multistage re-arrangeable networks operating at the bit rate of the switched data (McC90).

2) FUNDEMENTAL ASPECTS OF SCALEABILITY AND PERFORMANCE.

The network analysis of Churoux (Chu87) explores the scaleability of matrix vector crossbars in terms of the inevitable fan-out loss that they share with any broadcast bus network.It does not include any intrinsic loss (Dia87) on fan-in as discussed below. On this basis, under favourable circumstances, and assuming a modulator contrast ratio of greater than 1500, it is shown that switch bandwidths might approach 10^{12} bits/s for digital signals with a BER of 10^{-12}. Ferroelectric liquid crystal modulators are capable of these levels of contrast ratio, so it is concluded that neither the intrinsic fan-out loss, or the liquid crystal contrast ratio prohibit significant scaleability.

A further limit to scaleability is crosstalk caused by the overlap of optical signals in the SLM plane. Here we propose to replace the cylindrical lenses used to perform the fan-in and fan-out in the original designs of 1-dimesional crossbars by optics that produces discrete images of the input channels in the SLM plane (see below). The input channels of the crossbar switch proposed are optical fibres, which emit tightly confined Gaussian beams. These circumstances result in a major improvement in crosstalk in the SLM plane, and allow a high density of SLM pixels to be accomodated in a modest optical aperture. Problems caused by the discrete SLM pixels are also removed. It is shown that minimum pixel spacings of less than 5 microns are compatible with crosstalk figure of the order of -30dB from this source.

Intrinsic fan in loss occurs if the effective numerical aperture (NA) of the collection channel is less than the NA and /or area of the input channels. The design proposed below greatly reduces this problem.

3) SPATIAL LIGHT MODULATOR TECHNOLOGY.

Large arrays of electro-optic modulators with very high dynamic range can be combined with integrated drive and control circuitry using FELC/VLSI technology (Col88, Cro90). Novel drive schemes and pixel circuit configurations are required to ensure that the FELC is DC balanced without allowing any disruption of calls set up through the switch (Cro92). The design and layout of a silicon backplane to implement these schemes for crossbar applications is described. This uses graded junction drive transistors, so that >20volts is available at the mirror switching matrix from a standard 3.5 micron CMOS process. This should allow a pixel reconfiguration time of below 10 microsecs with existing commercial FELC mixtures of modest spontaneous polarisation made for display applications (Cro92). An improvement of more than an order of magnitude in this time is anticipated as materials improve (assuming that limited thermostating of the silicon die will be practical).

4) SWITCH CONTROL AND ARBITRATION.

The design proposed is a full single stage crossbar, so the call routing algorithm is trivial, (there is one crosspoint mirror for each forward and each backpath). Blocking is not possible. The algorithm for avoiding external collision (arbitration) is also simple. It consists of only allowing one request per fan-in group of pixels.

Schemes are outlined wherein silicon photodetectors are built into the silicon backplane in association with each fan-out group of pixels. This will enable each user to communicate with the central switch for control purposes. The on-chip control circuitry can also be connected to a single off-chip laser diode, whose light is fanned

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out through the fan-out optics. This enables the central switch to acknowledge requests sent in by users. Schemes are discussed in which switch arbitration might be accomplished by circuitry wired into the silicon backplane.

5) FREE SPACE OPTICS FOR CROSSBAR STRUCTURES.

Matrix-vector crossbars fan-in a 1-dimensional vector. Re-arranging this so that the fan-in occurs in 2-dimensions uses the available NA of the collection optics more efficiently, and for the case of monomode fibre input channels and multimode output channels, the maximum number that can be accomodated increases from 70 to 5000. To achieve this the input and output vectors must be arranged in 2-dimensional arrays. The crossbar then acts as a matrix-matrix multiplier in which two N^2 matrices are connected through an N^4 tensor. The planar SLM spatially encodes the N^4 tensor in 2-dimensions (Kir91).

Here we propose fan-out optics using Fourier plane array generators based on computer generated holograms (CGH) consisting of binary phase gratings(Dam71,Dam90). These form multiple images of the input array in the SLM plane. They enable the overall profile across the fanned out array to be independent of the amplitude distribution of the incident beam. They preserve the ideal beam profiles of the fibre optic sources into the SLM interconnect plane, thereby allowing a high pixel density with low crosstalk. The efficiency, uniformity and scalability are all considered. A CGH with a fan-out of 32 in one dimension (ie 1024 in total) has an efficiency of 80%, and requires a phase depth error of 0.3nm. Maximum fan-out from a single CGH is limited to 100x100. Higher levels of fan-out can be achieved by cascading Fourier plane array generators (at the cost of reduced efficiency). The ultimate limitation is the space bandwidth product of the lens imaging system, not the fan out grating.

The fan in optics needs to be chosen to make the crossbar highly compact. Schemes based on lenslet arrays, and also on tapered 'photon funnels' are discussed.

Outline designs of a crossbar based on these principles are presented. It is argued that the a crossbar serving 256 users is feasible using current technology and the SLM plane need not be larger that 32mm. There is further scope for miniaturisation beyond this.

6) CONCLUSIONS.

Designs are presented for a scaleable and compact optical crossbar that is compatible with requirements in modern optical communications systems. They exploit the extremely small channel size available with optical interconnections.

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MC1

HIGH PERFORMANCE HYBRID OPTOELECTRONIC TERMINAL COMPONENTS FOR OPTICAL INTERCONNECT

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Abstract.
Optical modulator and detector arrays flip-chip solder bonded to silicon VLSI circuits are described. This hybrid approach enables optimised silicon and III-V components to be integrated to provide a near term chip-level interconnect technology.

Introduction.

Optical interconnection of VLSI circuits offers a route to overcome some of the electrical interconnection limitation experienced in very large, high complexity systems. The freedom from topological and mutual coupling constraints of optical interconnect enables the technology to impact at all levels of the system. Particularly at the chip level new interconnect and switching architectures become possible, although these are longer term than for interconnection at board and module level. However, optical interconnection at the chip level requires efficient optoelectronic interface component arrays, capable of providing highly parallel optical input and output points from an integrated circuit.

Component design and technology.

A technology based on reflective optical modulators has been chosen for the optical transmitters because they can provide efficient modulation with low power dissipation in the transmit node of the silicon [1]. Solder bond hybridization was used to attach the optoelectronic transmitter and detector chips directly to the transmit and receive nodes of the silicon circuits. This was achieved using flip-chip solder bonding which has found widespread application since its introduction in electronics. The bonds are formed by confining a controlled volume of solder between metal pads of known area on either side off the bond. These pads are surrounded by non-wettable areas so that when the solder is melted surface tension forces bring the two chips into alignment. In addition to forming the electrical connections by this technique, accurate alignment of components relative to each other may be achieved, and this method is readily extendible to large arrays (10000 bonds) [2]. The approach may be extended to attach micro-optic elements such as lenses to the optoelectronic arrays, and sub-micron alignment accuracies have been demonstrated for a three level structure comprising a silicon backplane, III-V modulator and quartz plane used to simulate a lens array. To demonstrate the application of hybrid components to optical interconnect, transmitter and receiver arrays have been fabricated using both CMOS and ECL silicon circuits.

The modulator configuration used was the Asymmetric Fabry-Perot structure [3] fabricated in the long wavelength InP material system [1] The design is illustrated in figure 1 for an inverted AFPM which exploits the transparent InP substrate for optical access to the device, whilst enabling the electrical interconnections to the silicon chip to be formed on the opposite side of the device. The structure comprises an InGaAs/InP MQW absorbing region in the cavity formed by a highly reflective metal mirror and a low reflectivity ($\leq$50%) quarter wavelength stack of InP/InGaAsP. The advantage of this approach is the use of a smaller number of periods for the mirror giving broader bandwidth and thinner epitaxial structures. A typical reflectivity spectrum is shown in figure 2 where the maximum reflectivity (on-state) at the cavity wavelength was 33%, decreasing to 11% with 5volts applied to the device. This maximum reflectivity change, ΔR_{max}, of 22% occurred at 5volts with a corresponding contrast of 4.8dB. Arrays of up to 8x8 elements on a 4mm square chip have been fabricated. The values of contrast ratio varied across the array over a

small range with a mean and standard deviation of 3.5dB and 0.25dB respectively. For the array the operating wavelength of maximum contrast ratio had a mean value of 1618nm and a standard deviation of 3.3nm. Variations in optical performance can be directly related to the uniformity of thickness of the material structures, upon which this device places particularly stringent requirements.

CMOS hybrid transmitter

Eight element modulator arrays have been hybridized onto a custom 1μm CMOS driver circuit in which CMOS logic levels are amplified to provide a 5Volt output. A high degree of uniformity of modulation was obtained across the array with mean modulation of 4.8dB and standard deviation of 0.1dB for standard CMOS input voltages. The hybrid transmitter operated to 140Mb/s with a power consumption of 0.5mW per channel which compares very favourably with the power required for an equivalent electrical interconnect.

ECL hybrid receiver

The detector arrays are based on conventional InGaAs/InP planar photodiode technology, again with substrate optical access. High efficiency low capacitance devices can then be fabricated as the parasitic capacitance associated with solder bond hybridization is very small. Arrays of upto 64 elements have been fabricated with dark current values of 46pA and standard deviation of 17 pA for 100μm diameter active areas. Eight element detector arrays have been bonded to receivers fabricated from a commercial ECL gate array [4]. The minimum input photocurrent to switch logical state was in the range 8-10μA corresponding to -23dBm. Operation up to 1Gbit/s was demonstrated with a 3dB dynamic range at 800Mbit/s and 6dB at 650Mbit/s.

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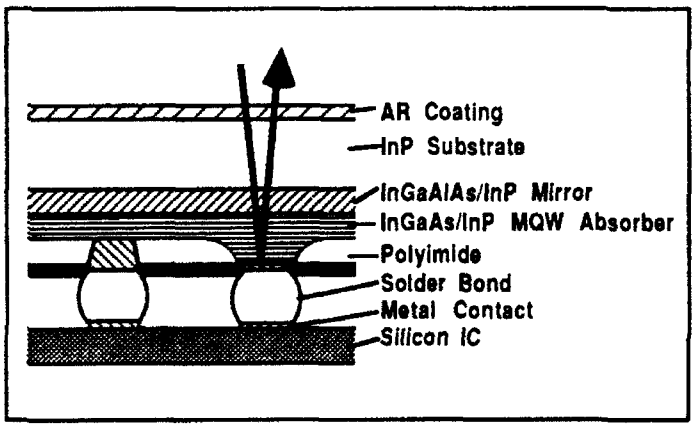


Fig. 1. Cross-sction of inverted AFPM.

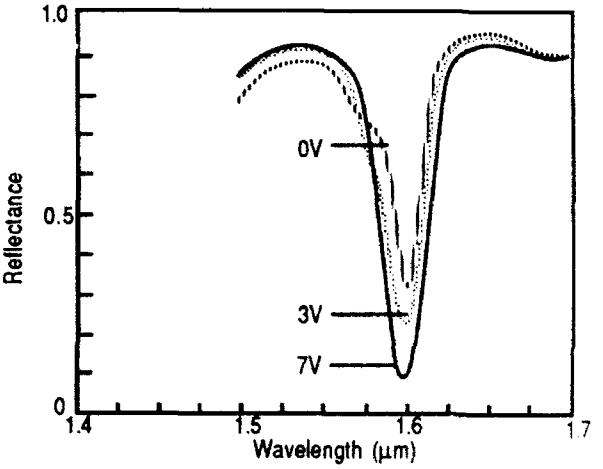


Fig.2. Reflectivity spectrum of InGaAs/InP modulator

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MC2

DESIGN AND IMPLEMENTATION OF FLIP-CHIP BONDED SI/PLZT SMART PIXELS

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Smart pixels employ materials with widely different properties for logic, detection, and light modulation. A straight forward approach is to combine these devices using a hybrid integration technique such as flip-chip bonding. Flip-chip bonding is a mature and well developed technique extensively used for silicon packaging. Figure 1. shows the cross-section of a processing element in a hybrid silicon/PLZT smart pixel. Silicon chips are placed on a PLZT wafer that is used both as a support substrate and for light modulation (Figure 2.). The driver circuitry is placed on the silicon chips and connected to the PLZT modulator using metal bumps. The silicon chips can be tested separately before placement on PLZT to insure a high yield process. The flip-chip process aligns the silicon chips to the modulators on the PLZT wafer. Since all chips use the same PLZT substrate, a chip aligned to the substrate is also aligned to all other chips on the substrate. A similar approach is being used to connect MQW modulators with Si VLSI circuits. PLZT modulators are suited for use in opto-electronic systems requiring a large dynamic range due to noise and fan-out considerations.

PLZT requires a voltage of 20-40 volts to modulate light with a large dynamic range (Figure 3.). High voltage bipolar and MOS processes are presently incapable of supporting VLSI circuit densities. On the other hand, transistor breakdown voltages in VLSI chips are too low to provide high voltage outputs directly. We have designed an amplifier circuit designed to drive PLZT with a 35 V swing (Figures 4. and 5.). The amplifier is implemented in a standard BiCMOS 2 μm process. This is accomplished using series connected transistors and a current-mirror like structure to increase the breakdown voltage of the circuit. The combination of the driver and a reflective PLZT modulator can produce light modulation with a dynamic range of 600:1. Studies of the speed response of PLZT 9/65/35 show rise and fall times of 10 ns, limited by the drive circuitry (Fig. 6).

We have also investigated the characteristics of simple optical links using flip-chip bonded smart pixel arrays incorporating PLZT modulators and will present their measured characteristics.

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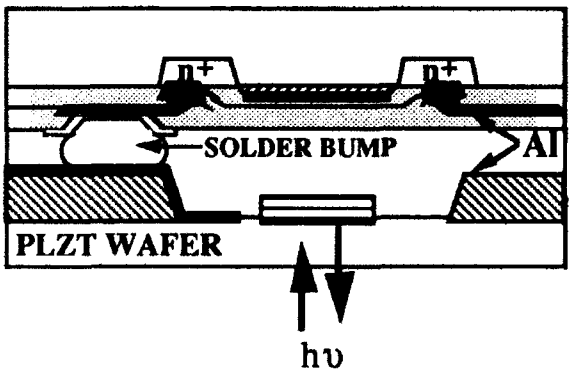


Fig. 1

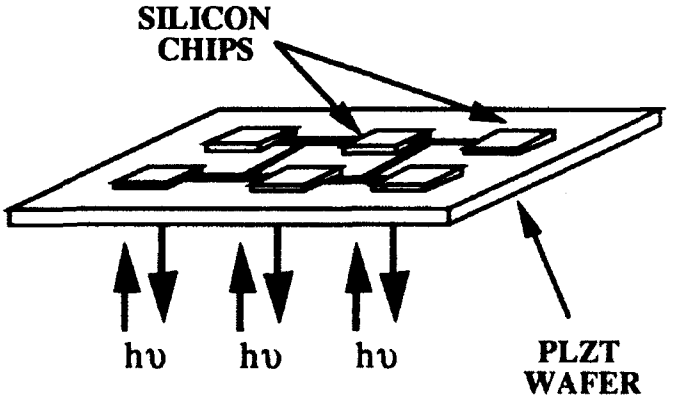


Fig. 2

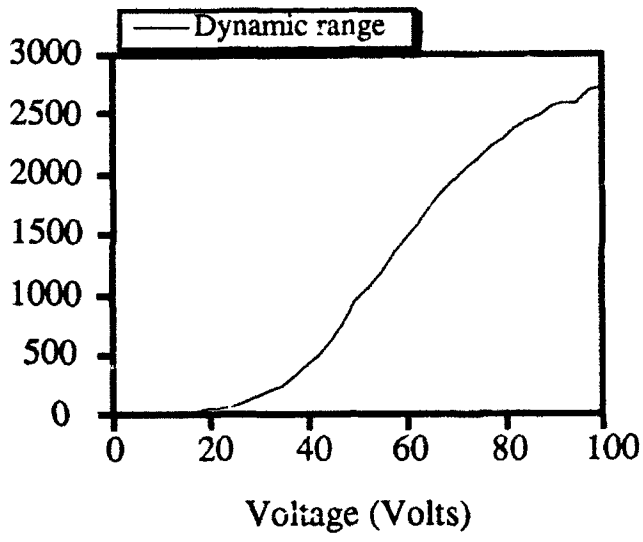


Fig. 3

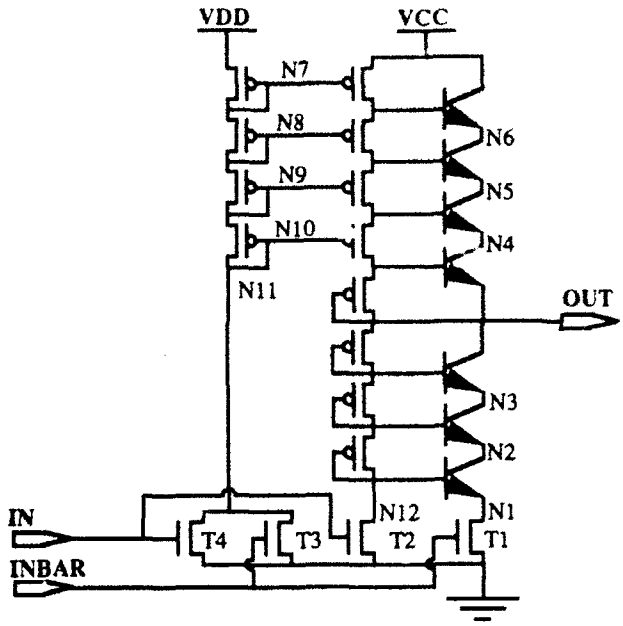


Fig. 4

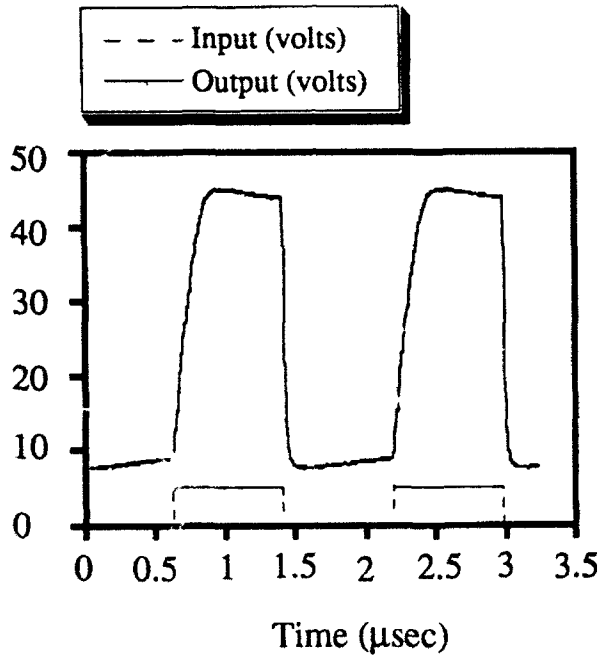


Fig. 5

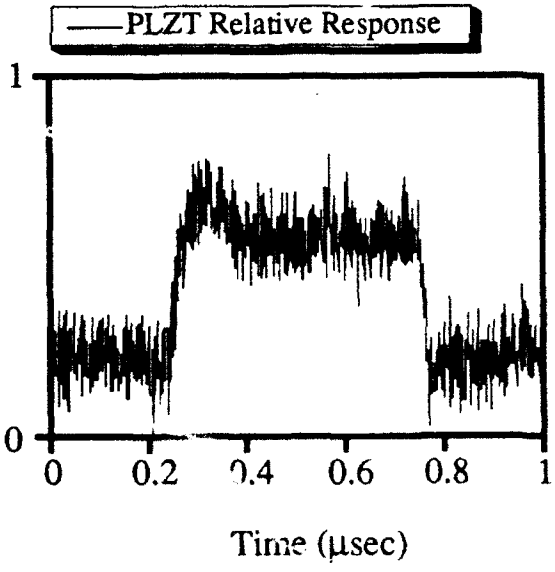


Fig. 6

MC3

THREE DIMENSIONAL INTEGRATED CIRCUITS: EPITAXIAL LIFT OFF GaAs PHOTODETECTORS INTEGRATED DIRECTLY ON TOP OF SILICON CIRCUITS

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To overcome the interconnection limitation between devices in the plane of integrated circuits, massively parallel interconnection in three dimensio s between planes of circuitry and for input/output is desirable. Using the three dimensional integration technique described herein coupled with thin film device array alignment and deposition [1], each device in arrays of thin film devices can be connected to Si circuitry for massively parallel processing. This three dimensional integration enables the simultaneous data transfer and signal processing of all data points in an array, increasing the throughput and speed of computational systems. For example, optical imaging arrays will benefit from parallel connection of each detector to signal processing circuitry, allowing imaging arrays to be large in area and in number of devices, and to have the high throughput and reduced pinout associated with the simultaneous processing of information from each pixel in the imaging array. The capability to align arrays of devices [1] also eliminates the need for wafer scale epitaxial growth uniformity for wafer scale device integration.

The three dimensional integration of high quality gallium arsenide (GaAs) optical detectors directly on top of silicon (Si) circuitry is presented in this paper. Using a modified epitaxial lift off (ELO) technique [1], a GaAs thin film optical detector is deposited on top of a layer of planarizing, insulating polyimide which lies between the detector and the Si circuitry. The detector and the circuitry are electrically connected through vias in the polyimide. This technology has potential for low cost and high performance systems since the circuits and devices can be independently optimized and tested before integration and since inexpensive prefabricated Si circuits are post processed with standard microelectronics fabrication techniques to integrate the thin film GaAs device layers only in the areas in which they are needed.

To demonstrate three dimensional integration, a GaAs metal-semiconductor-metal (MSM) detector was integrated directly on top of a simple silicon transresistance amplifier circuit [2]. Light incident on the surface of the MSM induces a current flow through the MSM, which appears as a voltage change at the gate of the first amplifier stage, which is amplified by the subsequent two amplifier stages. No attempt was made to optimize this circuit design for any particular MSM device.

To integrate the circuit and MSM device, the fully fabricated circuit was spin coated with 5 μm of polyimide. Using standard photolithography and reactive ion etching, 100 μm X 100 μm vias were etched in the polyimide, which fully exposed the underlying Al pads on the Si circuit. Gold was vacuum deposited on the etched substrate to electrically interconnect the underlying Si circuit to the top of the polyimide. The gold was then patterned for subsequent connection to the MSM.

To obtain the high quality, single crystal thin film GaAs devices necessary for this three dimensional integration, epitaxial liftoff (ELO) was employed. This technique utilizes the high etch selectivity between high Al concentration Al Ga_x As_{1-x} materials and low Al concentration alloys [3] to separate single crystal epitaxial material and devices from the lattice matched growth substrate. An array of 100 μm X 100 μm X 0.5 μm thick GaAs ELO devices was transferred to a transparent polyimide diaphragm for alignable and selective deposition [1] onto the polyimide planarized Si circuit. When the GaAs was deposited onto the host substrate, it was van der Waals bonded onto the Au fingers on the polyimide to form the MSM detector, forming a Schottky barrier electrical contact and a stable mechanical bond between the Au and the GaAs, thus completing the three dimensional structure. Figure 1 shows a photomicrograph of fully fabricated device, with the GaAs on top of the metal fingers.

The response of the circuit was tested using pulsed (square wave) 850 nm laser light from a Hewlett Packard HP8153A lightwave multimeter delivered through an optical fiber directly to the MSM. No illumination of the surrounding circuit occurred during this test. The resulting output signal was a square wave with a rise time of approximately 8 μsec and a fall time of approximately 12 μsec. This performance is typical for such a simple, unoptimized amplifier circuit. When the input optical signal was moved from MSM to the adjacent Si circuitry or when the circuit was incorrectly biased, no output signal was observed.

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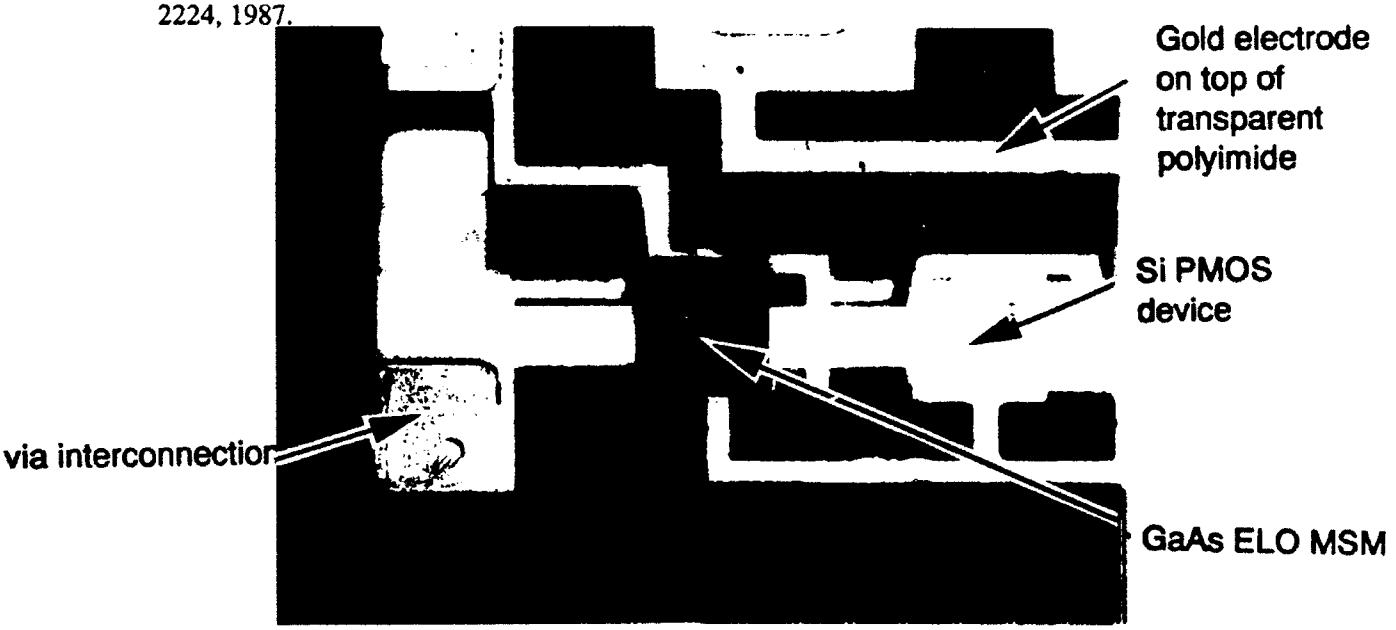


Figure 1. Photograph of the fabricated three dimensional vertical integration. The GaAs ELO material has been contact bonded to the Au MSM fingers which lie on top of polyimide planarized Si circuitry.

MC4 GaAs OEICs FOR OPTOELECTRONIC SMART PIXELS

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Monolithic optoelectronic integrated circuits (OEICs) constitute one method for implementing smart pixel arrays. GaAs circuits offer the advantage of high speed and, from a materials standpoint, compatiblity with high speed optoelectronic emitters and detectors. In addition, GaAs complementary heterostructure FET (CHFET) technologies are being developed which rival CMOS for low power dissipation. This paper will compare the available optoelectronic device and electronic circuit technologies in terms of their power dissipation and impact on the scalability of smart pixel arrays. The design, fabrication and demonstration of a 2-D optoelectronic smart pixel array will be described.

Figure 1 shows a comparison of the power dissipated per interconnect for six different optoelectronic emitter/detector pairs. The three GaAs/AlGaAs/InGaAs based emitters considered are light emitting diodes (LEDs), vertical cavity surface emitting lasers (VCSELs), and symmetric self electro-optic effect devices (S-SEEDs). These are paired with either a GaAs lateral p-i-n detector or a GaAs photoconducting detector. The analysis of the electrical power dissipated per interconnect follows that of reference 1. Above 100 MHz, VCSELs coupled with either type of detector result in the lowest electrical power dissipation per interconnect. In spite of their lower quantum efficiency and interconnect efficiency, LEDs coupled with photoconductors are more power efficient at lower speeds than are lasers coupled with either type of detector. This is due to the finite threshold current of lasers. However, S-SEEDs[2] coupled with either type of detector result in the lowest power dissipation at speeds <100 MHz. It should be noted, however, that S-SEEDs are more difficult to implement since they require several external beams per element, and cannot transmit the modulated beam through the substrate.

Figure 2 contains a comparison of different GaAs circuit technologies, and for interest, ECL and CMOS circuit technologies. Complementary technologies such as CMOS or CHFET have a clear advantage over the others in terms of power dissipation and ultimate array size and pixel complexity. Since CHFET devices currer y switch at lower voltages (1.5V) than CMOS, their switching energy is lower. CHFET also has the advantage of speed, with the capability of operating at speeds in excess of 1 GHz.

The optoelectronic smart pixel array which we have demonstrated consists of an 8 x 8 array of pixels, with each pixel containing a vertically emitting LED, an ion-implanted photoconducting detector and an 18-FET GaAs MESFET circuit which performs memory, thresholding, amplification and LED drive functions. For this first version of the array, well-developed components and a mature circuit technology were chosen in order to achieve the goal of an integrated array. In order to provide electrical input and output to and from the array, the circuit included 8 input buffers, 8 output buffers, 8 row drivers and a clock/control circuit in addition to the 8 x 8 array of pixels. The entire array contained 64 LEDs, 64 photodetectors, 1300 FETs and 500 thin film resistors. The device was produced using an epi-in-a-well process for fabricating LEDs while maintaining planarity, and an enhancement mode, self-aligned gate ion implanted MESFET process. The array is 2 mm x 2 mm and operates at 10 MHz. The LEDs emit at 850 nm with approximately 1% external efficiency without anti-reflection coatings. The photodetectors are sensitive to wavelengths shorter than 870 nm, and exhibited gain ranging from 50 at 1 μW incident optical power to 5 at 100 μW incident power.

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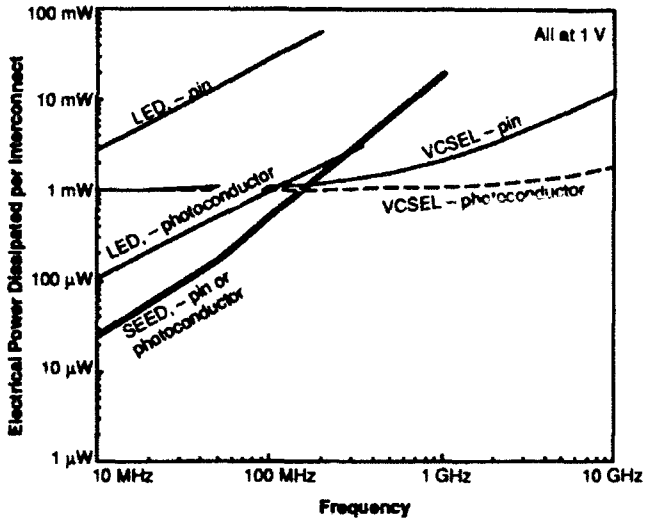


Figure 1. Comparison of the electrical power dissipated in an optical interconnect for various emitter-detector pairs. VCSEL power dissipation at threshold = 1mW; η_{ext} (VCSEL) = 0.5, η_{ext} (LED) = 0.02, SEED switching energy from reference 2, $\eta_{interconnect}$ (VCSEL, SEED) = 0.5, $\eta_{interconnect}$ (LED) = 0.05, η_{pin} = 0.35 photoconductor gain = 10.

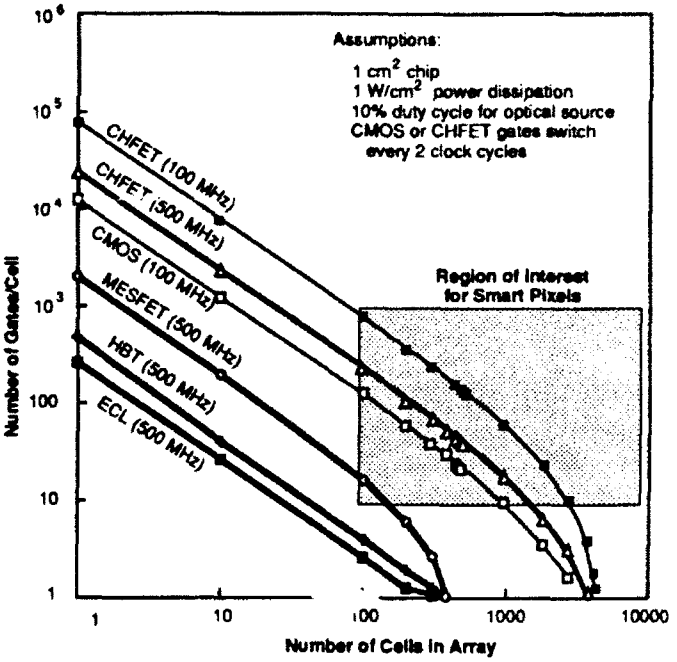


Figure 2. Comparison of the tradeoff of pixel complexity versus array size for different circuit technologies.

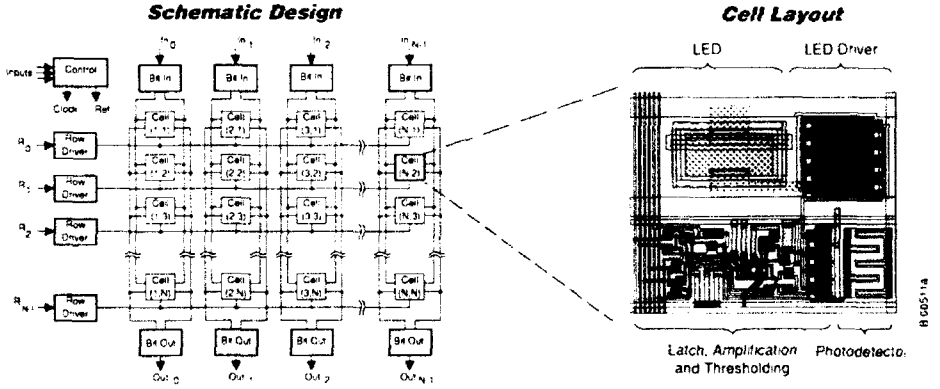


Figure 3. Block diagram and pixel layout of the 8 x 8 smart pixel array.

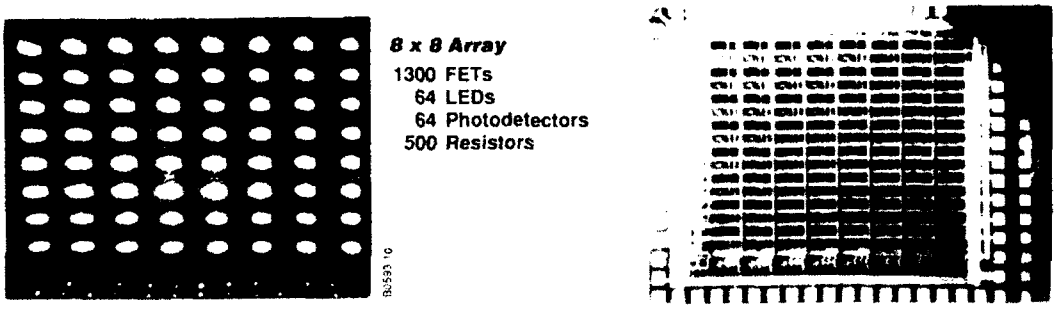


Figure 4. Optical micrograph of 8 x 8 smart pixel array and photo with all LEDs activated.

B920177-01

MD1 VSTEP OPTOELECTRONIC DEVICES AND THEIR MODULES

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Technical advances in optical semiconductor devices have permitted fabrication of two-dimensional surface-normal optical devices. Optical functional devices are foreseen to be used for highly-parallel information processing and high-speed switching. Vertical to Surface Transmission Electro-Photonic devices (VSTEPs) are concepts to allow these applications[1]. For these purposes, VSTEPs should have high E/O power conversion efficiency, and they should be combined, not only with electric circuits, but also with micro-optics. This paper describes laser-type VC-VSTEPs and their module technologies.

In LED-mode pnpn-VSTEPs, electrical-to-optical power conversion efficiency is low, and available output light power is limited by spontaneous emission. Therefore, laser-type VC-VSTEPs (Vertical Cavity VSTEPs) have been fabricated (Fig. 1). Figure 2 shows light-output characteristics for continuous wave operation for a 10 μm-square VC-VSTEP. The inset in Fig. 2 shows the current-voltage characteristics. Its switching voltage and its holding voltage are 3.5 V and 2.2 V, respectively. Its oscillation wavelength is 955 nm. Output light beams are transmitted through GaAs substrate. In laser-type surface-normal devices, it is important to improve E/O power conversion efficiency for achieving large-scale integration. We achieved 11 % efficiency which is by no means inferior to data for edge-emitting lasers.

A module consisting of an 8 x 8 VC-VSTEP array and a PML (Planar Microlens) array was fabricated for board-to-board optical interconnection (Fig. 3). Individual VC-VSTEP is addressable in this module. In order to decide focal length for a PML, and thickness of a VC-VSTEP substrate, we calculated transmitted beam profiles through a GaAs substrate and a PML. Thickness for the VC-VSTEP substrate was adjusted to 100 μm by polishing. Focal length and numerical aperture for the PML were determined 560 μm and 0.23, respectively. Individual elements in the VC-VSTEP array and the PML array were arranged with a 250 μm separation. The VC-VSTEP array was mounted on an AlN submount by using flip-chip bonding technology. Output light beams were propagated to the plane 20 mm away from the PML, and they were separated without crosstalk.

In order to fabricate modules for more advanced applications, we need optical elements with beam splitting, combining and permutation functions, as well as beam collimating and focusing functions. However, using conventional bulky optical elements, optical alignment always becomes a problem. Using computer-generated holograms and semiconductor lithography techniques, the problems are expected to overcome. We proposed D-VSTEPs (VSTEPs with Diffractive Optical Elements) in which VC-VSTEPs and diffractive optical elements are integrated[3]. They are easily aligned because both devices are on the same substrate. Figure 4 shows the D-VSTEP structure. Some light beams from VC-VSTEPs are diffracted and go out from D-VSTEP[4], and other light beams are diffracted and propagate along zigzag routes in the substrate. Figure 5(a) shows an example of the D-VSTEP, where zone plates are formed on the substrate. An output laser beam from the D-VSTEP is focused at a distance of around 55 μm from the substrate. The spot size is less than 10 μm (Fig. 5(b)). Figure 6 shows propagated light beams in the substrate. The substrate behaves planar optics. Using the D-VSTEP, beam splitting and combining between neighboring VC-VSTEPs may be performed. Such an approach as the D-VSTEP will lead to implementing smart pixels based on VSTEPs for highly-parallel information processing and high-speed switching applications.

The authors wish to thank M. Oikawa for supplying PML, and K. Kobayashi, K. Hotta and K. Asakawa for their encouragement. They also thank colleagues, M. Sugimoto, T. Numai, I. Ogura, H. Kosaka, K. Kurihara, A. Yasuda, Y. Yamanaka and S. Araki.

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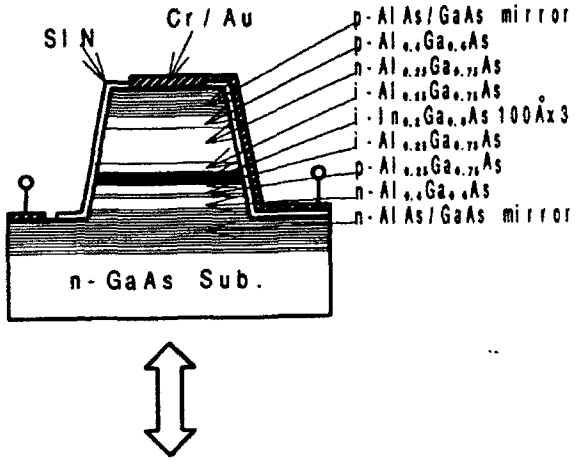


Fig. 1 Laser-mode VC-VSTEP structure.

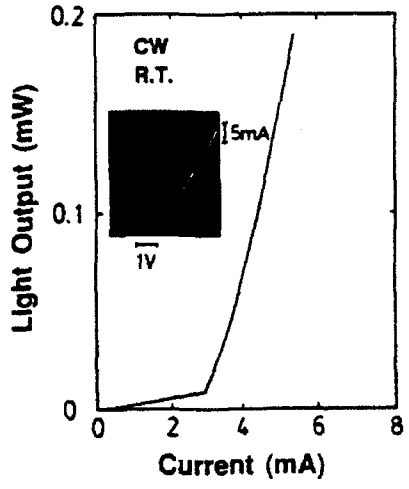


Fig. 2 VC-VSTEP L-I and I-V characteristics.

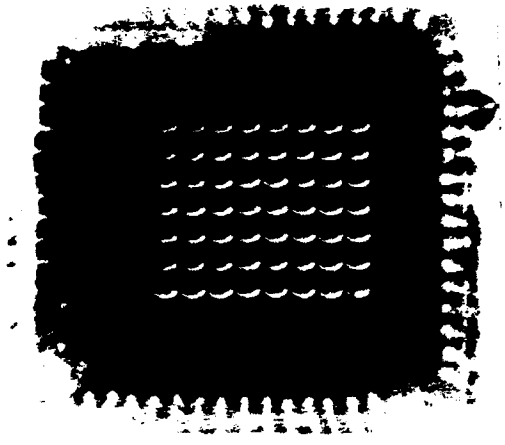


Fig. 3 Module with 8 x 8 VC-VSTEP and PML array.

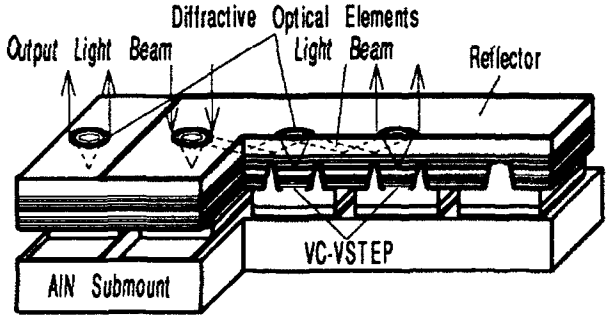
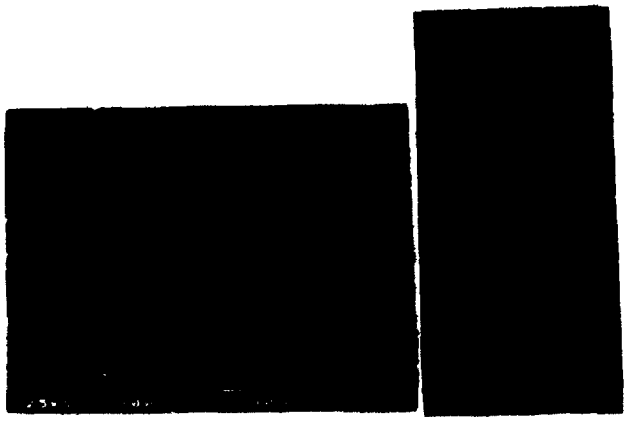


Fig. 4 D-VSTEP structure.



(a) Zoneplates on VS-VSTEPs (b) Focused beam

Fig. 5 Transmissive-type VC-VSTEPs.

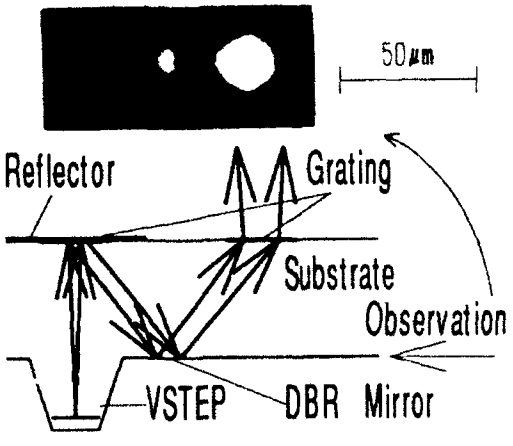


Fig. 6 Output light beams from D-VSTEP.

MD2

OPTICALLY CONTROLLABLE PIXEL BASED ON VERTICAL TO SURFACE TRANSMISSION ELECTRO-PHOTONIC DEVICES USING FOUR-TERMINAL pnpn STRUCTURE

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Surface-Emitting-Laser-based optical functional devices have promising features for photonic switching and optical data processing. All photonic switching networks need control signals to be sent into the nodes to allow for appropriate routing of traffic.[1] Control injection, thus, must be taken into consideration more in photonic switches. An optical self-routing switch has been proposed where a node consists of pnpn-Vertical to Surface Transmission Electro-Photonic Devices with Vertical Cavities (VC-VSTEPs).[2] The routing for optical data signals are controlled by an optical pilot signal placed at the head of the optical data signals. However, this switch still needs electric timing signals to be applied to the VC-VSTEPs, which might cause electromagnetic interferences among a large number of internal electric lines, and a delay in the timing signals due to parasitic capacitances. Therefore, it is desirable that the timing signals are further injected optically. This paper reports on VSTEP-based pixels aiming for optically controllable nodes.

The pixel consists of a VSTEP using a four-terminal pnpn structure with two distributed Bragg reflectors (DBRs) (Fig. 1). The fabrication process includes two-step mesa etching: 1) to the n-doped gate layer, and 2) to the n-doped DBR layer. The n- and p-gate electrodes are formed on the second mesa with Zn diffusion for the p-gate. In comparison to two-terminal VC-VSTEPs[3], the structure provides variable switching voltage characteristics and gate turn-off operation by means of carrier injection/extraction through the gate terminals. Also, this structure allows the formation of a hetero-junction bipolar transistor (HBT), or a hetero-junction photo-transistor (HPT) together with the pnpn-structure. These two features, in combination, expand flexibility in device configuration to meet the demands of photonic switching and processing systems. As an example, a pixel has been demonstrated for an optical self-routing switch with optical gating and optical reset operations. Figure 2 shows an equivalent circuit of the pixel. When the optical gate pulse is incident on the HPT1, current is injected to the pnpn device, resulting in a reduction of switching voltage, and allowing turn-on by the input optical pulse. Applying the gate pulses to the pixels with proper time delays, the pilot signal can select one pixel in which the pilot signal coincides with the gate signal. HPT2 is used for the optical reset. The optical reset pulse incident on the HPT2 removes the stored charge in the pnpn-device through the n-gate. Figure 3 shows voltage-current and light-current characteristics of the fabricated device with various current injections from the n-gate. The switching voltage without n-gate injection is 3.8 V and the threshold current is 35 mA. A common-emitter current gain of 180 is obtained for the npn-HPT using an n-gate as a collector and a cathode as an emitter.

Figure 4(a) shows the optical gating operation. A bias voltage of 3V was applied to the anode. The reset is also achieved as shown in Fig. 4(b). Optical energies obtained for the input, gate and reset are 8.0 pJ, 0.5 pJ and 10 pJ, respectively. Reduction in these values will be achieved by a decrease in device size.

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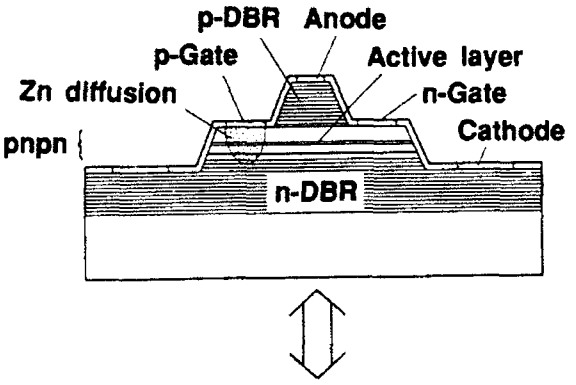


Fig.1 a schematic drawing of the fabricated four-terminal pnpn structure

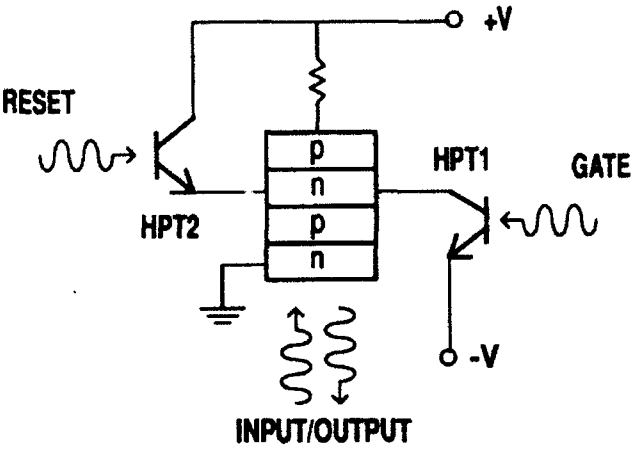
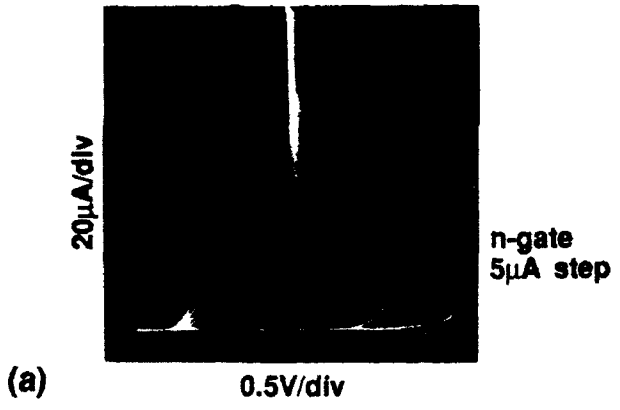


Fig.2 A schematic drawing of an equivalent circuit of the pixel. The three elements have the same four-terminal structure, two of which are used as HPTs by using an n-gate as a collector and a cathode as an emitter.



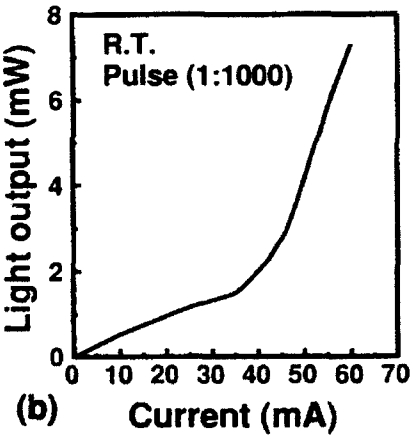


Fig.3 (a) Current-Voltage with various n-gate injections and
(b) Current-Light output characteristics of the four-terminal structure.

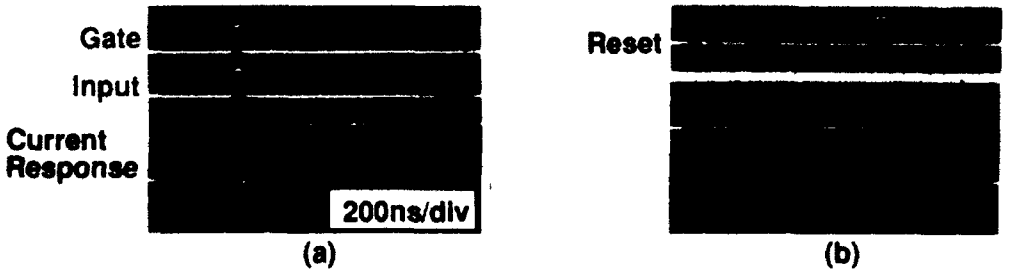


Fig.4 Operations of optically controlled pixel (a) optical gating (b) optical reset.

MD3 ALL-OPTICAL LOGIC GATES FOR USE AS SMART PIXELS

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Introduction

The goal of this work is to make use of the parallelism and interconnectibility of optical systems by creating large arrays of highly interconnected processing elements, called smart pixels, to implement high performance optical computing systems. The pixels make use of the decision-making abilities of electronics to process optical signals. Each pixel must contain at least one optical emitter and one detector, with more complex processing requiring more detectors and emitters. In addition to the requirements of optical inputs and outputs, the pixels must also accomplish some type of processing on the inputs. Specifically, boolean functions and memory are extremely desirable.

Two major obstacles for implementing optical computing systems are wavelength compatibility and optical signal restoration. In order for one optical logic gate to cascade with another, the output optical wavelength of the gate must lie within the sensitivity wavelength range of the input of the next gate. Additionally, to implement large systems of gates, the optical power output by the first gate must be greater than the power needed by the input of the next gate. A final consideration for implementing systems that will have practical size and power requirements is the ability of the pixels to be integrated onto semiconductor wafers.

The LAOS Solution

Our implementation of smart pixels makes use of a device made from a heterojunction bipolar phototransistor integrated vertically in series with a double heterostructure light emitting diode. We call this device the Light Amplifying Optical Switch (LAOS). The structures are grown in the InGaAsP/InP material system by gas-source molecular beam epitaxy. Due to this choice of material systems, the InP substrates are transparent to the operating wavelengths of the devices, facilitating the cascading of successive devices. The choice of materials in the LED active region also allows the output optical wavelength spectrum of the diode to overlap the input optical sensitivity widow of the phototransistors, thus meeting the first design criterion that the wavelengths be compatible.

The second criterion, optical signal restoration, is achieved by making use of the high optoelectronic gain of the phototransistor. The high phototransistor gain allows small optical inputs to cause significant increases in the current in the LED, creating optical output power levels that are greater than the input levels. Finally, by using existing semiconductor fabrication technology, large monolithic arrays of devices can be created.

We have discovered that it is possible to implement a complete boolean logic family from various configurations of the LAOS device and its components. Additionally, due to the inherent feedback present between the optical emitter and optical detector[1], the LAOS exhibits negative differential resistance in its I-V characteristics, which can be used to implement optical memory elements. Thus, using the LAOS, all necessary components for building optical computing systems are available.

Experimental Results

At the present time, we have demonstrated several of the many possible logic configurations available with the LAOS. The first demonstrated logic gate was the optical set-reset flip-flop/optical inverter, which was followed quickly, with the addition of another phototransistor, by a two input optical NOR gate[2]. Fig. 1. shows the circuit diagram and cross-section of a NOR gate (the inverter lacks one of the parallel phototransistors). Fig. 2. shows the optical input-output characteristics of a NOR gate with one input driven (equivalent to an inverter) as well as the optical timing diagram showing NOR operation. Fig. 3a. shows the load line diagram of the set-reset flip-flop, and Fig. 3b. shows the load line diagram of the inverter. Note that the difference in operation can be accomplished simply by changing the value of the dc bias voltage. Load line diagrams such as these will be used in the presentation to describe the operation of the various optical gates. In addition to NOR and inverter gates, NAND gates can be implemented simply by altering the metal interconnect lines to place the phototransistors in series. In fact, any of the possible logic gates can be implemented simply by changing the bias levels and metal interconnects, allowing many different types of smart pixels to be implemented on the same wafer.

Conclusion

We have demonstrated the feasibility of using the LAOS device to create several types of smart pixels that implement a variety of useful boolean and memory functions. These devices are cascadable and provide signal restoration. In the future, we hope to fabricate large arrays of smart pixels to be used in the implementation of an optical computing system.

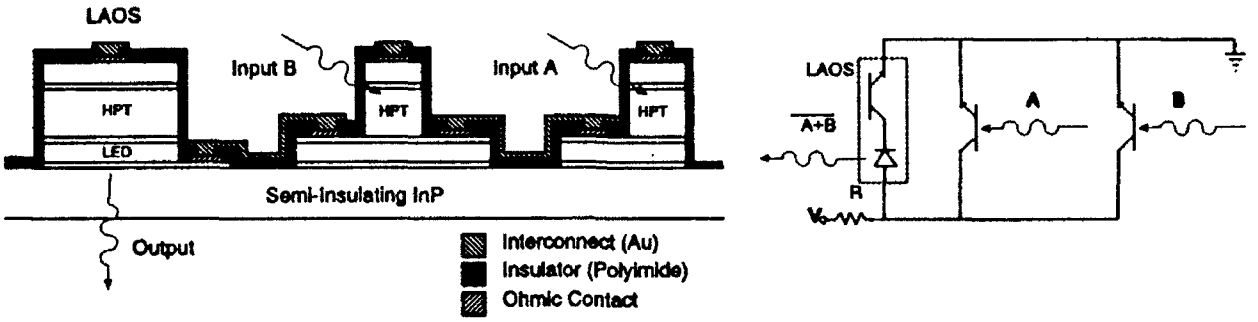


Fig.1. Layer Diagram and Equivalent Circuit of the optical NOR gate.

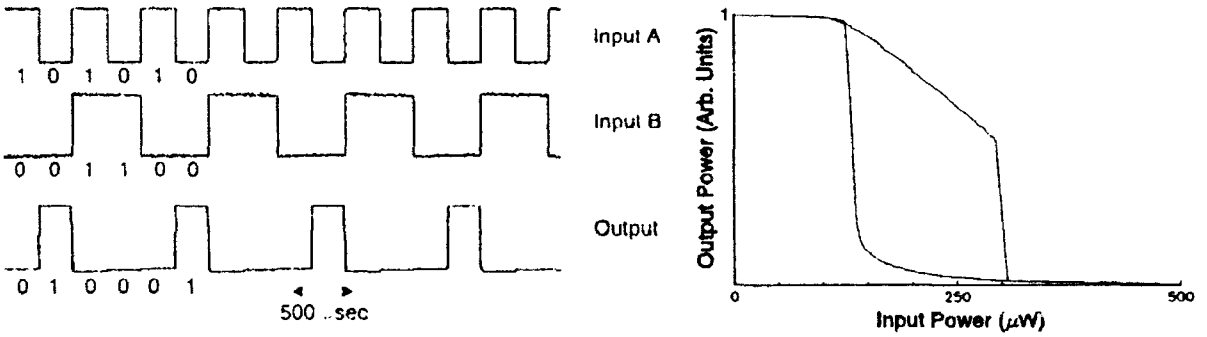


Fig. 2. Timing diagram of the NOR operation, and input-output characteristics of the NOR gate driven by one input (inverter operation).

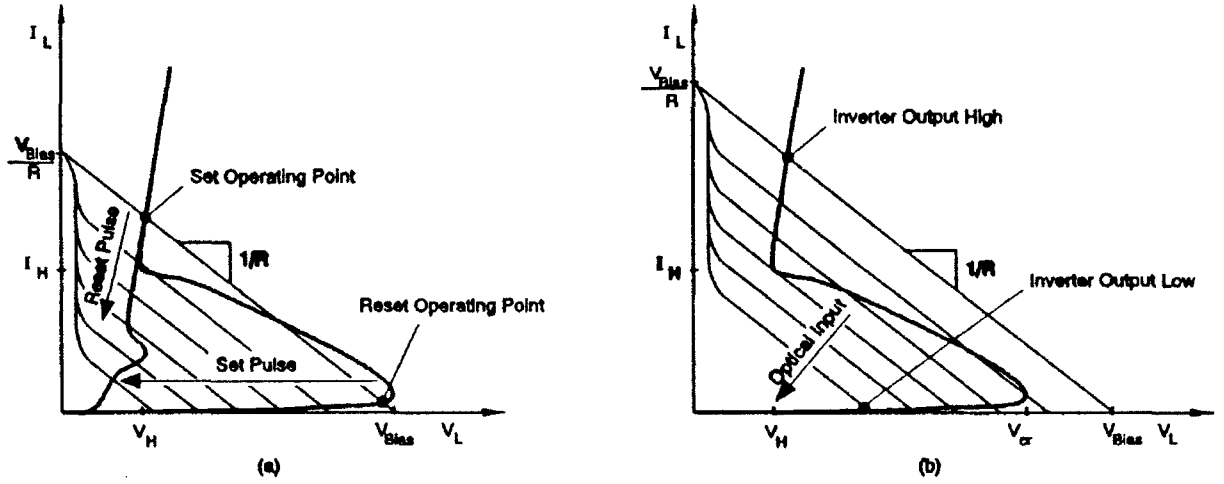


Fig. 3. (a) Load line diagram of the set-reset flip-flop. (b) Load line diagram of the inverter. Note that only the bias voltage has been changed.

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MD4 MONOLITHIC OPTICALLY BISTABLE CIRCUIT WITH TRANSISTOR GAIN USING NOVEL MODULATOR-HBT INTEGRATION TECHNOLOGY

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Very recently we demonstrated a simple, practical method of integrating heterojunction bipolar transistors (HBT's) and surface-normal modulator/detectors.[1] We inserted an electroabsorptive intrinsic region between the base and collector layers of a HBT. Then, a particular mesa may be either an HBT or a modulator, depending on whether either an emitter contact or an optical window is placed on the mesa, respectively. The base-collector contacts form the contacts for the modulator/detectors. For this technique to work we showed in Ref. 1 that the intrinsic region cannot be a multiple quantum well (MQW) with high barriers since this impedes current flow and seriously degrades the performance of the HBT. Bulk GaAs could be used for the intrinsic region but would have low modulation due to the weak exciton. Fortunately, we discovered that shallow GaAs-$Al_xGa_{1-x}As$ MQW's with $0.01 < x < 0.05$ possess strong excitons (and thus strong modulation) at room temperature,[2] and transport equivilant to bulk GaAs.[3] Therefore, we used this as the intrinsic layer. We named the process SESHL, for Single Epitaxy Supporting HBT and Low-barrier modulator. In Ref. 1 the substrate was etched to form a tranmission modulator. Here an integral mirror was grown so the more practical reflective modulator may be made (Fig. 1).

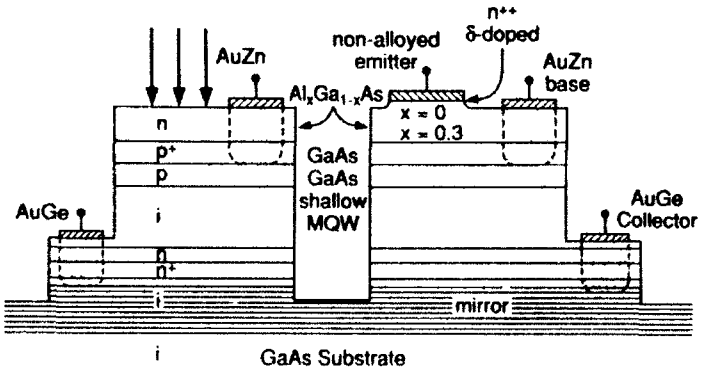


Fig. 1: Diagram of SESHL layer structure supporting both HBT and modulator.

Our work is the first integration of surface-normal modulator/detectors and HBT's. Previously, surface-normal modulators and *phototransistors* were integrated (i.e., no base contact made).[4] It is straightforward to show that a phototransistor does little to reduce optical switching energy compared to a simple detector. A phototransistor is modeled as a transistor with a detector across the base-collector junction. The current to charge this junction comes solely from the photocurrent. This junction must sustain a voltage swing necessary to charge the load (because the base-emitter voltage remains nearly constant). Also, the size of the phototransistor is governed by the spot size and so is as large as a simple detector. Therefore the switching energy (capacitance×voltage) has not decreased. If however, a separate detector is placed across the base-emitter terminals, its charging voltage to switch the output decreases dramatically (to about 0.2 V in our case), greatly decreasing the optical switching energy.

We present here large-area devices with wire-bonds placed on the surface to interconnect them. We are in the process of fabricating small-area devices with deposited metal interconnects. Our HBT's have good characteristics with a current gain of about 13 (Fig. 2). Our modulators also have good characteristics with a reflectivity change from 18 % to 46 % for 0-6 volt swing (Fig. 3).

The circuit we fabricated is the simplest posssible with the input detectors across the base-emitter terminals (Fig. 4). Two detectors in series are necessary across the junction in order to forward-bias it. This naturally forms a two-input logic gate. A

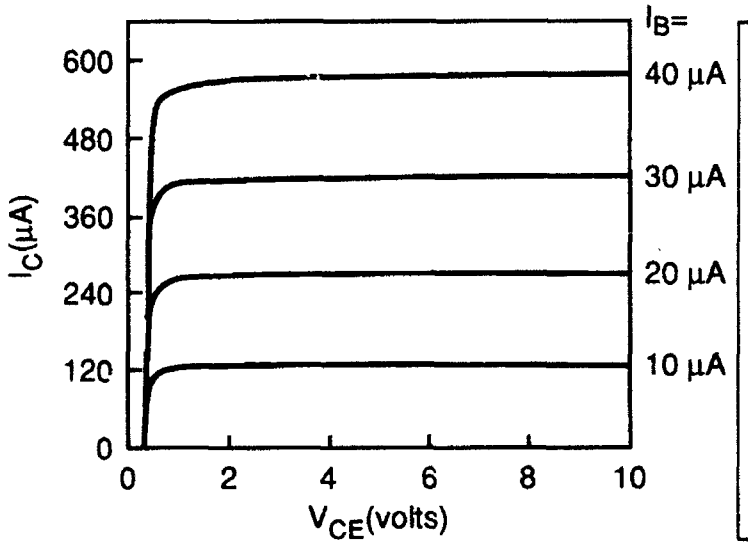


Fig. 2: CE characteristics of our HBT, showing gain of about 13.

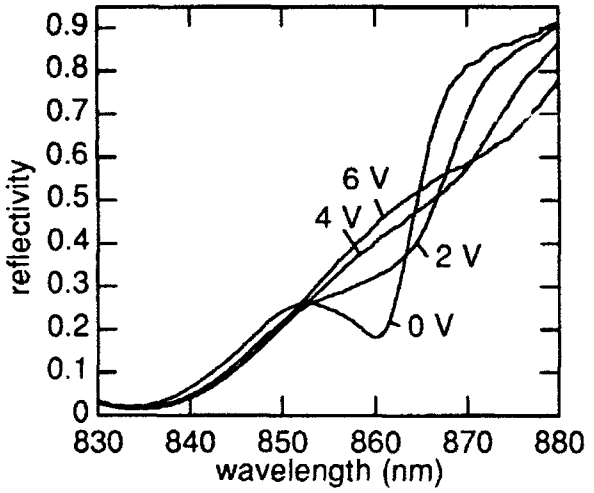


Fig. 3: Reflection spectra of our modulator, showing contrast ratio of 2.5.

reverse-biased modulator is placed in series with the collector-emitter port. By illuminating the modulator at the exciton wavelength, it has a negative photoconductivity with reverse bias, and therefore the circuit will have two stable operating points, just as in self-electro-optic effect devices (SEED's).[5] By raising the optical power on the input detectors, the collector current raises, and the circuit will switch between these operating points. This is shown in Fig. 4, where the optical power

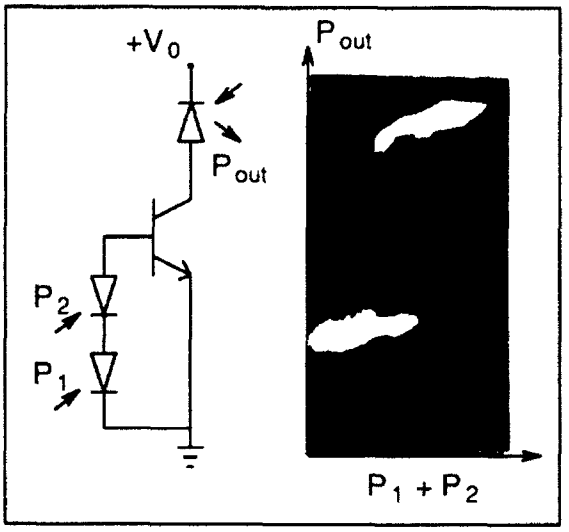


Fig. 4: Transfer characteristics of circuit shown, showing optical signal gain and bistability. Here V_0=7 V.

reflected off the modulator is plotted as a function of the input power. Clear bistability is observed, with an output contrast of 2.5. The optical signal gain is given by the ratio of the height/width of the loop and is about 4.

In conclusion, we have presented a monolithic optically bistable circuit with lowered switching energy due to transistor gain.

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MD5 # MICROLASER SMART PIXELS

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We describe the integration of vertical-cavity surface-emitting lasers (VCSELs) with field-effect (FET) and heterojunction bipolar transistors (HBT), photoreceivers, and micro-optics to form "*Microlaser Smart Pixels.*" [1] These optoelectronic integrated circuit (OEIC) "building blocks" will enable the realization of: optical interconnects/computing, optical memory, laser printing/scanning, visual projection displays, optical communications, and neural network systems. More specifically we describe our efforts to develop: monolithically integrated phototransistor/VCSELs, low-voltage-threshold VCSELs, visible-light (~650 nm) emitting VCSELs, 1D and 2D arrays of optically and electrically addressable *microlaser smart pixels* and system concepts based on *microlaser smart pixels* for optical multiplexing or optical interconnects.

We present our general concept for a *microlaser smart pixel* in Fig. 1a and a corresponding OEIC in Fig. 1b. In Fig. 1a *microlaser smart pixels* are illustrated as black boxes consisting of electrically or optically sensitive input components whose outputs are sufficient to drive VCSELs (phototransmitters). We are developing bipolar and field-effect transistors for the input components and VCSELs for the output components [2,3].

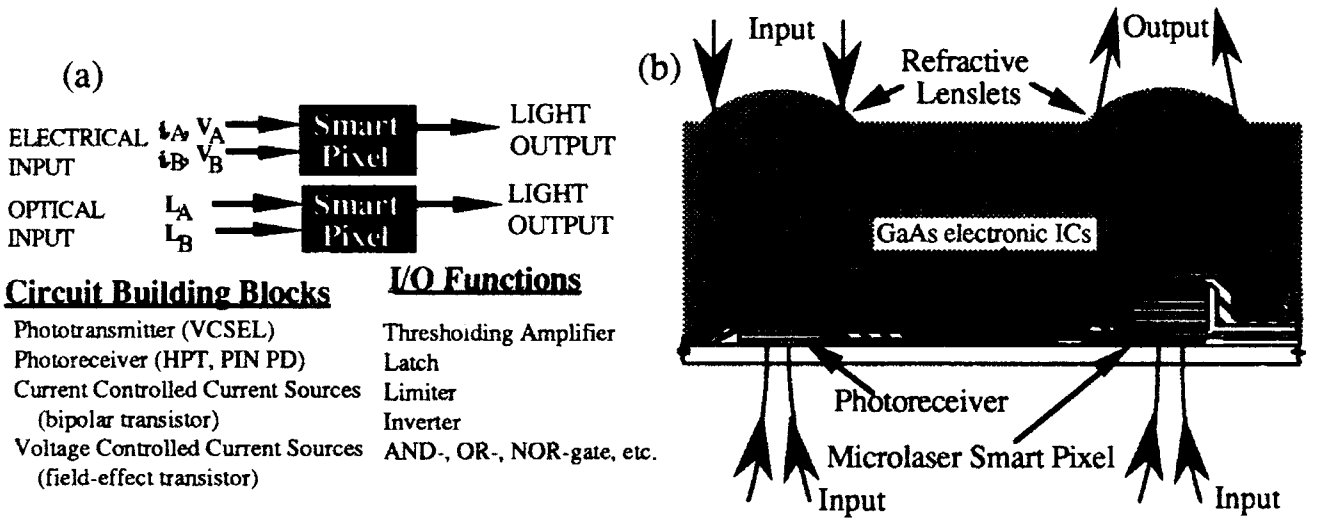


Figure 1. (a) Microlaser smart pixels: electrical/optical-input electrical/optical-output switching devices and the "building blocks" upon which they are based as well as examples of I/O functions. (b) Side view of a simple OEIC based on *microlaser smart pixels*. The OEIC consists of phototransmitters (*microlaser smart pixels*), electronic ICs, photoreceivers and diffractive micro-optic lenslets.

Microlaser smart pixels consist of bipolar and field-effect transistors integrated to VCSELs. For example, one embodiment of a cascadable *microlaser smart pixel* consists of a heterojunction phototransistor (HPT) monolithically integrated to a VCSEL to form an optical amplifier. In a first generation generation monolithic cascadable device we have demonstrated optical AND-gate operation. The gain of this device was low (near unity). Next generation devices promise to have much higher gain. For example, in a discrete cascadable HPT/VCSEL combination we achieved differential gain over 200, overall gain of 20, contrast of 34 dB and optical switching insensitive to input wavelength variations over 100 nm [4]. In addition, we are developing *microlaser smart pixels* consisting of HBTs and FETs integrated to VCSELs that promise current and voltage controlled operation in the10s of μAs and few Volt ranges, respectively.

Low-Voltage-Threshold VCSELs will greatly improve the performance of *microlaser smart pixels.* Previously, VCSELs had high series resistance and thus high-voltage operation resulting in poor heat dissipation and low packing densities. We have reduced the voltage threshold to 1.7 V, the lowest reported [5]. Low resistance was achieved by avoiding current injection through the top p-type mirror. This result will lead to higher efficiencies, higher powers, greater speeds, manageable heat dissipation, and much higher packing densities, thus making VCSELs practical for systems applications. The reduced thickness of the epitaxially grown portion of the low-voltage threshold VCSELs combined with shallower processing depths will also help enable transistor integration.

Visible Light-Emitting VCSELs (vis-VCSEL operating at 657nm) based on InGaP/InAlGaP strained quantum-well laser active region have recently been demonstrated [6]. Visible-emitting laser diodes have applications to optical memory, local area fiber-optic networks and laser projection displays. Integration of drivers, multiplexers, etc., to form visible-light emitting *microlaser smart pixels* will expand the range of accessible applications. The miniature properties of diode lasers combined with our ability to produce them in electrically addressable arrays makes them very attractive for visual projection displays. In addition, below we discuss the application of visible-light emitting *microlaser smart pixels* to optical multiplexing.

Systems Applications: The availability of low-power consumption, wide bandwidth optical interconnects that can be driven by transistors, forces us to rethink the comparison of Si and GaAs integrated circuit technology. Using *microlaser smart pixels* we envision a 3D hybrid electrical/optical computer consisting of electronic integrated circuits and *microlaser smart pixels* as optoelectronic interconnects. The functional parts of such a system consist of multilayer/multichip modules containing several integrated optical data/control bus communications components. In Fig. 2a we present a simple illustration of a 3D interconnect architecture. In addition, we will also discuss all-optical processors for digital optical computing and neural optical networks based on *microlaser smart pixels*.

Multi-wavelength arrays [7] hold the potential for achieving ultra-high-bandwidth optical fiber communication using wavelength-division multiplexing (WDM). A WDM system based on volume holography and optical fibers has been developed [8] and is suitable for multiplexing and demultiplexing multi-wavelength optical outputs from VCSEL arrays. Furthermore compact and ultra-fast holographic memory using an array of visible-light emitting *microlaser smart pixels* may also be realized. Commercial versions of these systems are realizable based on electrically addressable arrays of vis-VCSELs. In Fig. 2b we illustrate optical multiplexing using vis-VCSEL arrays.

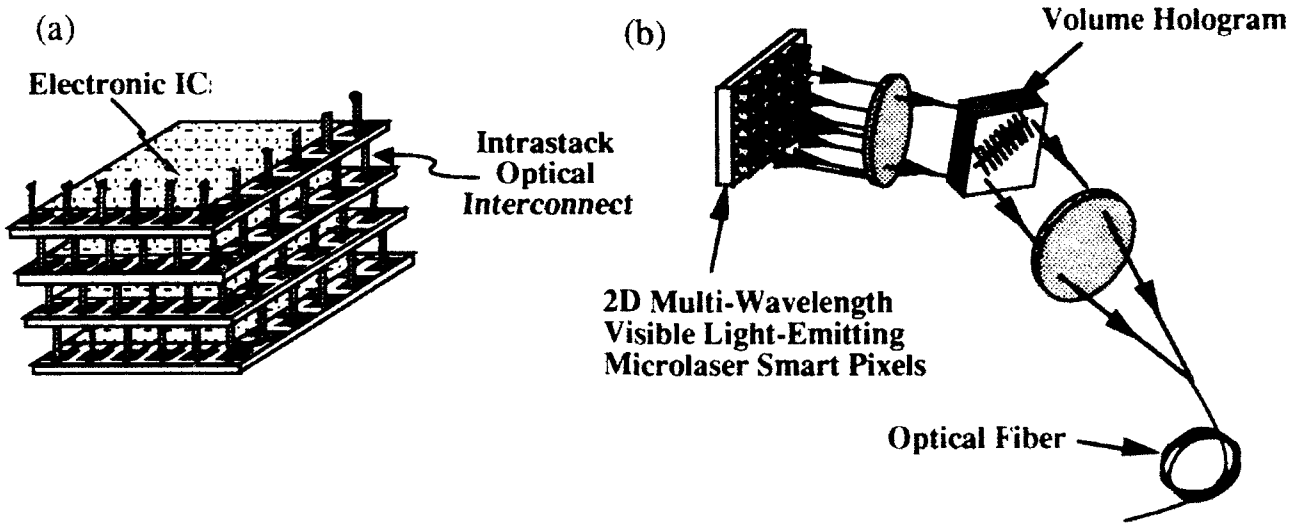


Figure 2. (a) Ultra high-speed 3-D hybrid optoelectronic parallel processor based on digital electronic logic and surface-normal OEIC interconnects based on *microlaser smart pixels*. (b) Optical multiplexing using arrays of visible-light emitting microlaser smart pixels having separated output wavelengths.

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TuA: Interconnects and VCSELs

TuB: Optical Switching and Processing

TuC: QW Smart Pixels

TuD: Optics and Optomechanics

TuA1 MONOLITHIC AND HYBRID INTEGRATION APPROACHES TO FREE SPACE OPTICAL INTERCONNECTS

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Abstract
Parallel beam free space optical interconnect depends critically on the interface from electronic signals to optical beams and vice versa. Integration may help to make these interfaces reliable and cheap. Three quite different approaches to this integration with different merits are discussed.

Introduction
Free space optical interconnect with many parallel channels is a promising technology for electronic systems with demanding interconnect requirements. It offers a way to interconnect two adjacent circuit planes without use of a backplane or connectors and allows to address the whole area of VLSI circuits rather than just the periphery. The implementation of free space optical interconnect faces many technological choices, both related to type of devices and to integration or assembly approach. At the transmitter side one can make a choice between LED's, laser diodes and modulators. Each of these have their specific advantages and disadvantages. The actual implementation implies that one has to integrate or assemble VLSI chips with optoelectronic device chips and passive optical elements like lenses or beam splitters (fig.1). This leads to uncommon packaging or integration approaches.
The most straightforward approach is to use a flip-chip solder bond approach to assemble the electronic, optoelectronic and optical layer. Such an approach is described elsewhere in these proceedings [1]. An alternative strategy is to integrate some of the functions in a monolithic or quasi-monolithic way. This offers the benefit of wafer-scale production and in certain cases enhanced performance. One can envisage the integration of the electronic and optoelectronic functions or alternatively of the optoelectronic and optical functions (fig.1).
In this paper we describe three integration approaches. The first is the monolithic integration of optoelectronic devices with Silicon circuits by heteroepitaxial growth of III-V on Silicon. The second is the quasi-monolithic technique of epitaxial lift-off (ELO) that can give an almost identical result as the heteroepitaxial technique. Finally the monolithic integration of optoelectronic devices with diffractive lenses will be discussed. Each of these approaches has specific assets for optical interconnect.

Monolithic integration by heteroepitaxial III-V growth on Silicon
The integration of III-V devices with Silicon VLSI circuits has been an attractive goal for many years now. Most research has focussed on the difficult problem of growing high quality III-V layers on Silicon. While enormous progress has been reported over the years [2], it seems that at least two problems remain. The first is that the dislocation density is still relatively high. This implies that the performance esp. lifetime of optoelectronic devices based on recombination is rather limited. The second is that the integration of these devices with Silicon VLSI gives rise to important practical problems, such as the fact that standard Silicon processing cannot be used, because the substrate preparation and growth of the III-V layers involves high temperature steps.
There have been different approaches to solve this problem. One is to try to get rid of the high temperature steps altogether. This implies that the Silicon circuits can be completed (incl. metallisation) in a standard way and that the III-V growth and device processing proceed afterwards. This is very attractive because it decouples the processing of both device types. Recently CNM (Madrid) has done impressive work to come near this goal. They demonstrated that high quality III-V layers can be obtained with a low temperature HF cleaning step and growth by Atomic Layer MBE at temperature below 300C on misoriented Si wafers [3]. With this technique they integrated AlGaAs/GaAs PIN diodes with CMOS (fig.2) and demonstrated acceptable forward and reverse PIN diode characteristics as well as the survival of the CMOS [4]. In spite of these rather spectacular results, progress in this area cannot be expected to be very fast because the ALMBE technique is not widely available.

Epitaxial Lift-off techniques
Given the problems associated with heteroepitaxial growth as described above there has been quite some interest over the last few years in epitaxial lift-off (ELO). In this technique (fig.3) the epitaxial layers for a device are removed from their underlying substrate (either by substrate etch or by undercutting an intermediate layer) and placed on a new host substrate that contains other devices. It has the character of a monolithic approach if one looks at the final result, but still makes use of a hybrid-like (and very delicate) pick-and-place technique. An obvious worry relating to this is reliability but promising results are being achieved [5].
The ELO-principle has been applied to quite a variety of device and material combinations (for a review see [6]). More in particular it has been used to transplant LEDs, laser diodes, MQW vertical modulators and photodiodes. In most of these devices the bond between ELO device and host substrate needs to provide low electrical resistance on top of good mechanical adhesion. An interesting approach to this problem is to use a Pd layer [7] that forms a

metallurgical bond at low temperatures. For applications in optical interconnect one would need to have a number of optoelectronic devices transplanted to the VLSI-chip. Depending on the density and placement topology one can think of having one area of the VLSI-chip covered with an ELO-"chip" or alternatively of covering most of the VLSI-chip with an ELO layer and afterwards etch through it to obtain a final IC with a number of ELO device islands.

Integration of diffractive lenses

Free space optical interconnect generally requires collimating and focussing lenses. If the interconnect distance is small and/or the number of channels large, one has to use micro-lens arrays on planar substrates[8]. These lens-"chips" have to be mounted with high transverse and axial precision on to the optoelectronic device chips. One option is to use solder bump technology. It is more attractive however to integrate the lenses with the optoelectronic devices. This can be done by defining lenses on the rear side of the optoelectronic device substrate, with the light going through the substrate (which can be done with either InGaAsP devices on InP or with InGaAs strained layer quantum well devices on GaAs). This integration ensures accurate alignment at a wafer scale level. Unfortunately such an approach is not readily applicable to optoelectronic devices that are integrated with Si-VLSI. Although implementations with refractive lenses have been reported it is very attractive to make use of diffractive lenses due to their planarity. The only problem is that their fabrication requires high resolution lithography, at least for wide apertures. The integration of Fresnel microlenses with surface-emitting lasers has been reported[9]. The integration of such lenses with LEDs (fig.4) is being studied theoretically [10]. It requires the use of rigorous diffraction models. It was shown that wide aperture Fresnel lenses can result in a strongly improved power transfer efficiency in comparison to LEDs combined with hybridly mounted micro-lens arrays.

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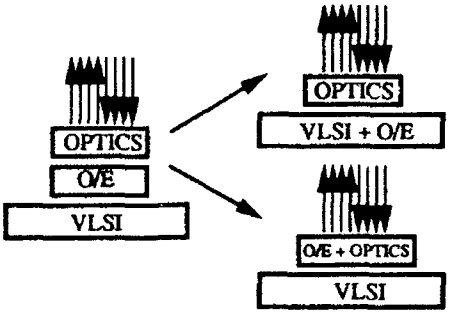


Fig. 1 Integration approaches for free space opt. interconnect

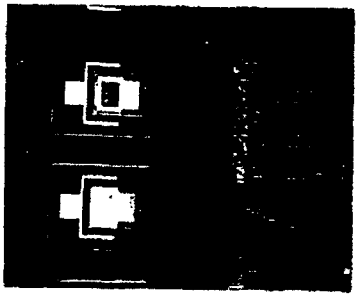


Fig. 2 Integrated III-V PIN diode with Silicon CMOS

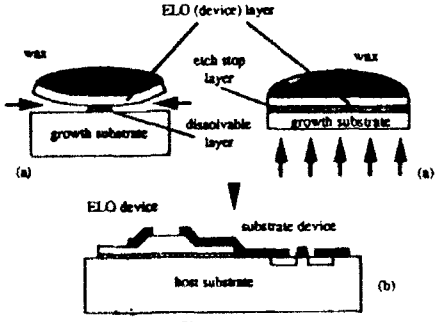


Fig. 3 Two approaches to Epitaxial Lift-off

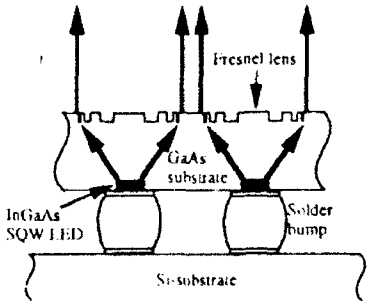


Fig. 4 Schematic drawing of LED with integrated lens

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TuA2 VCSE LASER TRANSMITTERS FOR PARALLEL DATA LINKS

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Integration of inter and intra-element logic into arrays of light emitters, detectors or modulators to form "smart pixels" has been stimulated by applications which include optical interconnection, switching and optical signal processing. Achieving this combination of logic and optoelectronic functionality in a way which is scalable to one or two-dimensional arrays is being approached in a variety of ways. One approach that in the near-term allows for sophisticated inter- or intra-pixel logic and control functions involves combining Si CMOS or bipolar technology with light emitter, modulator, or detector elements. This approach also leads naturally to incorporating smart-pixel based processors into a larger, Si-based system.

In this paper we focus on the major issues associated with utilizing vertical cavity surface emitting laser (VCSEL) arrays in conjunction with Si CMOS as the transmitter array in a DC coupled parallel data link. An assumption is made that only limited optimization of the individual links is permitted, and to the extent that the required circuits are shared by many channels. This is motivated by the observation that large parallel systems will have extremely limited utility if individual optimization is required.

The principle system performance metrics used in this work are bit error ratio and sensitivity to the tolerances of laser characteristics. The measured tolerances for ≈1000 lasers on a 0.5cm×0.5cm array were 20% for threshold current, 10% forward voltage and 23% differential quantum efficiency. We performed a detailed analysis of bit error ratio and show that the nominal SNR must exceed 14 at a 10^{-15} BER, corresponding to a 5dB power penalty, to "absorb" reasonable device tolerances. The tolerance of differential efficiency is most critical. This analysis suggests there is a trade-off between receiver complexity and laser tolerances, which is obviously a function of improvements in uniformity across VCSEL arrays.

Electrical crosstalk and thermal coupling issues become significant as the number of transmitters operated simultaneously increases. Block coding of data prior to optical transmission, in which *m* processor inputs are mapped into *n* driver inputs, has been investigated as a way of using abundant lasers to alleviate crosstalk-induced noise. To this end, Fig. 1(a) shows the eye diagram for current through a dummy load in a four-element transmitter array with four channels of uncoded random data. Fig. 1(b) shows the same channel after the random data is coded using a 4B5B mapping (4 data in, 5 lasers) which requires 11 gates to implement. The level of improvement is significant. Three other possible coding schemes are also described along with the tradeoffs in complexity and power dissipation. The results for the four schemes are summarized in Table 1.

Experimental work towards realization of a VCSEL-CMOS transmitter utilizing an 8×8 CMOS driver array is in progress. The CMOS driver array incorporates various levels of functionality across the array, ranging from laser driver circuits (Fig. 2 for example), to 4B5B coding circuits and latches, word generators and bandgap reference circuits. Internal word generators and control logic were provided for half of the drivers on the 8×8 CMOS chip to facilitate simple *in – situ* testing. Fig. 3 shows four CMOS drivers and the shared logic circuits for *in – situ* testing. Fig. 4 illustrates results utilizing an eight element CMOS driver which was wire-bonded to 8 elements of an 8×8 VCSEL laser array. This shows the (optical) waveform and eye diagram for a channel of this transmitter array operating at 622Mb/s, for which the BER was $< 10^{-9}$. Further work involves flip-chip bonding of VCSEL arrays directly onto CMOS logic circuits, as illustrated in Fig. 5.

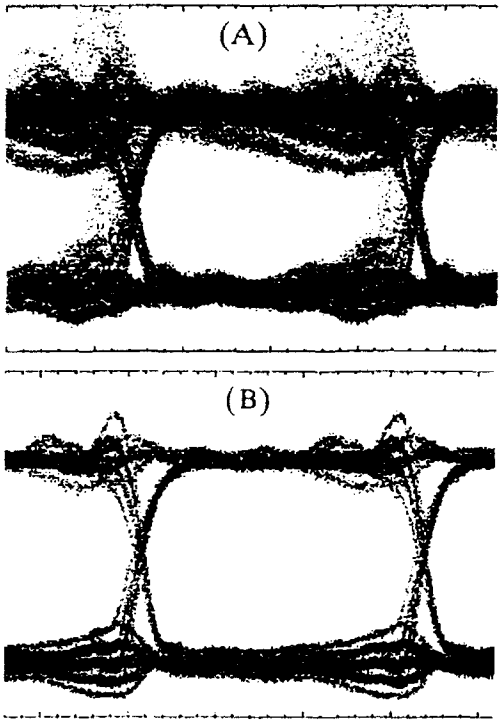


Figure 1. (a) Switching noise with random data and (b) noise following 4B5B coding

Coding	P_{AVE}	RMS noise	complexity
none	2	1.415	0
4B8B4	4	0	4
4B6B3	3	0	18
4B6B2	1.938	0.349	20
4B5BL	1.563	0.861	11
4B16B1	1	−0−	28

Table 1. Comparison of various mappings (*m* Bits data in, *n* Bits out/lasers, *l* lasers "on")

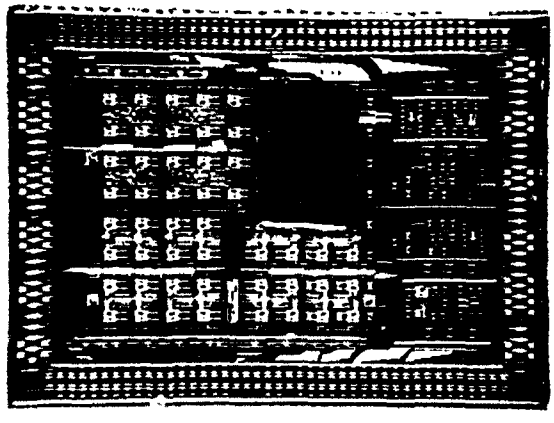


Figure 5. VCSE laser array on 8×8 CMOS interface chip.

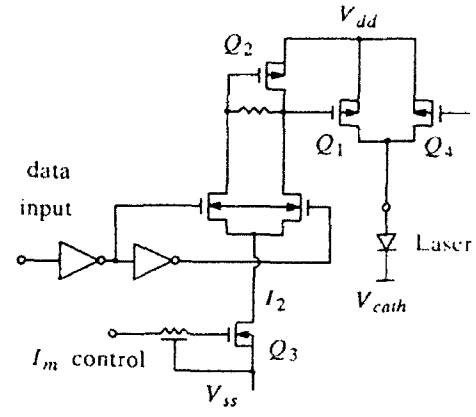


Figure 2. One of several new CMOS laser driver circuits.

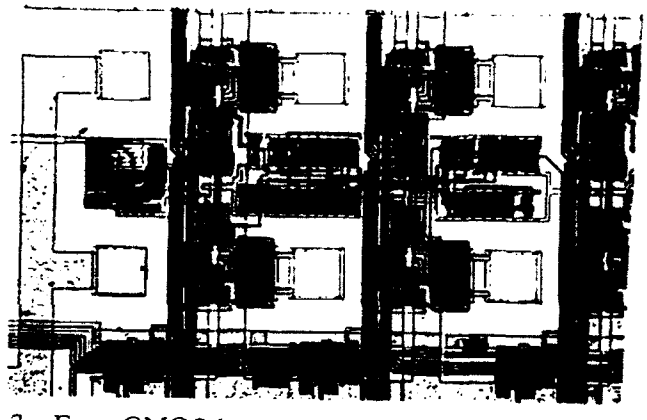


Figure 3. Four CMOS laser drivers with shared test circuits.

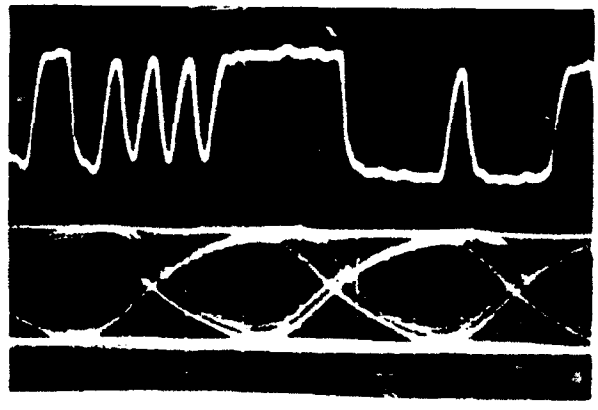


Figure 4. VCSEL-CMOS transmitter output at 622Mb/s.

TuA3 PERFORMANCE OF VERTICAL-CAVITY SURFACE-EMITTING LASERS AS SOURCES FOR SMART PIXELS

by

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Ideally, smart pixels would combine the advantages offered by both optical and electrical systems. An optical interconnection has the potential for large fanout at high speed. Practical design of the optical system, however, is complex. Questions of maximum fanout, beam steering, and array configuration are very dependent on source characteristics. Furthermore, the complexity and power requirements of the driver circuit is also an important consideration for these high density arrays.

Vertical-Cavity Surface-Emitting Lasers (VCSEL) have attracted attention as sources for these applications. Due to their cavity geometry, the output is a single mode, low divergence beam. Their small size leads to low threshold current and facilitates making high density arrays. However, their small size also leads to inherently high thermal resistance. Thermal effects limit the output power, cause shifts in wavelength and threshold current, and limit the array density due to thermal crosstalk. We have fabricated some of the most efficient devices to date [1,2], and have simulated the device characteristics including thermal effects with a finite element model. Using the verified model, more efficient designs have been studied.

Three major device structures have been modelled. All use three 80Å strained layer quantum wells as the active region cladded by semiconductor mirror stacks. In all three cases, the cavity mode has been designed to be on the long wavelength side of the gain peak. As the junction heats up the gain curve shifts into resonance with the cavity mode, resulting in a temperature insensitive threshold current. A comparison of the three devices under CW operation is shown in the figures below. In Fig. 1 the optical output power is plotted as a function of the input electrical power. Power efficiencies range from ~6% for device (*A*) to ~20% for device (*B*). Also shown is the approximate increase in wavelength. In Fig. 2 the threshold current is plotted as a function of junction temperature. In both plots, curve (*A*) matches the measured device while curves (*B*) and (*C*) are predicted performance.

The first device, (*A*), is a vertically contacted bottom emission VCSEL [1]. The current

injection is through the mirror stacks. This causes relatively high drive voltages and power inefficiencies. Eventually, carrier confinement in the active region becomes poor, and the threshold current rises dramatically. The second device, (*B*), uses intra-cavity contacts to bypass the mirror stacks, reducing Joule heating and improving power efficiency. The carrier confinement has been improved by increasing the aluminum content of the layers cladding the active region, leading to a broader region of temperature insensitivity. The third device, (*C*), also uses intra-cavity contacts but has improved the overlap of the optical mode with the injected current. The resulting reduction in spatial hole burning improves power efficiency. The penalty of a larger optical mode is a slight increase in threshold current.

In summary, well designed VCSELs make efficient, low threshold and temperature insensitive sources for optical interconnection. With an understanding of present and future device performance, system designers can begin to make choices for the most practical architectures.

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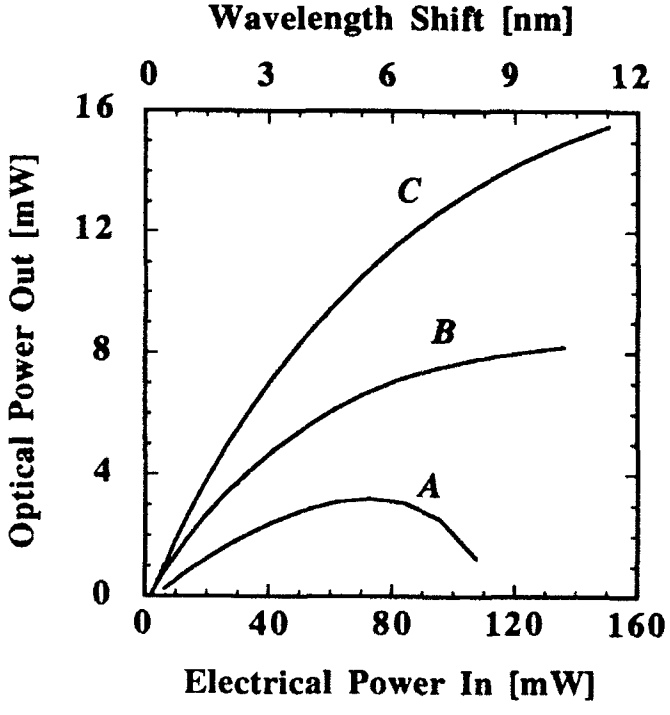


Figure 1

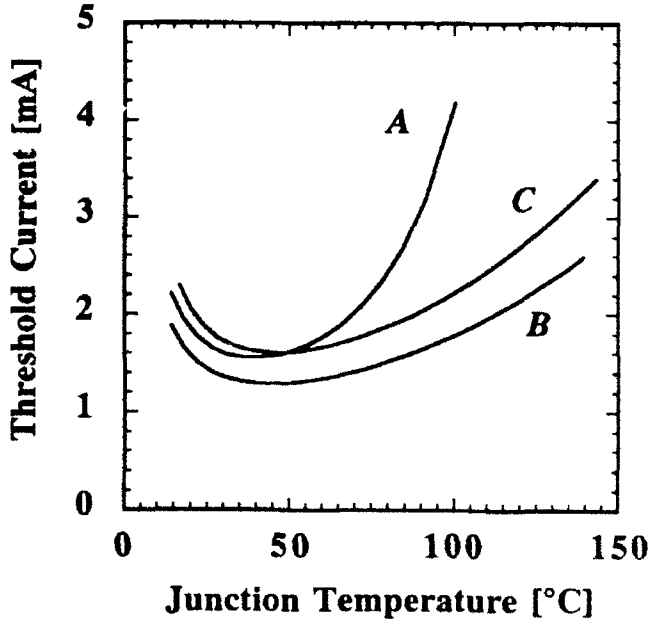


Figure 2

TuA4 THERMAL PROPERTIES OF PROTON-IMPLANTED TOP-SURFACE-EMITTING MICROLASERS IN LINEAR AND NONLINEAR REGIMES

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Vertical-cavity surface-emitting lasers (VCSELs) are key active components in smart-pixel technology. Optical switches, logic gates, and memory elements have been proposed and implemented using microlaser-type VCSELs monolithically integrated with other electronic and optoelectronic devices[1-3]. VCSEL-based compact two-dimensional switching arrays are very attractive for use in parallel optical information processing, optical computing and interconnection architectures. A major obstacle preventing development of such arrays today is the excessive thermal dissipation in electrically pumped VCSELs. However, in spite of their importance, very little attention has been given to thermal problems in microlaser-type VCSELs.

Microlaser VCSELs feature a quantum-well active region sandwiched between two distributed Bragg reflectors (DBRs). The active region is aligned to coincide with the antinode of the standing wave at the lasing wavelength. Planar proton-implanted GaAs/AlGaAs microlaser VCSELs emitting light through the top surface are very attractive for integration due to their relatively low series resistance[4] and wavelength compatibility (and associated cascadability) with GaAs-based phototransistors or photothyristors[3]. In this paper, we investigate thermal properties of these devices, with a special attention given to development and validation of a simplified approach that would not require an extensive numerical analysis.

The specific device structure under consideration is described in detail in Ref. 4. A multiple-quantum-well GRINSCH GaAs active region is defined by an annular contact on the top surface and by a highly resistive proton-implanted region funnelling the current towards the central section of the device. In order to reduce series resistance, all interfaces in DBR sections are linearly graded.

Thermal analysis of the top-surface-emitting VCSELs is performed using a self-consistent model that features realistic distribution of heat sources combined with two-dimensional treatment of heat-flux spreading. Self-consistent solution is found by numerical iteration, taking into account temperature-dependence of device parameters, including thermal conductivity, threshold current, electrical resistivities, *etc.* In the nonlinear regime, large temperature variations affect substantially lasing characteristics, eventually leading to positive feedback and thermal runaway.

In the linear regime, not too far above the threshold, thermal behavior of a top-surface-emitting laser is approximated by lumping all sources of heat generated in the device into a single source located at the active region. Below the active region, two-dimensional heat-flux spreading is considered. Upward heat flow (from the active region to the p-type mirror and then down to the substrate) is neglected. The nonuniform system of the n-type mirror and the substrate is replaced with an equivalent medium of an effective thickness obtained by converting each layer into its thermal equivalent with the thermal conductivity of the substrate. Under these assumptions, thermal resistance of the structure can be approximated by a simple analytical formula. To test its validity, we compare in Figs. 1 and 2 the approximate result with the comprehensive numerical model.

Fig. 1 shows the current dependence of thermal resistance R_{th}, defined as the ratio of the average active-region temperature increase ΔT_a and the total power of all heat sources in the device. Relatively high value of R_{th} is primarily caused by the "junction up" configuration of the top-surface-emitting microlaser. Although R_{th} is often treated as a constant parameter, it is

clear that due to nonlinear processes it is a function of pumping current. Nevertheless, the approximate formula gives a very good estimate of R_{th} near the lasing threshold.

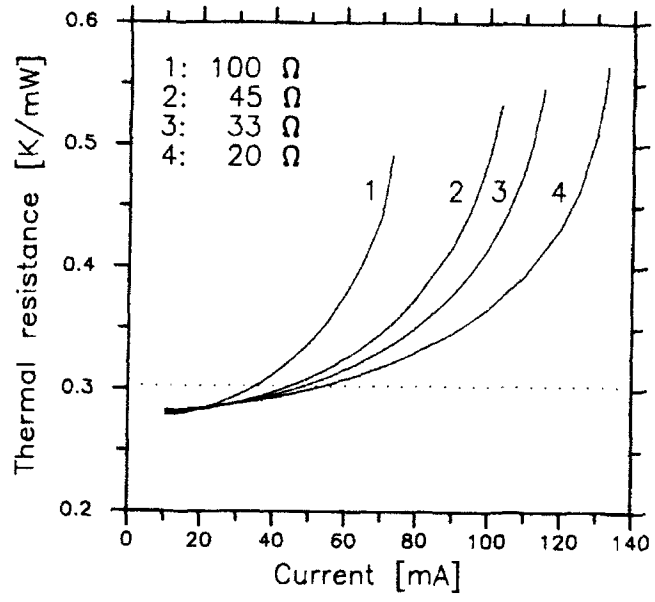


Fig. 1. Pumping-current dependence of thermal resistance of GaAs/AlGaAs top-surface-emitting laser with active-region diameter of 35 μm. Solid lines - nonlinear analysis. Dotted line - linear approximation. Curve 3 corresponds to the device of Ref. 4, with cw threshold current of 10.2 mA.

The range of validity of the simple linear treatment can be estimated by examining the calculated active-region temperature. As shown in Fig. 2, a remarkably good agreement between approximate results and the numerical model is obtained for low-series-resistance devices all the way up to 6 times the threshold current.

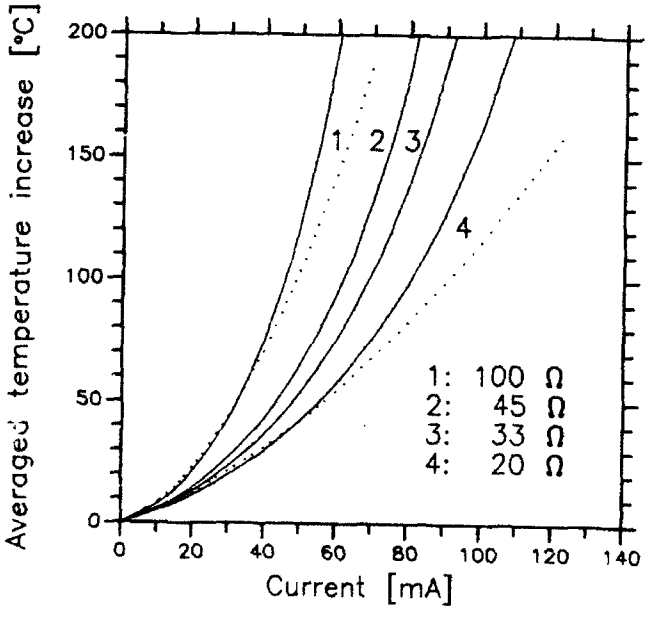


Fig. 2. Pumping-current dependence of averaged active-region temperature increase ΔT_a in a GaAs/AlGaAs top-surface-emitting laser with active-region diameter of 35 μm. Solid lines - nonlinear analysis. Dotted line - linear approximation.

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TuB1 APPLICATIONS OF 2-D SMART PIXELS TO PHOTONIC SWITCHING

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INTRODUCTION

There have been several recent studies on various types of free-space optical switches for photonic switching systems and optical interconnections. To make more sophisticated switches, 2-D-array devices with smarter pixels are needed. Here, we discuss the functions required of smart pixels in free-space optical switches.

CLASSIFICATION OF FREE-SPACE SWITCHES

Free-space optical switches can be classified as shown in Fig. 1. Analog switches are transparent for signal format, bit rate, and type of modulation, and so can handle high-speed optical signals over a wide range of wavelengths. Their drawback, however, is the loss and crosstalk accumulation when they adopt a multistage structure. Digital switches, on the other hand, can regenerate the level and/or timing of the signal. In this case, there would be no loss and crosstalk accumulation even with the multistage structure. The signal speed, however, is limited by the response time of the switching devices. The wavelength range is also limited when the device has MQW structures or cavities. Therefore, each type of free-space switch has its own range of applications according to these limitations.

SMART PIXELS FOR PHOTONIC SWITCHES

The role of smart pixels in photonic switches is to add some functions to optical switches in order to improve the performance of the switches or to simplify the external control circuits. A signal monitoring function, for example, is worthwhile even in analog switches, because monitoring is indispensable for system operation and maintenance. Signal regeneration is a basic function of digital switches and is valuable for making multistage switches. The 2x1 [1] and 2x2 switch elements are useful for reducing the complexity of the optics in free-space switches. The self-routing function is also attractive for photonic packet-switching systems.

To introduce smart pixels into free-space systems, several technical issues must be solved, such as what function, speed, and the number of pixels in an array are required. The function of a pixel is limited by the number of available electronic elements it contains. Its function should be determined by carefully considering the speed-function trade-off; complex electronic circuits limit pixel operating speed and reduce the performance of the system. To solve these issues, system designers need various information about the devices.

SMART PIXELS IN AN ANALOG SWITCH

An optical subscriber-line concentrator, an analog switch with a self-routing function, is an attractive application of smart pixels. It automatically picks out live lines from among all the input lines and connects those to the output lines, as shown in Fig. 2 [2]. A key component of this switch is a beamshifter (Fig. 3), an array of shift cells (smart pixels) that has the function of shifting an optical beam to a vacant cell. The shift function is accomplished using polarization switching based on twisted-nematic liquid-crystal and the birefringence of calcite. Other indispensable functions are signal-level monitoring for live-line detection, searching available paths, and liquid-crystal cell driving. These functions require that photodetectors, amplifiers and logic circuits (Fig. 4) be integrated on each cell. High-speed operation, however, is not needed for these circuits, because the connections are only changed at the origination and termination of calls. Modest speed elements such as thin film transistors (TFTs) and photodetectors on liquid-crystal switching cells can therefore be used.

As a step in the development of such an optical concentrator using beamshifters based on smart pixels, we have built an experimental 1024-input/256-output concentrator with external control circuits and a light-transmissible 1024 (32x32) a-Si PIN photodetector array module with switching TFTs for the readout and have confirmed their basic operation [3]-[5].

SMART PIXELS FOR DIGITAL SWITCHES

Recently, a 2-D photonic switch array, an exciton-absorptive reflection switch (EARS), consisting of vertically integrated MQW modulators and phototransistors has been developed for free-space optical switches and optical processing circuits. OR and NOR gates and memory operations have been demonstrated using the EARS [6]-[7]. In the future, more sophisticated functions necessary for the digital switches would be integrated onto each pixel.

CONCLUSION

Free-space photonic switching applications require that smart pixels perform various functions such as 2x2 switching, signal monitoring, signal regeneration, and self-routing. A cascaded-beamshifter-type optical switch has been presented as an example of such applications. Further investigations on the system architecture and device fabrication are necessary to determine the specifications of smart pixels for free-space optical switching systems.

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Switch type { Analog switch / Digital switch } Structure { Singlestage / Multistage }

Fig. 1 Classification of free-space switches

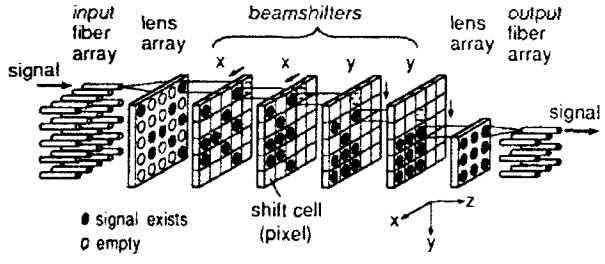


Fig. 2 Structure and principle of the two-dimensional concentrator

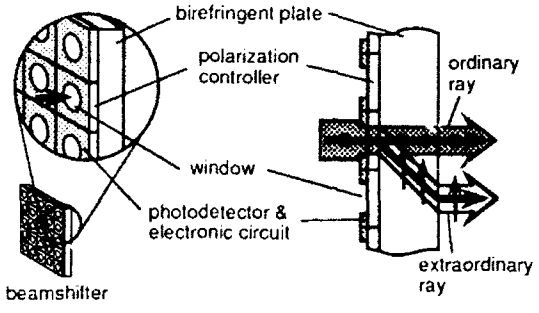


Fig. 3 Beamshifter structure

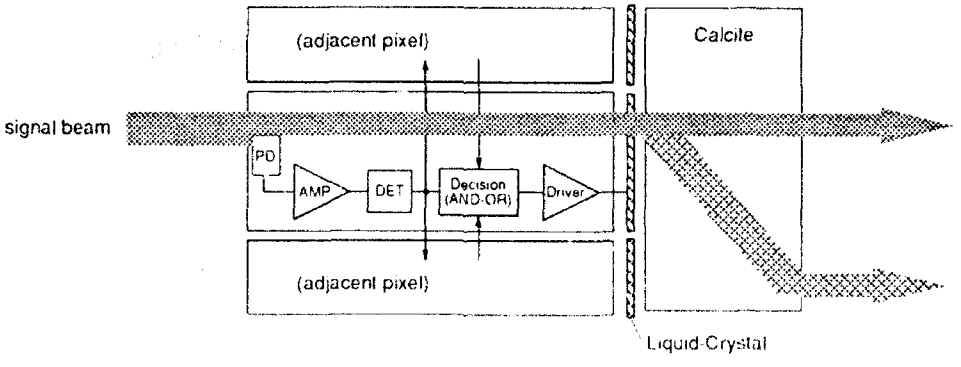


Fig. 4 Example of electronic circuits on pixels

TuB2 MONOLITHIC 2X2 BYPASS-EXCHANGE NODE FOR TWO-DIMENSIONAL OPTICAL INTERCONNECTION ARCHITECTURES

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We describe for the first time the experimental demonstration of a monolithic two-dimensional bypass-exchange node, which routes optical data to different destinations in accordance with a set of control voltages. This 2x2 switching node is the surface-normal analog of an optical directional coupler, which forms the basic building block for a new three-dimensional space-division multiplexing architecture. This switch possesses all the positive attributes of vertical cavity surface-emitting lasers (VCSEL)-based optical switches, including optical regeneration, high optical gain and contrast.

The bypass-exchange node consists of two closely-spaced input/output optical channels, each comprising a pair of HPTs (PNPNs) and a VCSEL. The PNPNs (HPTs) and VCSELs are interconnected as in Fig. (1). The switch can be used in either the latching, non-latching, or bistable format [1]. For real applications of the bypass-exchange node, either the non-latching HPT-mode or the bistable PNPN mode is preferred, since these permit the switching to be effected optically in response to the input data. However, because of the much lower switching optical power is required, we demonstrate the concept here using the latching PNPN mode.

To demonstrate the exchange and bypass operations, control voltages V_1 and V_2 are toggled back and forth between the values of 0V and 8V in Fig. (2), thus connecting the HPT/PNPN to one of the two VCSELs in either the straight-through or cross-over configuration. The optical input from an external modulated source is incident upon one input channel 1 (channel 2 is identical). As the controls toggle back and forth, the input pulses alternately switch on VCSEL 1 (bypass) or VCSEL 2 (exchange). The input data is regenerated alternately from one of the VCSEL outputs (850 nm), which is capable of triggering the next switching stage. The alternation of the output optical pulses between channels 1 and 2 is clearly seen in Fig. (2). The slow response of the output traces belies the high switching speed of the node, and is attributed to the slow response of the photodetection circuit. The actual switching speed is better represented in Fig. (3), which shows the temporal relationships between the input laser drive current pulse, the input laser output, and the response of the HPT/PNPN current. The input laser rise time is 8 ns, following a turn-on delay of 28 ns. Both the HPT and PNPN respond to the laser excitation with unobservable delay, with a deconvolved rise time of a few ns. The VCSEL can be modulated at a multi-Gb/s rate, and its turn-on delay is negligible. The true switching speed, which is presently limited by the parasitic capacitance and by an external series resistance, can be improved by packaging. The integration of multiple switching nodes on a common substrate should also be possible using a minimum of isolation layers .

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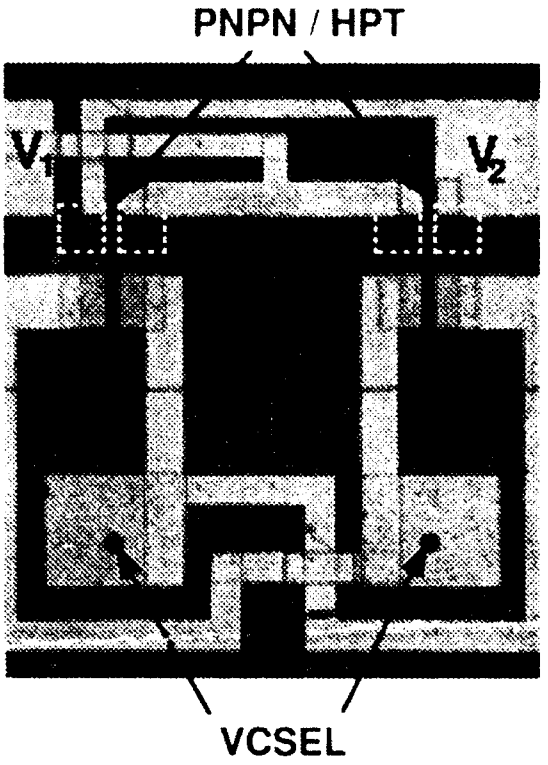


Fig. 1 Layout of 2x2 optical bypass-exchange switch.

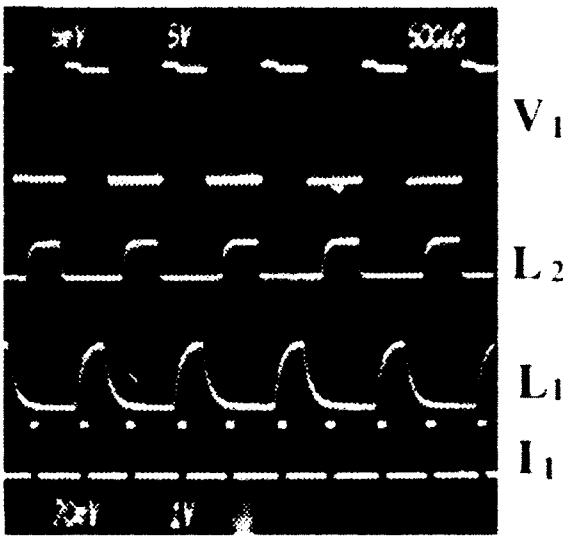
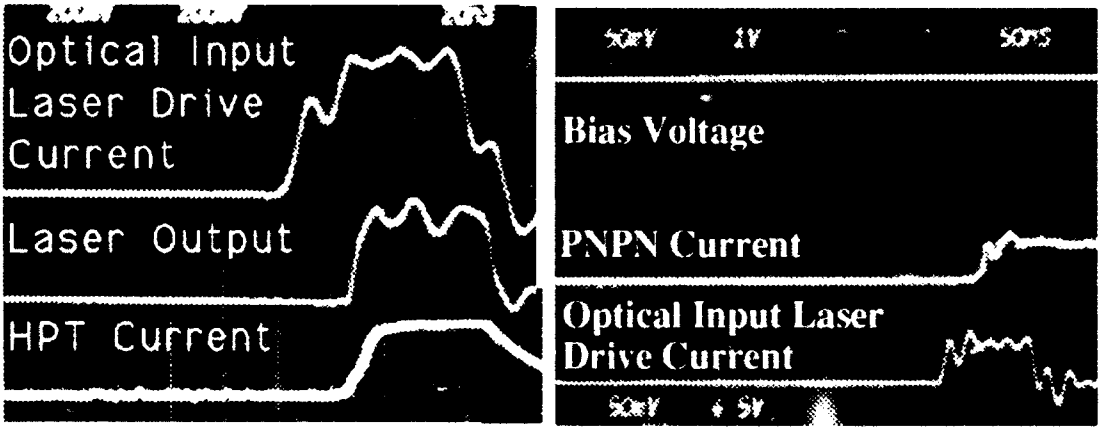


Fig. 2 Oscilloscope traces of optical 2x2 node operation. V_1 and V_2 are the route control voltages, L_1 and L_2 are the outputs. I_1 is the input on CH1. V_2 (not shown) is compliimentary to V_1.



(a) (b)

Fig. 3 Oscilloscope traces show the input laser drive current. laser output, and the (a) HPT, (b) PNPN currents.

TuB3 ADDED FUNCTIONALITY FOR SYMMETRIC-SEED SMART PIXEL OPTICAL INTERCONNECTS, OBTAINED VIA SIMPLE OPTICAL CONTROL TECHNIQUES

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SUMMARY OF PRESENTATION

Introduction

Recently, a great deal of attention has been focussed on how optics can be used to advantage in telecommunications and data processing architectures. The advantages of optics are well known. They include very high bandwidth and because of lights immunity to electromagnetic interference, many optical channels can be placed in close proximity to each other.

Electronic technology, with its very high degree of integration, is very efficient at processing information. However, as logic speeds increase and the propagation delays of electrical system interconnects become significant relative to a single clock cycle, Input/Output increasingly becomes a limitation in digital systems design. This I/O bottleneck can be alleviated by the use of high speed optical interconnections. Another way of increasing throughput of a system, rather than by higher bit rates, is by interconnections in parallel. This attention to parallelism has given rise to interest in two-dimensional arrays of optical devices interconnected by bulk optics. The optical elements of the 2-D array can be simply optical logic gates or even a combination of electronics and optical devices ('smart pixels') to take advantage of the relative merits of electronic and optical technologies. Because the electronics are close to the optical input, interconnection lengths are small and the speed of these smart pixels can be very fast [1]. Optics provides an efficient and fast pin in/out to the electronics which does the intelligent processing on the data. Functionality of the smart pixel is obtained from the high speed electronics. However, this presentation will demonstrate how simple optical control techniques can be applied, (in the case of S-SEED based interconnects), to give quite sophisticated additional functionality to the pixel aside from that gained from any electronic processing.

Theory

In the S-SEED, two multiple quantum well (MQW) PIN electroabsorption modulators are reverse biased in series [2]. The MQW PIN diodes are operated at a photon energy corresponding to the zero field e1-hh1 exciton peak and therefore upon increasing applied field, the exciton red-shifts reducing device absorption and photocurrent. This decreasing photocurrent for increasing voltage, ('negative resistance'), under certain conditions, gives rise to positive feedback and optical switching. The S-SEED is bistable in the ratio of its two input beam powers. By using asymmetric Fabry-Perot modulators the change in device reflection on switching and switching contrast can be made very high [3] (figure 1). For the S-SEED to change its state, the ratio of optical input powers has to be greater than the required input contrast ratio, $C = (A_{max}/A_{min})$, where A_{max} and A_{min} are the maximum and minimum device absorption coefficients.

As the inputs to the S-SEED vary from 01 to10 the S-SEED changes state and the entire bias voltage is seen entirely across the diode receiving the least optical signal power, with corresponding complementary changes in the devices reflectivities. Information can be passed to the electronic pixel logic by monitoring the S-SEED centre voltage V_{centre}. If however, a constant control optical bias signal is made incident on the S-SEED diodes, the control signal effectively degrades the input contrast ratio of the two input signals below that required for switching. The S-SEED now remains latched in its state prior to the application of the control bias signal (figure 2). One of the two inputs to the S-SEED is now reflected, the other suppressed, depending on which

state the S-SEED has latched. V_{centre} of the S-SEED remains fixed and therefore no information is passed on to the electronic pixel logic. Under zero illumination conditions, the S-SEED operates with the supply voltage equally distributed across the two diodes constituting the S-SEED. If equal intensity light beams are applied, the S-SEED operates in a metastable state where a small difference in input beam powers will be sufficient to cause latching in one direction or the other. If the two signal inputs and control bias are added simultaneously, after a period of inactivity, then any difference in input powers will cause the S-SEED to latch and remain latched. Latching therefore occurs on the first bit difference of the two input signals, whereas the same signal inputs, in the absence of the control bias, would cause the S-SEED to toggle as the input signals changed.

Experiment

The MQW device structure used was grown by MOVPE and is a normally-off, Bias-reflecting, asymmetric Fabry-Perot modulator [3] consisting of a 15 x (150Å GaAs well/60Å $Al_{0.3}Ga_{0.7}As$ barrier) intrinsic region sandwiched between p-type and n-type layers, with $(A_{max}/A_{min})\approx 1.8$. Two information beams were made incident on the S-SEED. The S-SEED was bistable in the ratio of these beams, changing states with the inputs 01 and 10 and remaining in its present state for the inputs 00 and 11. When the control bias beams were applied, the S-SEED remained latched and did not change its state regardless of the combination of signals at its input. Latching on the first bit difference of the signal beams + control beams was also observed.

Application

The functionality that can be obtained from S-SEEDs operating in this simple manner can be quite sophisticated. For example, consider two bit-synchronised binary optical signals serially forming an input to the S-SEED. If these numbers are in most significant bit (MSB) last format, and are followed by the optical strobe control signal, then the S-SEED remains latched in the state corresponding to the MSB difference of the two binary streams. Linking such a device into a smart pixel containing a routing high-contrast AFPM-PIN MQW device pair potentially leads to a smart pixel self-routeing element for use in a Batcher type sorting network.

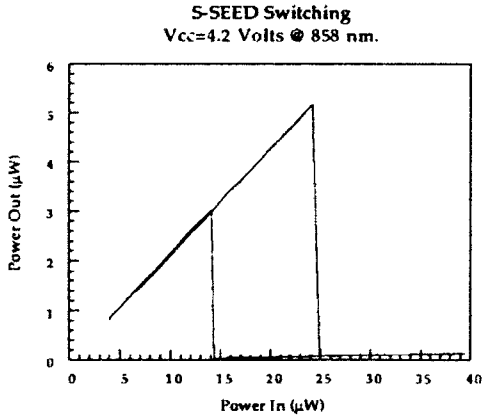


Figure 1

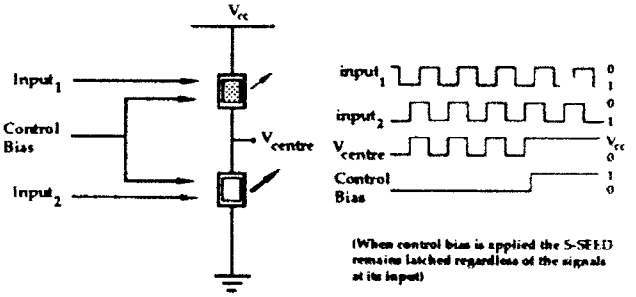


Figure 2

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TuB4

SEMI-INSULATING MULTIPLE QUANTUM WELL DEVICES FOR IMAGE PROCESSING APPLICATIONS

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Sensitive, fast optical nonlinear devices are an essential component of any optical information processing system. For optical image processing, a large degree of parallelism (~ 10^6 pixels) and moderate speeds (10^{-3}-10^{-6} sec) are desired. Currently, the most common optical nonlinear devices for these applications such as the liquid crystal light valve and bulk photorefractive materials suffer from lack of speed, sensitivity, or resolution. The large excitonic nonlinearities of multiple quantum wells along with the efficient carrier transport properties of these materials and the flexibility in design of the semiconductor structure allow fabrication of novel, sensitive, highly nonlinear devices.

Here we describe semi-insulating MQWs devices that we have developed for image processing applications. These devices are fabricated by placing the semi-insulating multiple quantum well (SI-MQW) between wide-gap semiconductors or dielectric layers and transparent electrodes. Application of an external voltage produces an electric field across the SI-MQW layer, which creates an absorption change due to the quantum confined Stark effect (QCSE). Illumination of the device can generate carriers that drift in the applied field, are trapped at the SI-MQW/ wide-gap material interface and screen the field. In this way variations in the incident intensity produce corresponding changes in absorption coefficient and refractive index through the QCSE. Absorption changes of $\Delta\alpha$~7000 cm^{-1} with less than 2 $\mu J/cm^2$ are obtained in these devices [1,2]. Furthermore, use of semi-insulating MQWs in these devices relieves the need for pixelation [3]. The absorption and refractive index of these semi-insulating MQW (SI-MQW) devices near the excitonic absorption peak is a function of the intensity of the incident light. The SI-MQW device can therefore be thought of as sensitive real-time image recording elements. Real time optical holograms can be written in this device through intersection of two laser beams in the sample. We have obtained diffraction efficiencies as high as 3% from the self-diffraction of the write-beams from the thin hologram (2 μm thick). Figure 1 shows the diffraction efficiency for a Cr-doped SI-MQW device consisting of 150 periods of 100 Å GaAs wells and 35 Å $Al_{0.28}Ga_{0.72}As$ barriers as a function of grating period and applied voltage. The high diffraction efficiencies obtained open up the possibility of use of these devices as real-time optical recording materials for applications such as image correlation [4]. We have developed a compact (30 X 30 X 10 cm) joint transform correlator system consisting of a Cr-doped GaAs/AlGaAs multiple quantum well device, two diode lasers, a liquid crystal spatial light modulator (SLM) input device and a CCD camera for output of results. This system was developed for pattern and character recognition applications. For only 3 mW incident power the correlation is performed in less than 1 microsecond.

We will report on the use of semi-insulating multiple quantum wells for optical image processing. Relevant design parameters for optimization of devices will be discussed. The performance of the optical image correlator system will be evaluated and compared with competing systems.

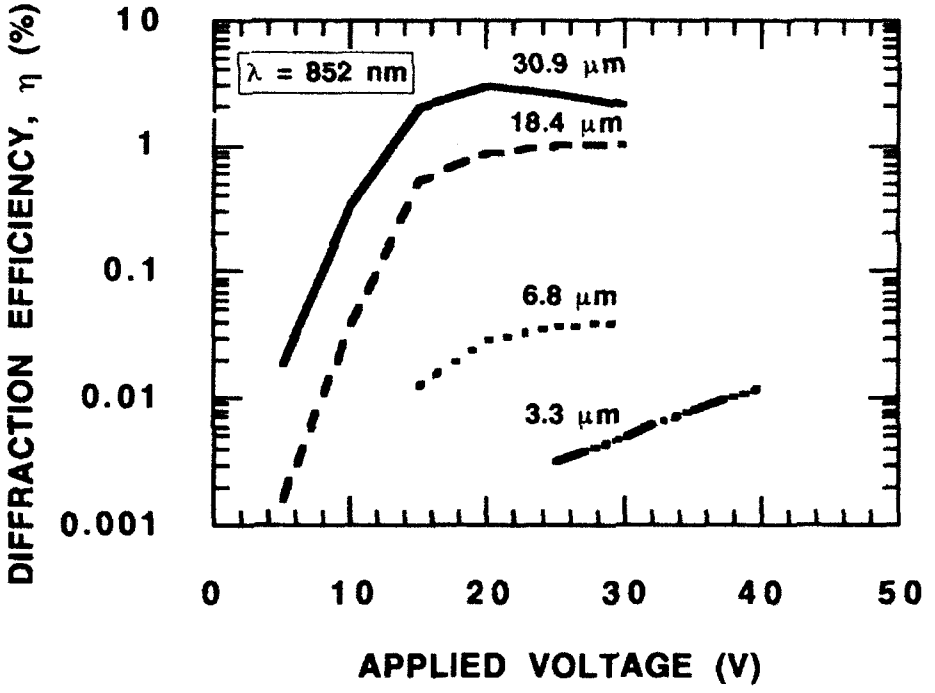


Figure 1- Diffraction efficiency as a function of grating period and applied voltage for the Cr-doped GaAs/AlGaAs MQW device.

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L-SEED AND F-SEED SMART PIXELS

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This paper will be a basic tutorial on two classes of Smart Pixels developed with the Self Electro-optic Effect Device (SEED) technology. The principal building block for both classes is the Quantum-Well diode (QW-diode), depicted schematically in Figure 1a. By virtue of the Quantum Confined Stark Effect [1] the QW-diode can act both as a photodetector with a voltage variable responsivity and as a voltage variable photo-modulator. Because of these two properties, the QW-diode can be reverse-biased through a load to produce a SEED (Fig. 1b&c) [2], which enables light beams to modulate other light beams for optical switching. A proper SEED operation occurs when a "signal" beam (or beams) sets the floating node voltage, V_N (Fig. 1b&c), to one of the DC voltage rails, and then a "read" beam (or beams) in effect reads the value of V_N, when its intensity is modulated be the QW-diode according to the value of V_N. It is critical, that the read beam itself not alter the value of V_N during the reading process. Another useful configuration (for Smart Pixels) is the optical transmission gate (Fig. 1d) consisting of two back-to-back photodiodes (not necessarily QW-diodes). When both diodes are illuminated, the voltages V_{N1} and V_{N2} will tend to equalize, whereas when the diodes are not illuminated V_{N1} and V_{N2} will tend to maintain their values, whatever their relative polarity.

The first family of Smart Pixels, based on SEED's, dubbed Logic-SEED's (L-SEED's) consist of electrically interconnected QW-diodes and perhaps ordinary photodiodes. (The photodiodes, of course, can be QW-diodes, or when in parallel with a QW-diode, can just be additional optical windows in the QW-diodes). The precursors of this family are the Symmetric SEED (S-SEED of Fig. 2a) [3] and the Dynamic SEED (Dy-SEED of Fig. 2b) [4]. The S-SEED operates as a toggle with differential optical input/output signals, and relies on bistability, when read by two equal intensity beams on the two QW-diodes, to keep V_N from changing during the read process. The S-SEED can perform as a logic gate, receiving two differential inputs, but then also requires a preset signal. The Dy-SEED is a toggle that operates with very short (in time) mode-locked laser pulses and relies on dynamic latching to keep V_N from changing during a read. The Dy-SEED can be an OR-gate or a NOR-gate, with single-ended signals. The circuit in Fig. 2c [5] is a true L-SEED which can perform the function of the four basic Boolean Logic gates with differential signals and without preset. It does rely on bistability for proper read-out. Another L-SEED, the circuit of Fig. 2d [6], is a 2×1 switching node, a basic building block for digital information routing systems. Its function is to receive two different differential signals, at the outer photodiodes, and to alternately pass one and block the other, depending on optical control signals on the transmission gates. It also relies on bistability for proper read-out. The talk will give a more detailed explanation (including experimental results) of these and other L-SEED's.

The FET-SEED (or F-SEED) family of Smart Pixels has just recently become possible as a result of a new and very versatile fabrication process [7] which allows the monolithic integration of QW-diodes with Field Effect Transistors (FET's). Each component is individually isolated, and then electrically interconnected with other components (as desired) by top surface metallic leads. Arbitrarily complex Smart Pixels are now possible, limited only by fabrication yield. A pixel consists of optical to electrical (O/E) signal converting input stages (Fig. 3a&b), driving electronic logic circuits, which then drive E/O converting output stages (Fig. 3c&d). Many of the L-SEED functions can be performed by circuits, consisting only of F-SEED input and output stages. The talk will focus on a discussion of these input and output stages and their requirements.

[1] D. A. B. Miller et al., Phys. Rev. Lett., V. 53, p. 2173 (1984).
[2] D. A. B. Miller et al., IEEE JQE, QE-21, p. 1462 (1985).
[3] A. L. Lentine et al., IEEE JQE, QE-25, p. 1928 (1989).
[4] G. D. Boyd et al., APL, V. 59, p. 2621 (1991).
[5] A. L. Lentine et al., Appl. Optics, V. 29, p. 2153 (1990).
[6] A. L. Lentine et al., OSA Proceedings on Photonic Switching, Vol. 8, H. S. Hinton and J. W. Goodman, eds. (OSA, Washington, DC, 1991), p. 60.
[7] L. A. D'Asaro et al., Postdeadline paper PD9, 1991 LEOS Annual Meeting, Nov. 1991.

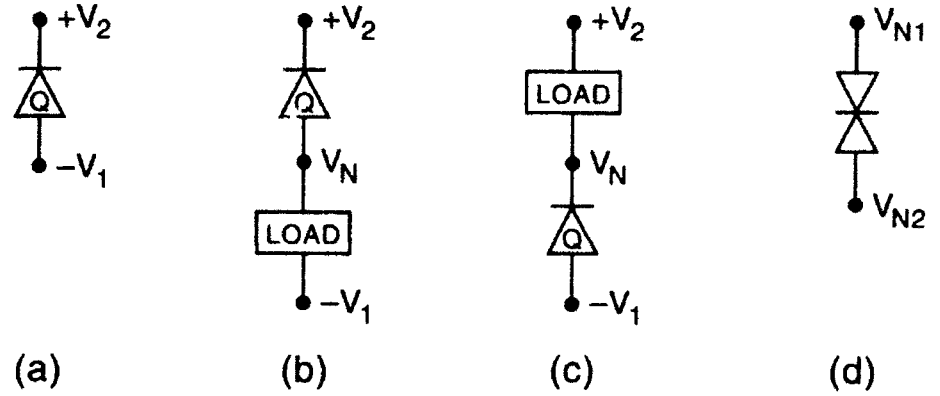


Figure 1. a) A schematic representation of a QW-diode, reverse-biased between two DC voltage rails; b) An illustration of a basic SEED, which is a QW-diode reverse-biased through a load with a floating node voltage, V_N, between them; c) An illustration of an alternative basic SEED; d) A schematic rendering of an optical transmission gate.

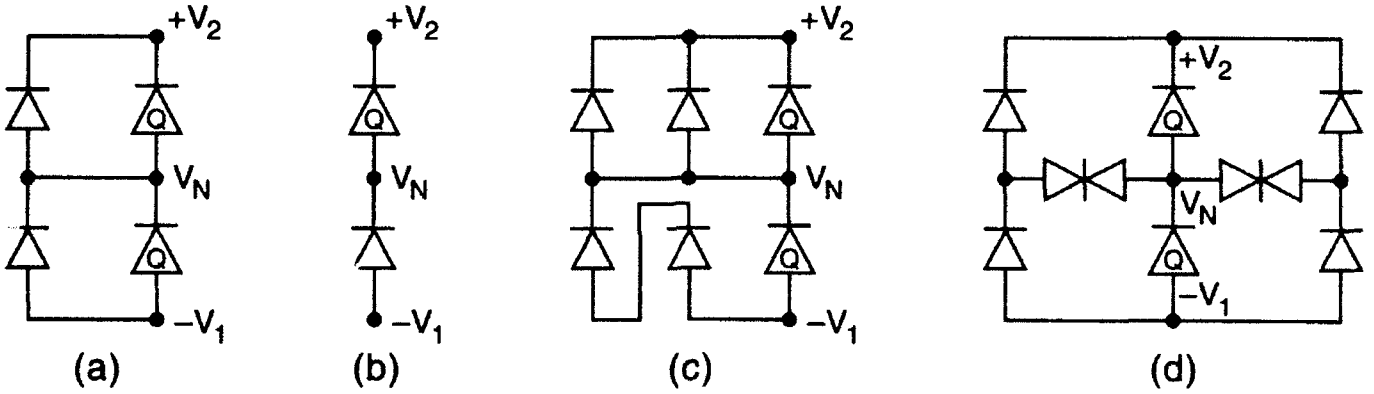


Figure 2. Schematic diagrams of: a) an S-SEED; b) a Dy-SEED; c) a Boolean Logic SEED; and d) a 2×1 switching node.

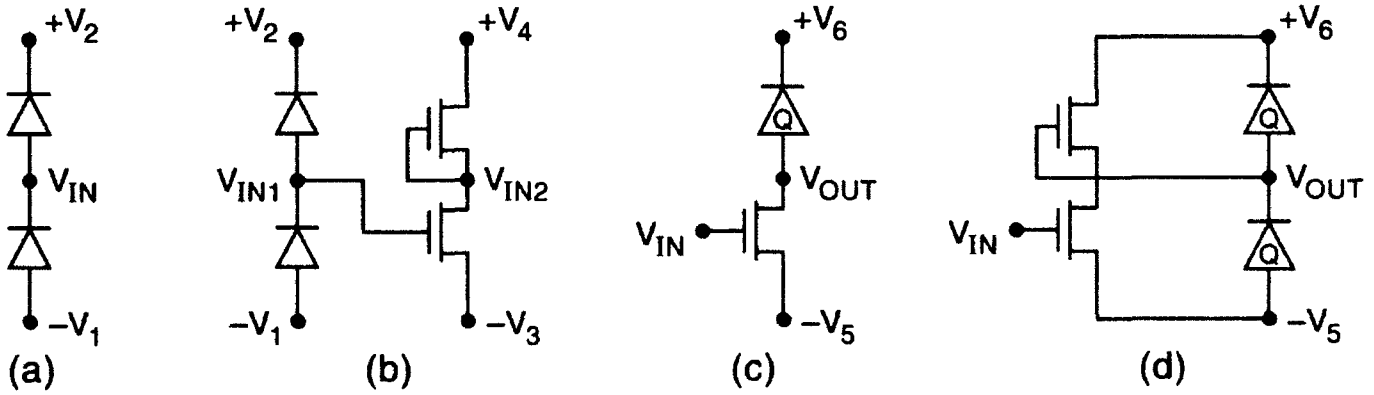


Figure 3. Schematic diagrams, for F-SEED's, of: a) a simple input stage; b) an amplified input stage; c) a simple output stage for dynamic operation; and d) an all-purpose output stage. The DC voltage rails, $-V_1$, $-V_3$, $-V_5$, V_2, V_4 and V_6, do not all necessarily need to be different.

TuC2

A COMPARISON OF L-SEEDs AND S-SEEDs: TOLERANCE TO SPATIAL POWER VARIATIONS

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Logic-SEEDs (L-SEEDs)[1] and symmetric-SEEDs (S-SEEDs)[2] have been obtained from AT&T Bell Laboratories. L-SEEDs are a smart pixel technology consisting of electrically connected quantum well p-i-n diodes that can implement complex functions beyond simple NOR gates. Several experiments are currently in progress which will compare the tolerance to spatial power variations of L-SEEDs and S-SEEDs[3]. These include quantifying the effects of the preset, offset bias and/or differential attenuator techniques which are used to provide increased tolerance. In addition to presenting experimental results of the operation of these devices as arrays of programmable logic gates, we will present a model with which the optimum operating points for various circuit configurations can be found.

We will present the use of L-SEEDs and S-SEEDs as the logic gate arrays in cellular logic image processor circuits. By considering specific applications and algorithms, we identify what functionality (or degree of smartness) is most desirable in such a processor. Simulations of trial optical implementations on an electronic array processor (the AMT DAP) combined with our experimental efforts, enable us to identify and quantify the various trade-offs encountered. As an example, the space-bandwidth of the lens used to image the S-SEED is limited. Consequently, the parallelism of the system (number of channels) may need to be decreased with increased pixel smartness due to the extra space that they require. For example, a L-SEED XOR gate has a 55 μm pitch which should be compared to the 20 by 40 μm pitch of a S-SEED.

We have recently concluded an experimental study of the characteristics of a S-SEED array. This has involved quantifying the effects of using different voltages, wavelengths and powers. The effect of the saturation of the exciton absorption at high power causes a reduction in contrast from >4:1 at low power to <3:1 at 100's of microwatts. The effect of increasing voltage is an increase in loop width and contrast. A static model has been developed to model these observations.

In addition, we have quantified the effect of small translational misalignments on the effective characteristic. The 3μm diameter beam has been positioned at different locations across the 5μm by 10μm window and the shape of the characteristic noted. This study reveals the precision with which it is necessary to align the system. Alternatively, if the setability of the position of the beams in the windows can be measured, it allows us to quantify the degradation in the characteristic caused by non-ideal alignment.

The required loopwidth and output contrast for correct operation has been the subject of a study[4] which concludes that loopwidth should be maximized and tolerance is relatively insensitive to contrast. The predictions of the model[4] were found to agree with experiment. An optical circuit was constructed with which primitive image processing such as noise removal[5] could be performed. The performance of this system when spatial noise was introduced was characterised. An example of the results of this investigation was the measurement of a non-uniformity of 25% and the prediction that with this non-uniformity some of the gates would not operate correctly with the low loopwidth and contrast used. This prediction was confirmed by experiment.

In addition, this optical circuit was characterised for operational errors at different voltages and with defocus introduced. Full details will be presented of this characterisation. It is found that it is impossible to get 100% of the 12[illegible]ata channels working simultaneously. The belief is that by using L-SEEDs, the tolerance to misalignment and spatial noise will be reduced to an extent that error-free operation will be possible.

The tolerance to spatial noise of a S-SEED array can be increased using a technique described in ref. [3] which requires differential attenuation of the outputs. Unfortunately, this technique cannot be used if the gate needs to be programmed using the preset[2] to be either a NOR or a NAND gate. The need with the CLIP architecture[6] to have programmable gates has forced us to consider a novel way of increasing the tolerance to spatial noise which we call offset bias. This technique consists of simply leaving the preset beam on during the write cycle. One advantage of L-SEEDs may be the lack of the need for this offset bias or of a preset.

[1] A.L. Lentine, F.A.P. Tooley, et al., "Logic SEEDs ...", J. Quant. Electron., to appear (1992): see also A.L. Lentine et al., Appl. Opt., 29, 2153 (1990).

[2] A.L. Lentine, et al., "A 2 Kbit array of S-SEEDs", IEEE Photonic Technol. Lett., 2, 51-53 (1990).

[3] F.B. McCormick, F.A.P. Tooley, et al., "S-SEED-based photonic switching network demonstration", OSA Proc. Phot. Switching, Vol. 8, 48-55 (1991).

[4] S. Wakelin and F. A. P. Tooley, "The tolerance of differential logic gates to spatial noise", to appear in Int. Jour. of Optical Computing 1992.

[5] F. A. P. Tooley and S. Wakelin, "Design of a S-SEED Cellular Logic Image Processor", submitted to Applied Optics 1992.

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TuC3 GaAs/AlGaAs FET-SEED SMART PIXELS WITH SEVERAL TRANSISTORS

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Massively parallel optical interconnection of electrical processing elements requires the intimate integration of a controllable optical element with semiconductor electronics. To this end we have pursued the integration of GaAs microelectronics technology with GaAs multiple quantum well (MQW) modulators. We have chosen doped channel HFETs, or doped channel MIS-like FETs (DMTs), as our GaAs electronic component.[1]

Planar process technology has been developed that permits the integration of both modulator and transistor in a planar process requiring a single growth step.[2] Growth of the structure is by molecular beam epitaxy and a schematic cross-section is shown in Fig. 1. This process permits the realization of circuits having varying degrees of complexity. Previously, we have reported the operation of single stage amplifier circuits having at most two transistors.[3] Here we demonstrate the operation of circuits composed of several transistors, some having multiple stages of amplification. As an example, we present in Fig. 2 the circuit diagram for the most complex circuit we have to date realized, consisting of a differential amplifier input stage and and two complementary output drivers. Both the inputs and the outputs are taken from $p-i-n$ MQW devices. At the input we take advantage of their detecting properties, while at the output their voltage dependent absorption is used to modulate a constant power falling on the output diodes. The detected output signals are shown in Fig. 3. Two complementary inputs were provided by directly modulated laser diodes at about 850 nm having 216 μW and 39 μW average power. The period was 6 ns (166 MHz) for input pulse energies of 1.3 pJ and 234 fJ, respectively. Each output window was illuminated with 130 μW at approximately the same wavelength. The phase delay in the complementary outputs is actually present. We speculate that it arises from the strong asymmetry in the input stages (note the input powers were different by about a factor of 5), which may come from an unintentional process variation in the resistors. Other circuits have also been operated in which the input stage consists of two diodes in series. These were found to have less asymmetry, with roughly 200 fJ switching energy at 40 MHz operation.

In summary, we experimentally demonstrated the 160 MHz operation of a 9 transistor smart pixel with 2 optical inputs and outputs with less than 1 pJ switching energies.

1. see, for example, S. S. Pei, N. J. Shah, in *Introduction to Semiconductor Technology*, (Wiley, New York, 1989) Ch. 3.
2. Our process is an extension of that described in L. A. D'Asaro, L. M. F. Chirovsky, R. F. Kopf, S. J. Pearton in *Advanced Processing and Characterization Technologies* P. H. Holloway, ed. (American Vacuum Society Series 10. Conference Proceedings No. 227, American Inst. of Physics, New York, 1991) p. 192.
3. T. K. Woodward, L. M. F. Chirovsky, A. L. Lentine, *1990 Annual Meeting of the Lasers and ELectro-Optics Society*, Postdeadline paper PD-10. and T. K. Woodward, L. M. F. Chirovsky, A. L. Lentine, L. A. D'Asaro, E. J. Laskowski, M. Focht, G. Guth, S. S. Pei, F. Ren, G. J. Przybylek, L. E. Smith, R. E. Leibenguth, M. T. Asom, R. F. Kopf, J. M. Kuo, M. D. Feuer, to appear *Photonics Tech. Lett.* June 1992.

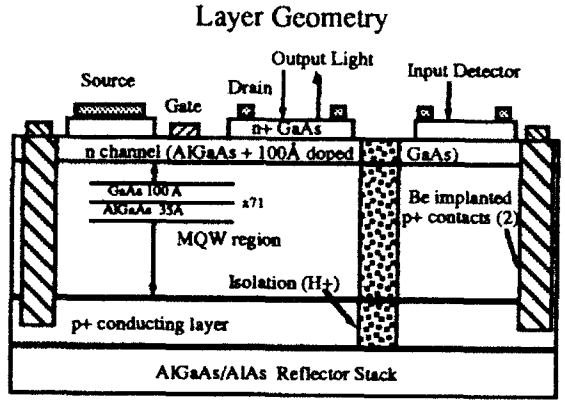


Figure 1: a schematic structure cross section.

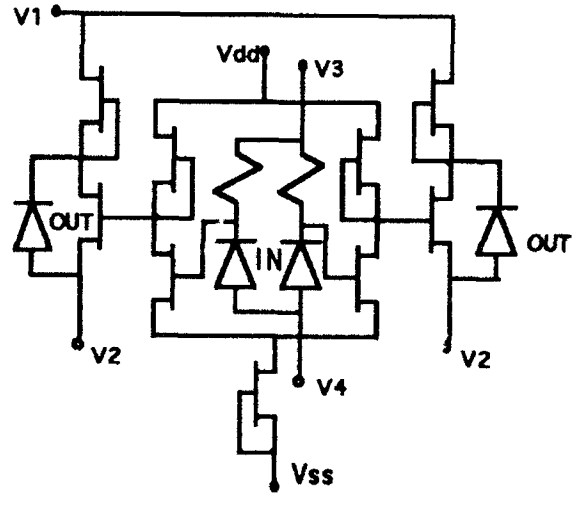


Figure 2: A schematic of the integrated circuit. Inputs and outputs are MQW *pin* diodes.

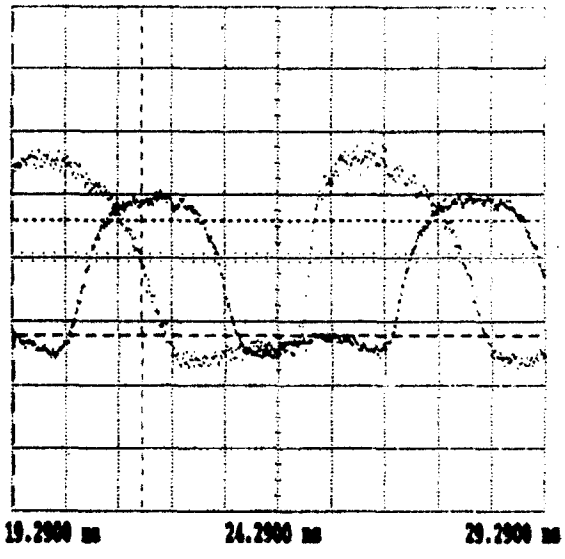


Figure 3: Both output oscilloscope traces, zero at bottom of plot. Horizontal scaling is 1 ns per division.

TuC4

BATCH FABRICATION AND TESTING OF FET-SEED SMART PIXEL ARRAYS

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We have fabricated and tested arrays of smart pixels using FET-SEED (Field Effect Transistor - Self Electro-optic Effect Device) integrated optoelectronic technology on GaAs-AlGaAs MBE grown epitaxial layers. The FET amplifiers placed between the MQW (Multi Quantum Well) photodiodes and the MQW exciton absorption modulators enable us to avoid the problem of slow switching speed due to limited photocurrent.

Fig. 1 illustrates the wafer structure and device design. We use a reflection type modulator[1] in order to provide a robust structure suitable for batch fabrication[2] and for heat sinking. A DMT[3] (Doped Channel) MIS-like Field Effect Transistor) structure is chosen for reproducible fabrication, low optical absorption at the exciton wavelength, adequately high source-drain operating voltage ($\simeq$ 10 v), and speed ($f_t \simeq 10$Ghz for 1μm long gates). The method of integration is an extension of the previously described buried interconnect structure[4] which uses shallow etching to isolate the top n^+ contact layer, proton implantation to isolate regions of the buried p-layer for the definition of the active devices, and Be implantation for contacts to the buried p-layers. The gate fabrication uses a self aligned technique in which the same resist serves for both the plasma stop-etch to remove the n^+ layer above the DMT channel and for definition of the lifted-off gate metal. The p-layer is used not only as a terminal for the PIN MQW photodiodes and modulators, but also as a control electrode under the DMTs, where it shields the gate regions from stray electric fields which are known to produce sidegating.

The photograph in Fig. 2 shows a small section of a representative array of 128 optoelectronic circuits. The yield of good arrays as measured by a simple test was ~50% for the first full wafer. Each circuit in the array contains two MQW photodiode input windows (10μm square), a DMT amplifier with a 10μm wide gate, and a MQW modulator output (10μm square). This circuit with 5μm dimensions switched the output optical modulator at a speed of 170 Mb/s with a contrast of 3:1 when driven with an input optical power of 70 fJ. Inasmuch as the output power can be much larger than the input, these devices are cascadable.[5] Other and more elaborate optoelectronic circuit arrays have also been made and will be reported elsewhere.

1. G. D. Boyd, et. al., "Appl. Physics. Lett., vol. 50, pp. 1119-1121, 1987.
2. L. M. F. Chirovsky, et. al., in **OSA Proceedings on Photonic Switching**, J. E. Midwinter and H. S. Hinton, Eds. Optical Society of America, Washington, DC, vol. 3, pp. 2-6, 1989.
3. H. Hida, et. al., IEEE Trans. Electron Devices, vol. ED-34 pp. 1448-1455, 1987.
4. L. A. D'Asaro, et. al., in **Advanced Processing and Characterization Technologies**, P. J. Holloway, Ed., American Vacuum Society Series 10, Conference Proceedings No. 227, American Institute of Physics, New York, pp. 192-194, 1991.
5. F. B. McCormick, et. al., SPIE 1396 **Applications of Optical Engineering: Proceedings OE/Midwest**, pp. 508-514 (SPIE, Bellingham, WA., 1990.)

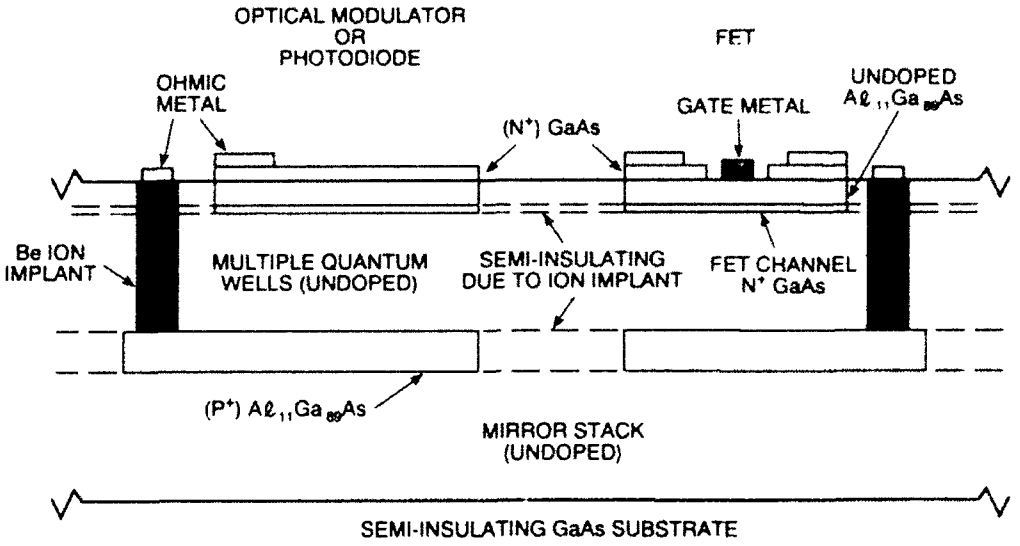


Fig. 1. Schematic Cross Section of the FET-SEED Structure

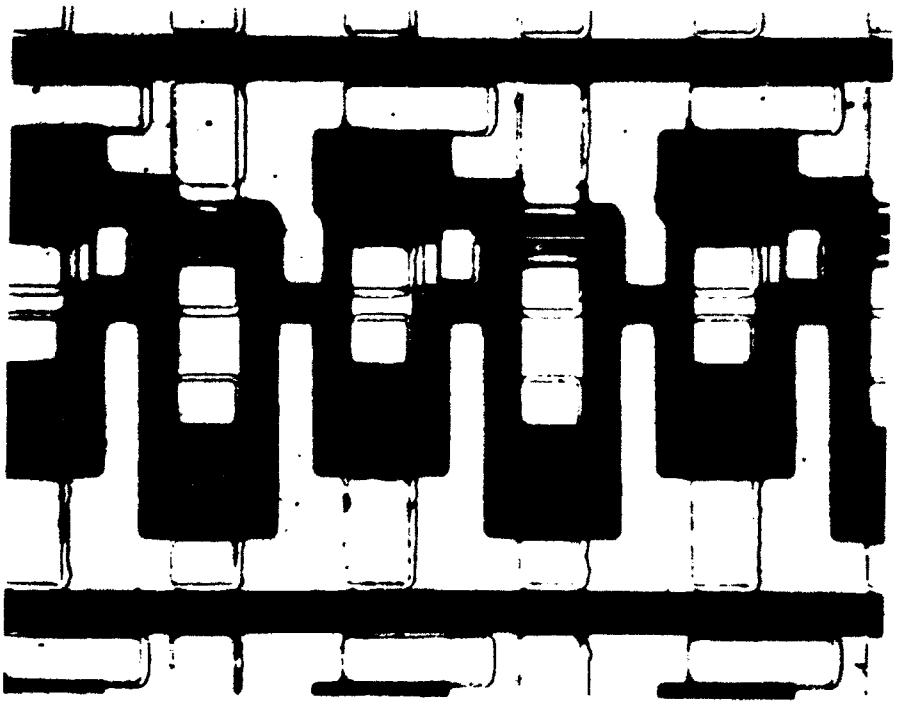


Fig. 2. Photograph of part of a FET-SEED Smart Pixel Array

TuC5

THE MONOLITHIC OPTOELECTRONIC TRANSISTOR

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The monolithic optoelectronic transistor (MOET) is a smart pixel device that performs thresholding and logic operations and can be tailored either for optical logic applications or for optoelectronically implemented neural networks. It displays optical gain, is cascadable, and has an abrupt switching threshold and saturated "on" and "off" output states.

The circuit of figure 1 shows the operation of the most rudimentary version of the MOET, which performs optical inversion. A p-i-n diode with a multiple-quantum-well (MQW) intrinsic region serves as an input photodetector and a separate one serves as an output modulator. The photocurrent from the input detector flows through a double-barrier resonant tunneling diode (RTD), which has a region of negative differential resistance in its I-V characteristic. When the photocurrent exceeds the peak current of the RTD, the RTD abruptly switches to a higher voltage operating point and this voltage change is amplified by a JFET to drive the output modulator. Since the modulator can be illuminated at much higher optical power than required for switching at the input, the MOET displays optical gain. We project that the MOET will switch in 10 ns with 10 μW of input power, or a switching energy of 100 fJ.

The p-i-n detector/modulator structure uses an asymmetric Fabry-Perot to achieve a high contrast reflection modulator and a highly efficient photodetector. This structure requires high purity and low background doping in the MQW, good control of layer thicknesses, and very high uniformity in layer thickness (<0.1%) over the area of an array. Using gas-source MBE, we have grown a detector/modulator structure with 65:1 contrast at 8 V, high quantum efficiency as a photodetector, and high thickness uniformity (0.3% over a 2-inch wafer).

The RTD peak current determines the input optical power required for switching. Therefore, high optical gain requires an RTD with low peak current. A systematic study to optimize barrier composition has yielded RTDs with peak current densities under 100 A/cm^2 with peak-to-valley current ratios of more than 2.

We discuss the growth and fabrication of the MOET structure and the successful achievement of high performance in each of its critical components. Alternative versions of the MOET will be described.

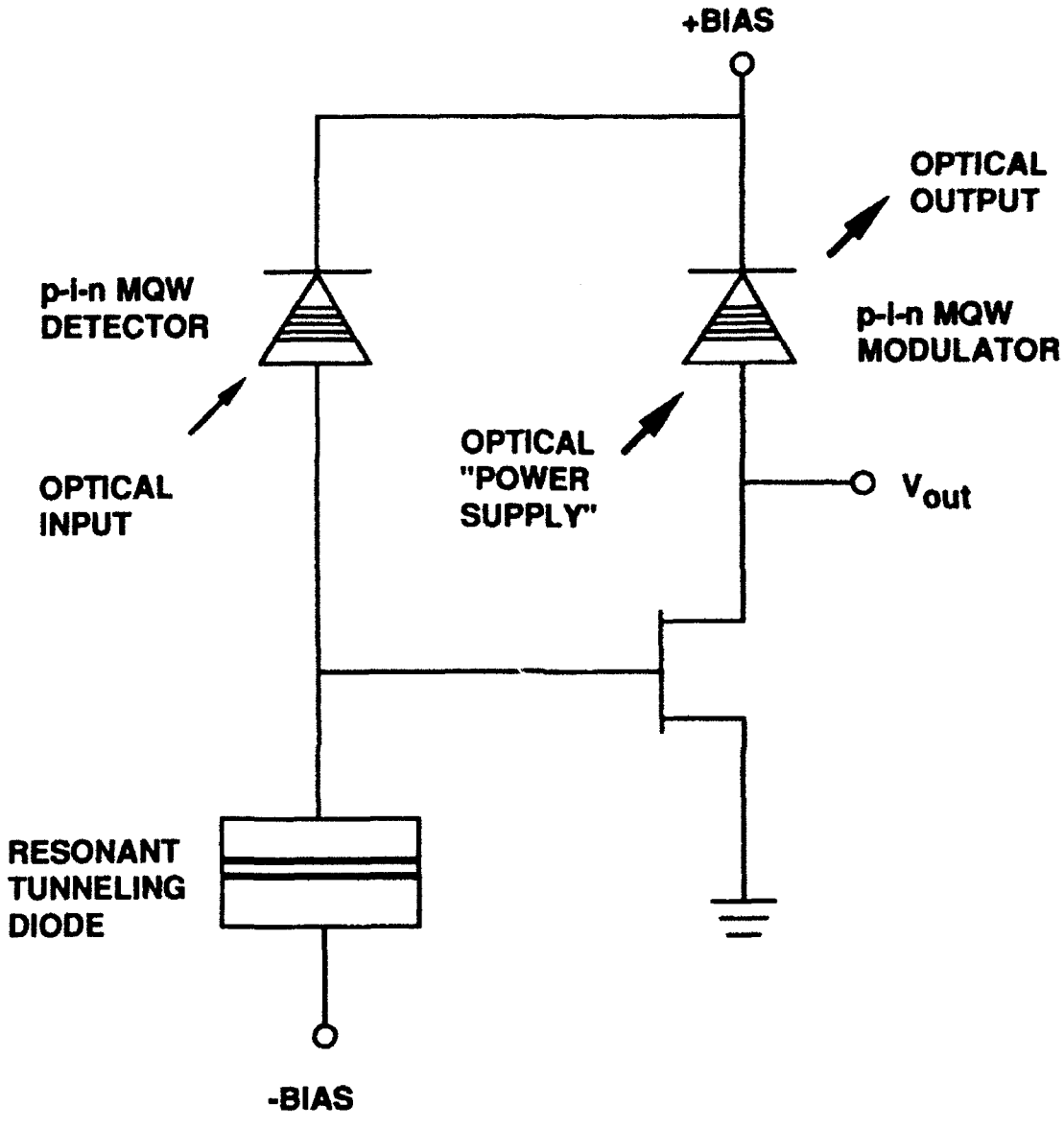


Figure 1 The circuit of the monolithic optoelectronic transistor

TuD1 OPTOMECHANICS OF SMART PIXEL SYSTEMS

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1. Introduction

Routing signals as beams of light within high performance digital systems offers the potential benefits of high bandwidth, high density connectivity, low signal skew, and low degradation of signal quality. Availability of 2-D optoelectronic device arrays has enabled the fabrication of demonstration systems that require simultaneous optimization and integration of several technologies, and this has begun to focus attention on the practical issues of optical design, alignment, stability, reliability, repairability, and cost.[1] For optical systems, these issues generally fall under the heading of *optomechanics* or *system packaging.*

The advent of smart pixels introduces two important changes to the system packaging problem. In the past, few device configuration choices have been available, and the optomechanical designs of demonstration systems are usually optimized to match available device characteristics. The flexible integration of electronics and optoelectronics may now allow us to engineer the device characteristics to match the most efficient packaging schemes. For example, electronic signal amplification can enable the use of larger detectors which will ease alignment tolerances. The limited capabilities of initial optoelectronic devices are also partially responsible for the high degree of coupling between architecture, device, optical design, and mechanical design choices. This coupling requires that systems be optimized collectively, and limits development of "standardized components", as well as general purpose systems. Flexible configuration of specific device characteristics (detector/source sizes and locations, receiver sensitivities, electrical signal access and processing, etc.) may allow the creation of generic interfaces not only at the device level, but also within the optics and mechanics. This flexibility introduces several optical and mechanical design tradeoffs.

2. Optical and Mechanical Issues

Initial optical switching an computing demonstrations used devices with a high density of optical I/O, and the high space-bandwidth product (SBWP) provided by conventional "macrolens" imaging was efficiently used. Smart pixels integrate additional electronics which lower the optical I/O density significantly. Hence, only moderate ($<10^4$) SBWPs are needed, and most of the macrolens SBWP is left unused. Thus, depending on the optical I/O density, three types of imaging may be useful: "macro" lenses, microlens arrays, and hybrid macro-microlens systems.[2]

Macrolenses image an entire array of devices is imaged onto the next device array. This macrolens imaging technology is a well understood and established technology. As a result, several complex macrolens optical free-space system experiments have been demonstrated.[1] Macrolens optical systems characteristics include high SBWP (10^4–10^6 object/image points), low time-skew, multi-element lenses and precise element mounting. A well-corrected refractive telecentric imaging step can maintain synchronization of the parallel optical connections to within a few femtoseconds. The relatively long focal lengths generally used (10-30mm) result in significant physical distances for the optical interconnections, and thus latency.

Microlens arrays provide high resolution only at the optical I/Os by dedicating a separate optical system for individual or small groups of optical signals. Since the beam spreading due to diffraction is inversely proportional to the transmitter/receiver density, there is a tradeoff between the connection capacity and the distance between microlens arrays.[3] This distance may be necessary for the interconnection and fan-in functions, or simply to connect to the next chip, MCM, or board. Propagation distances of several centimeters appear feasible with microlenses 100-300 μm in diameter. Microlens array systems may be characterized by lower SBWP and simple lenses, although the complete optical system design may be quite complex.[3] Time skew between channels will accrue proportionally to the globality of the interconnect. Inexpensive fabrication and replication of microlens arrays should minimize the costs, but new micro-optomechanical techniques for aligning and mounting microlens arrays are required.

Hybrid lenses use macrolenses to control the diffraction of the signal beams and microlens arrays to provide most of the focussing "power" in the system. The macro "front lens" operates at high f-number (f/10-30) and provides the geometric

image magnification. The microlenses operate at low f-number (f/1 to f/5) and provide most of the lens numerical aperture. These lenses possess have moderate SBWP and lens design complexity, and low signal skew. The relatively long focal lengths (10-50mm) result in a constant delay (latency) across all connections.

In addition to laboratory demonstrations constructed on optical benches with discrete optics, electronics, and mechanics, we can define two broad package integration levels. The **custom optical bench/frame** level of integration has been reached by some FSOI demonstrations,[1] and it is used in some commercial products such as optical correlators, free-space optical communication systems, and telescopes for tracking or reconnaissance. High reliability and alignment stability is demonstrated by the many flight qualified optical systems used in military and space applications. Lower performance systems like supermarket bar-code scanners also demonstrate the viability of this integration level. However, manufacturability and the relative costs of these systems suffer from the still low level of integration.

Monolithic optical bench packages integrate the optics, optomechanics, and optoelectronics on a commmon substrate or substrates. They require the most new technology development, but offer the best chance of achieving low cost and ease of manufacture. One drawback is the potential for greatly increased coupling between different system aspects. For instance, in monolithic packages, thermally induced stresses may affect the alignment procedures, long term system stability, and the system's aging characteristics. In general, thermal management will be a critical issue in monolithically integrated FSOI packages, because of the high density and lack of accessible surface area. Another important issue may be the lack of test and/or repair capability. As in electronic packages, when the level of integration reaches a certain point, test and repair are no longer feasible, and the package is simply discarded and replaced. For this approach to be economically practical, the costs of the optics, optoelectronics, and assembly must decline so that the total package costs may be kept very low.

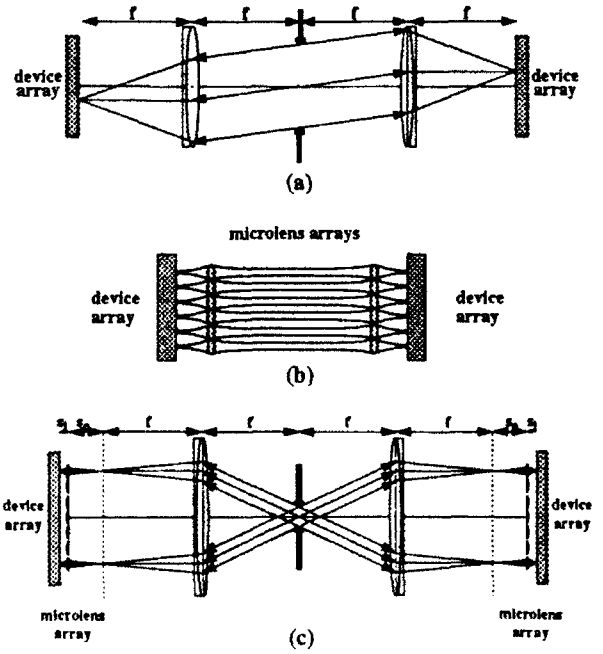
The collaboration and support of my colleagues in the Photonic Switching Technologies group is gratefully acknowledged.

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Optical system options: (a) macrolens (b) microlens arrays (c) hybrid micro-macrolens

TuD2

FABRICATION, ASSESSMENT AND MODELLING OF MICROLENS ARRAYS

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Arrays of microlenses may be important components in the development of optically interconnected electronics since they can be used to provide relatively long (~ 20 mm) connections between optical ports spaced by > 200 μm[1,2]. This paper will present analysis of the accuracy required for the fabrication of microlenses and construction of a simple two-lens optical link. It will present calculations which extends the tolerance analysis presented in reference [1]. In addition to the consideration of the effects of clipping, focal length variation, initial source waist variation and defocus which were shown to be important in [1], we will also consider the effects of mode quality (M^2). A model currently being developed which encompasses the cumulative effect of the tolerance to all these parameters will be described. It will be shown that the system constraint of having tolerance to reasonable variation in these parameters leads naturally to the existence of optimum operating points. This study will identify how a 'stable' operating point may be found and what quality of lens is required.

In addition, we have recently fabricated three types of microlens arrays: refractive lenses (using mask erosion of melted positive photoresist), multi-level diffractive lenses and volume holographic lenses(using DCG). These three techniques will be explained and compared. In particular, the issues that will be discussed will include: packing density, uniformity of focal length, optical quality, fill factor, field of view, efficiency and operating wavelength range. Each type of microlens has limitations.

Holographic lenses fabricated in DCG are not readily used at a wavelength significantly different from that used to write the lens(488nm or 514nm). However, it is possible to record the lens so that it can be nearly diffraction-limited at a different wavelength[3]. The minimum size of lens is large at around 200μm to ensure that there are sufficient fringes for high efficency. The quality of the lenses is high since it can reproduce the original wavefront used in recording. There is a problem with accuracy of placement which can be overcome using high quality micropositioners. The principle drawback of volume holography-produced microlenses is that initial fabrication and replication is expensive and time-consuming. Typical results achieved in the holography laboratory at HWU are (simultaneously): >90% overall efficiency into a "diffraction-limited" spot, operation at 850nm, array sizes of 56 by 56 square aperture lenses with 100% fill factor, uniformity of focal length better than the measurement technique (5%) and off-axis operation at 36 degrees. This last characteristic is particularly troublesome. It generally means that operation with a deflector hologram to bring the rays back on-axis is neccessary.

The other two types of microlens array are both on-axis and use microlithography to ensure that the lens is placed in the required position with sub-micron accuracy. The other benefit of microlithographic techinques being used is that all of the lenses are prepared simultaneously with a consequent saving in time and cost. Diffractive lenses can in principle be of any size or focal length. However, the minimum feature size and number of phase levels constrains them[1]. The efficiency of an ideal L-level diffractive lens is $\mathrm{sinc}^2(1/L)$. A binary lens diffracts only 41% of the incident light into the required order. The efficiency can only be increased using more masks: 81%(L=4 or 2 masks) and 95%(L=8 or 3 masks). The lithographic resolution(x) required to fabricate a diffractive lens is related to the f-number(f/#) by $xL=2\lambda f/\#$. Thus, it is only possible to make a f/3 lens with a diameter of 300μm with four levels if 1μm minimum feature size lithography is used. A variety of diffractive lenses have been made in the HWU Micro-optics Laboratory, these include 4 level and 8 level arrays of 16x16 f/4 lenses on 200μm centres and a 4x4 arrays of f/4 lenses on 800μm centres.

These two arrays have been used as the fan-in optics in a matrix-matrix crossbar photonic switch[4]. The microlens array collimates each beam in a aerial image formed by a compound lens, this is followed by the macrolens array which focuses 4x4 groups into multimode fibres. In addition, an array of 32x32 200μm diameter diffractive lenses has been designed which all operate to bend the beams through different angles. The results of experiments with these lenslets to provide a perfect shuffle interconnect will be presented.

A well-known technique used to create microlens arrays is to form pillars or cylinders of photoresist which when melted take up a hemispherical shape due to surface tension. Thus, the lens will have high efficiency especially if it is antireflection coated after fabrication. A problem with these lenses is that large diameter (>100μm) and slow lenses (f/#>3) are difficult to fabricate due to the photoresist forming shapes that are not lenticular. The gap between lenses means that the fill-factor cannot be 100%. Typically, a 10μm gap is left between adjacent lenses. The shape of the lens is such that the spot created is not diffraction-limited, usually there will be significant spherical aberration. An approach adopted by HWU Micro-optics Laboratory has been to form the photoresist lenses on top of pillars of previously etched glass, and then use mask erosion to transfer the hemispherical shape into the glass[5]. This prevents resist spreading. Preliminary results will be presented of this technique. Arrays of 64x64 50μm and 125μm diameter lenses have been fabricated.

Assessment of the optical quality of microlens arrays is a critical issue. The measurement of focal length and its uniformity across the array and from array to array are important for refractive lenses which may have significant variation. In addition, the spot size and shape formed by these lenses must be measured carefully. HWU is currently equipping a optical assessment laboratory which will be used for these measurements. It will include a Mach-Zehnder Interferometer to access the optical quality of the diffractive and refractive lenses we have produced. In addition, the effect on the M^2 of light passing through a two microlens relay will be measured using a slit scanning spot profiler. This sort of analysis (e.g. system tolerancing, fabrication analysis and quantitative component testing) is one of the main issues that will "make or break" this idea, since it determines the feasibility of novel packaging.

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TuD3 PARALLEL OPTICAL INTERCONNECTIONS USING SURFACE-EMITTING MICROLASERS AND A HYBRID IMAGING SYSTEM

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SUMMARY

The current development of arrays of opto-electronic devices that combine electronic logic and optical input/output ("smart pixels" [1]) may result in a significant step towards the actual use of optics in a computing environment. Smart pixel devices have been proposed based on modulators [2-3] and surface-emitting microlasers [4]. The current model for a smart pixel devices uses a relatively small area for the optical input and output that is surrounded by a larger area that is occupied by electronics. The IO ports in an array of smart pixels are therefore separated by a relatively large distance and form a "dilute array" [5].

For interconnecting arrays of smart pixels, it seems to be a natural choice to use multi-faceted optical components consisting, for example, of gratings for beam deflection and microlenses for beam collimation and focusing. A specific optical system that combines micro- and macrooptics was suggested and discussed recently by Lohmann [5] (see Fig. 1). It is essentially a 4f-imaging system where microlens arrays are added near to the input and the output planes. Light from each source located in the input plane I is first collimated by a microlens before it passes throught the 4f-system. A second microlens array is used to focus to the output positions in plane O.

A hybrid imaging system was demonstrated and analyzed. The use of a hybrid imaging system breaks up the imaging task in a favorable way which results in reduced performance requirements for the single elements and some of the alignment tolerances of the whole system. In order to generate small spots the microlenses in A1 and A2 need to have a small f-number, but they operate over a very limited field. The big lenses L1' and L2' are required to have a certain diameter to transmit all the light, but they can be slow lenses. These considerations allow one to choose different types of microlenses that are particularly suited for the different sub-tasks in the hybrid system. For example, in our experiment, the lenslets A_1 and A_2 were conveniently implemented as fast refractive microlenses (f/#≈3, diameter: 90 μm), the big lenses were implemented as slow diffractive lenses (f/#≈30, diameter: 2 mm). The use of diffractive lenses to implement L1' and L2' is particularly suitable for an integrated implementation of a hybrid imaging system based on the planar optics concept since aspherical lenses are required [6].

In the experiment, a 4x4 array of top-surface-emitting microlasers [7] operating at 850 nm was used as the input array. The separation between individual lasers is 100 μm in each direction. The experimental result is shown in Fig. 2. The size of the array was limited by the electric connections required to address the lasers. In another experiment, where the lasers were replaced by a mask illuminated from a single laser source, 16x16 channels were transmitted. From these experiments, it is estimated that even larger arrays can be imaged.

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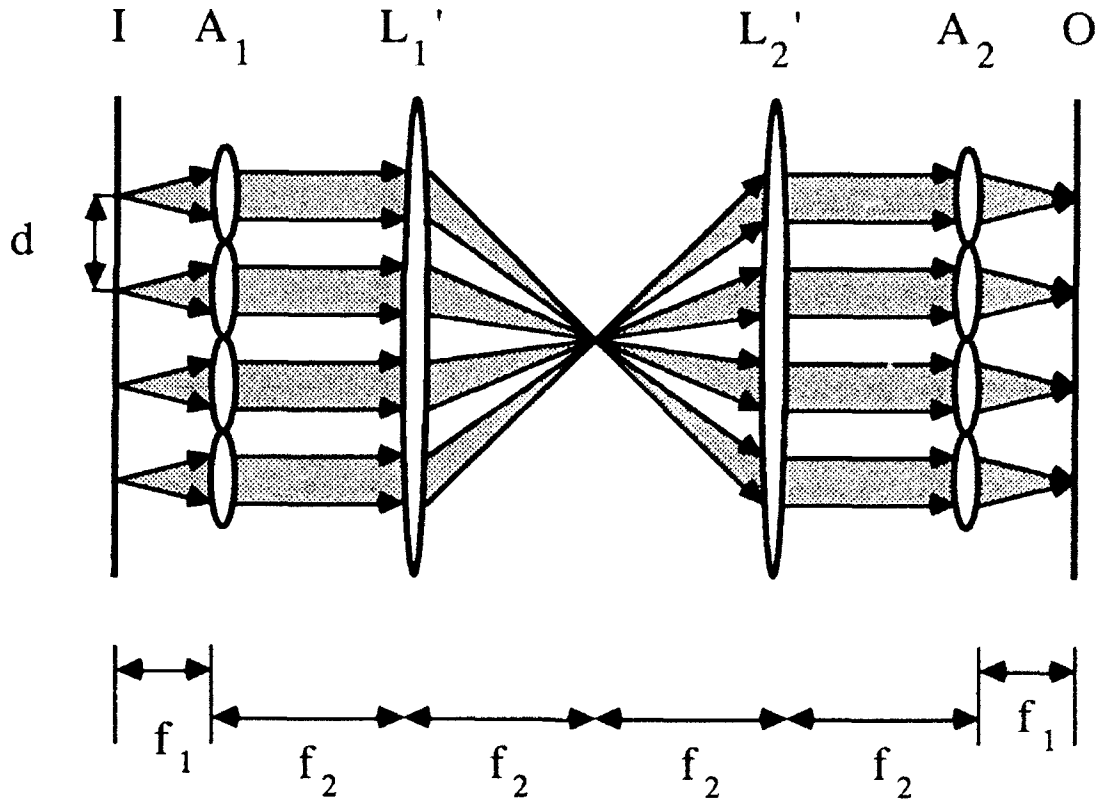


Fig. 1: Hybrid imaging system. I - input plane with a pixel separation d, A1 and A2 - lenslet arrays with the same pitch, L1' and L2' are macrolenses.

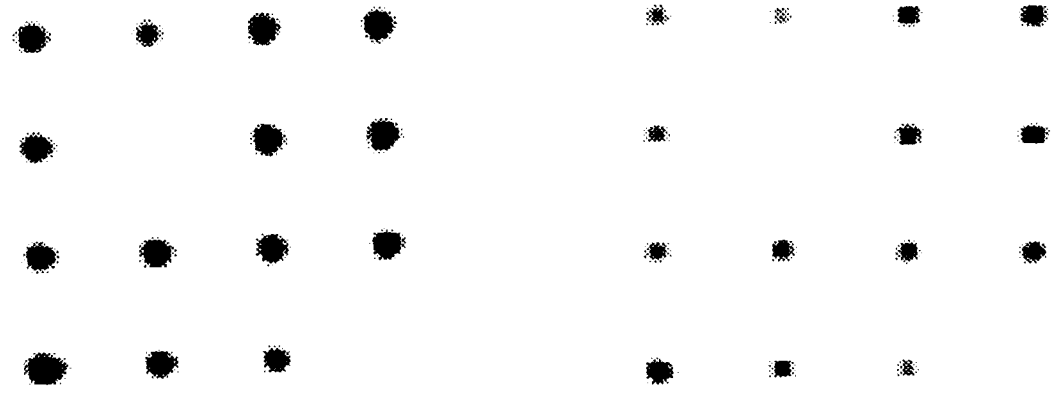


Fig. 2: Experimental result (left: input, right: output). Pixel separation was 100 μm in each direction.

TuD4

GUIDED-WAVE OPTIC DIRECT INTERCONNECTION FOR TWO-DIMENSIONAL OPTICAL PATTERNS

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Many optical interconnection technologies have been proposed, most of which can be broadly classified as either guided-wave or free-space type optics. Guided-wave optic interconnections using optical fibers or waveguides can be practically implemented because they match with conventional fiber-optic transmission technology. By contrast, free-space optic interconnections can carry large amounts of data in the form of two-dimensional optical patterns, though they are more difficult to integrate. In this paper, we propose a new class of optical interconnections, in which a two-dimensional optical pattern is directly transmitted through a multimode fiber or waveguide. It could offer both the advantages of the flexiblity of guided-wave optics and the massive parallelism of free-space optics.

Although direct image transmission utilizing phase conjugation has been proposed[1], a viable implementation has yet to be realized because of the practical difficulty of preparing two identical fibers for transmission. However, use of a phase conjugation mirror (PCM) with an image-input function enables guided-wave optic interconnection for optical patterns, as shown in Fig. 1. With this approach, reference and object light from the receiver site are conveyed to the transmitter through a single-mode and a multimode waveguide, respectively. When the reference beam is perpendicularly incident on the PCM, the conjugated wave is reflected and transmitted back through the multimode waveguide. When an interference pattern on the PCM is modulated by the optical data pattern, the optical pattern input on the PCM can be reconstructed at the receiver site through an imaging lens because the phase distortion of returned beam through the multimode waveguide is compensated. .

The interconnection proposed above has been experimentally demonstrated using a multimode fiber (1 mm in diameter by 200 mm in length) and an optically-addressed spatial light modulator (SLM). The SLM[2], consisting of an a-Si:H photoconductor and a ferroelectric liquid crystal (FLC), acts as a PCM with an image-input function. Two coherent beams from a He-Ne laser were incident on the photoconductor via the FLC to record the interference pattern[3]. The optical pattern to be transmitted was focused on the photoconductor with another incoherent light source. The pattern illumination modulated the interference pattern on the SLM since the interference pattern were erased in the illuminated regions. One result of the experiment is shown in Fig. 2. The intensities of the coherent beams and data illumination light are 0.5 mW/cm^2.

This interconnection technology could also be applied for reconfigurable interconnection among processors and memories, where parallel access to optical storage would support a huge throughput capacity[4]. Switchable parallel access from two receiver sites to the same optical data has been demonstrated, as shown in Fig. 3. A He-Ne laser beam is split into three beams. One is a reference beam, and the others are object beams which are separately sent to the SLM through a fiber and a shutter. Two shutters (S1,S2) are placed in the path of each object beam for access switching. Experimental results are shown in Fig. 4., where the optical data were readout by CCD sensor configured for each fiber. And the same data pattern was also readout by both sensors simultaneously. The significant implication is that multiple processors can access the same memory in parallel at the same time.

In conclusion, we have proposed a guided-wave optic interconnection for optical patterns that uses a spatial light modulator which acts as a phase conjugation mirror with an image-input function. This technology could have a wide range of applications, including parallel access to optical memories from multiple processors.

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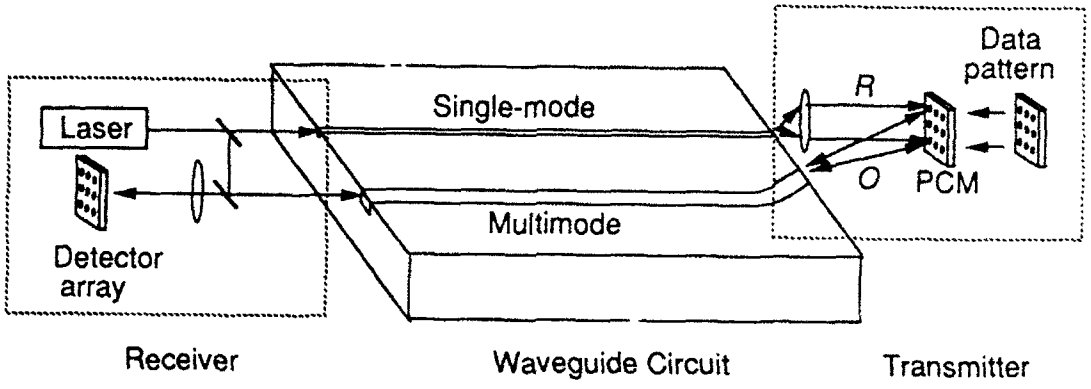


Fig. 1 Schematic of guided-wave optic interconnection for optical patterns.

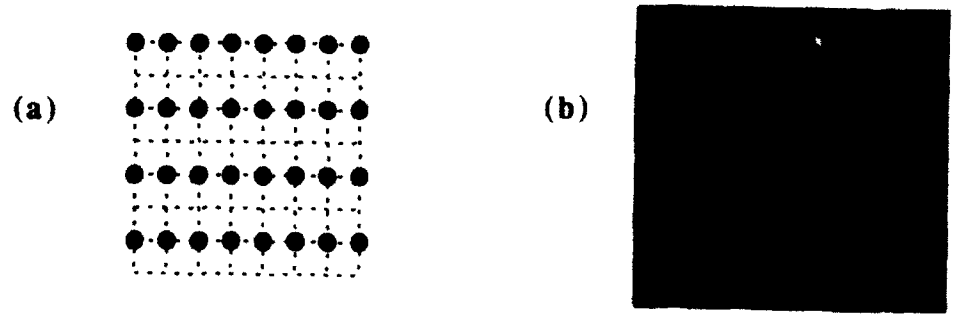


Fig. 2 Original data pattern (a) and transmitted data pattern (b).

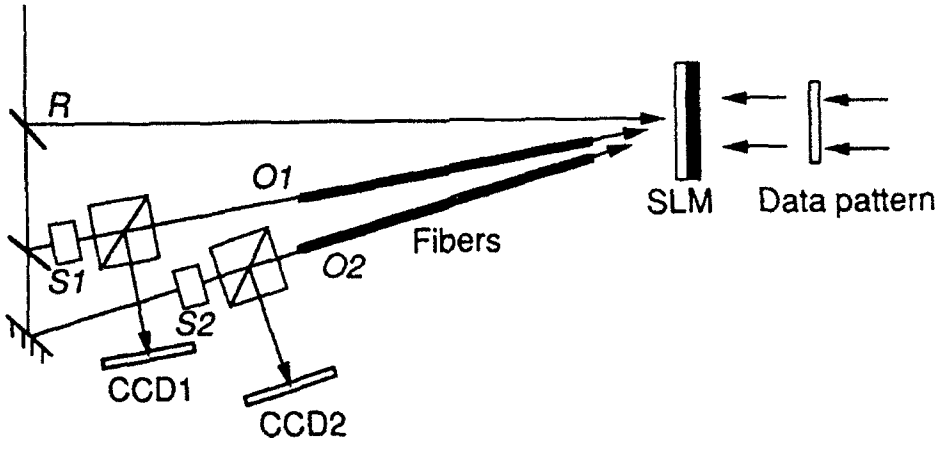


Fig. 3 Experimental setup for switchable parallel access.

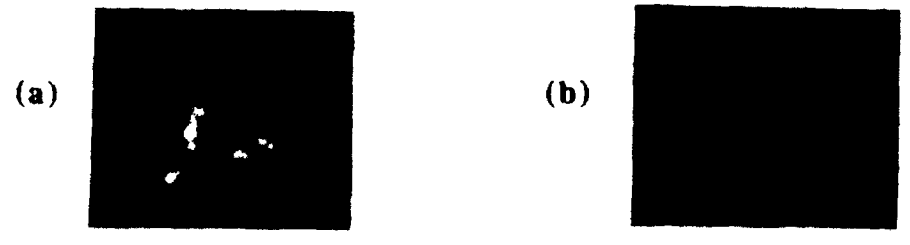


Fig. 4 Image pattern "A" readout through each fiber. (a) S1 on; S2 off, (b) S1 off; S2 on.

Wednesday

August 12, 1992

WA: Neural Networks

WB: Modulators

WA1 OPTICAL NEURAL NETWORKS UTILIZING SMART PIXELS

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1. Introduction

Optical neural networks[1] are quite attractive because of their direct image processing, dense-interconnectivity, and parallel-processing capabilities. However, there was a problem that a suitable analogue spatial light modulators (SLM) as the synaptic device had not been developed. In order to solve this problem, we have reported a smart SLM called a variable-sensitivity photodiode (VSPD) that has the multiple functions of photodiode, analogue SLM, and analogue memory[2] . In this paper, several optical neurodevices[3-5] using the 2-D VSPD arrays are reported, as well as the characteristics of the VSPD.

2. Variable Sensitivity Photodiode[2]

A MSM (Metal-Semiconductor-Metal)-VSPD , which is monolithically integrated with a LED on a GaAs substrate, is shown in Fig. 1. The operation principle is that the photocurrent is varied by the electric field across the electrodes. The VSPD is useful for the optical neurodevices in the following points: (1) The photocurrent monotonously increases with the bias voltage applied to the electrodes. Supposing that the synaptic weight corresponds to the sensitivity, the analogue weight essential to the neural networks is achieved. (2) The relation between the photocurrent and the voltage is symmetric around 0. This property permits to implement both excitatory and inhibitory synapses in one VSPD device. (3) The structure is very simple, so it is suitable for a 2-D and/or 3-D integration. (4) The VSPD works as an analogue memory as well as a variable sensitivity photodiode. The principle is based on the optical properties of impurities in the GaAs film. This feature is useful because no external memory is required for storing the knowledge.

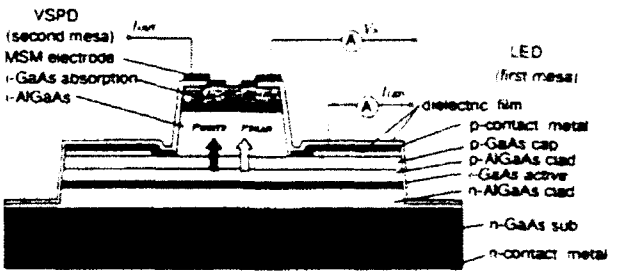


Fig. 1 Variable sensitbity photodiode.

3. Optical Learning Chip with Analogue Memory[3]

The functions of the fabricated optical learning chip are to acquire the knowledge and to store it as the synaptic weights in the VSPD array at learning phase, and to perform the vector-matrix multiplication at retrieval phase. All the processing is done in analogue values. The chip consisting of a 32 $\times$32 array of LED, VSPD pairs was developed. As shown in Fig. 2 the VSPD array is monolithically integrated with the LED array in a layered structure. The chip size is 6 $\times$6 mm^2. The experiments of the pattern classification with 14 traning signals were successfully performed using the BP model. The processing speed was about 10 GCPS. The storing time of the memory was about 30 min.

4. Optical Neurochips for Direct Image Processing[4, 5]

Two kinds of optical neurochips for image processing are introduced. In these devices, the input image is projected on the neurochip consisting of the 2-D VSPD array as the synaptic matrix. The neurochip performs the vector-matrix multiplication, where the vector is an electric control signal for the function selection. The output vector is the low-dimensional signal compressed in information quantity.

Fig. 3 shows an optical associative memory[4] where the output signal is fedback to the input after threshholding. A randomly-selected voltage pattern is used as an initial control signal. To enhance the image separation, an optical filter was attached on the VSPD array. Its transmittance is determined by learning based on the simulated annealing. Three images can be successfully recognized with a 8×8 VSPD array. Fig. 4 shows an artificial retina with the function of edge detection[5]. In this case, the electric control signal is chosen so that the function of the lateral inhibition is achieved. We have succeeded in the experiment using a 64 ×64 VSPD array chip.

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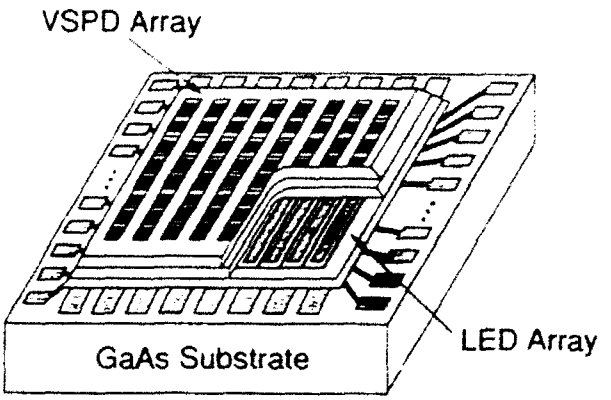


Fig. 2 Optical learning chip with analogue memory.

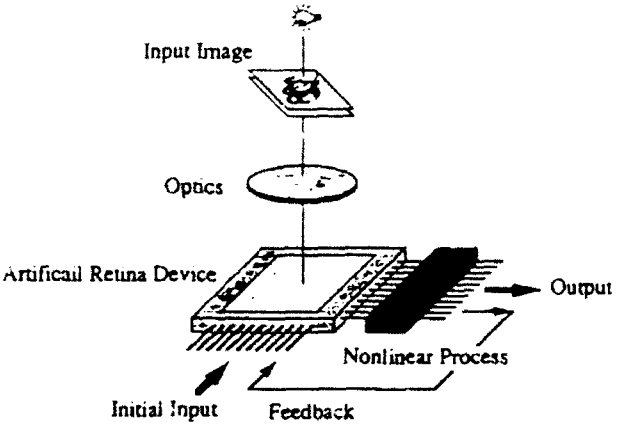


Fig. 3 Optical associative neurochip.

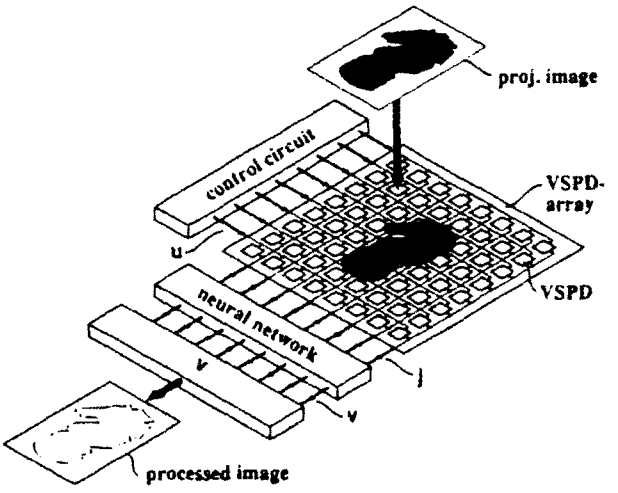


Fig. 4 Artificial retina for edge detection.

WA2

OPTOELECTRONIC CHIP FOR THE IMPLEMENTATION OF BACK ERROR PROPAGATION

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We present a CMOS silicon chip that optically implements the back error propagation (BEP) algorithm [1] of a two layer neural network. The chip has eight units (or "neurons") on a area of approximately 2×2 mm. Each unit consists of a phototransistor as the detector, a modulator pad for light modulation, sample-and-hold circuits, and additional circuits necessary to perform the BEP algorithm.

The modulator pad is an exposed metal layer on which voltage may be applied. Liquid crystal is added on top of the chip and covered with a glass plate coated with a transparent conducting film. Light is modulated by applying voltage between the modulator pad and the transparent conductor which changes the polarization of the reflected light (Figure 1) [2,3].

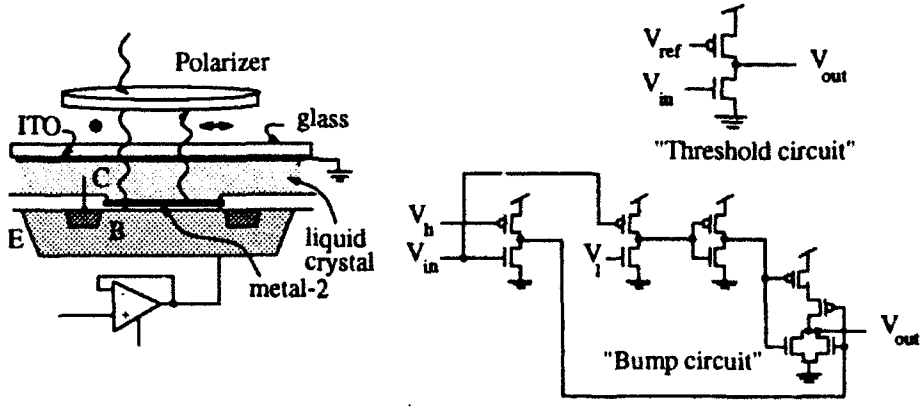


Figure 1. The liquid crystal modulator pad and threshold and bump circuits .

Phototransistors are fabricated directly under the modulator pads that have small openings in order to let light pass through. Two functions are needed to implement the BEP algorithm. These are thresholding in the forward direction and a bump function in the backward direction [1]. The schematic of the circuits that perform these functions are shown in Figure 1. The circuit can be electronically switched between the forward and backward modes. Figure 2(a) shows the measured pad-voltage versus input signal for both the forward and backward responses. Figure 2(b) shows the measured light reflectivity versus pad-voltage. The contrast obtained with this device is about 4:1. Experimental demonstration of the training of a simple network using this chip will be presented at the conference.

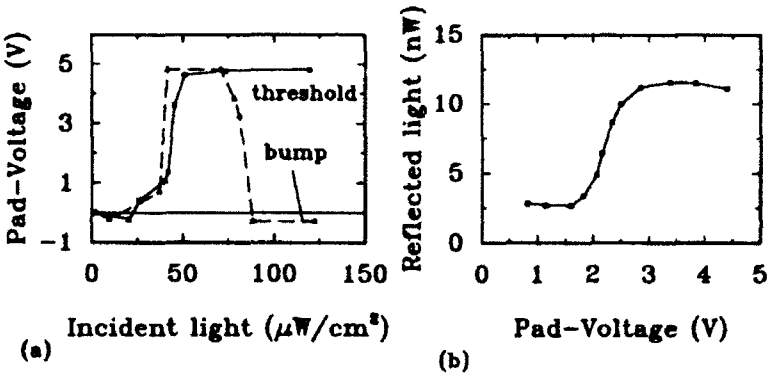


Figure 2. (a) Pad-voltage vs. input signal. (b) Reflected light vs. pad-voltage.

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WA3

HOLOGRAPHIC FAN-OUT OF MQW MODULATORS IN AN OPTOELECTRONIC NEURAL NETWORK

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Many potential applications for neural processors, such as real-time image processing and high-speed control systems, will require both parallelism and speed. Fast transducers will be needed that do not limit the performance of the constituent processors, together with optical techniques capable of providing a complex network of wide bandwidth interconnections. The use of optical fan-out has enable us to significantly improve on the size of our earlier neural networks.[1]

Multiple-quantum-well (MQW) modulators have ideal properties as output transducers: they can operate at over 1 Gbit/s, require negligible electrical drive power and two-dimensional arrays are readily fabricated.[2] We have fabricated arrays of up to 64 independently connected transmission modulators in InGaAs/InP for operation at 1.5 μm. Parallel interconnections can be formed with spatial optics, employing computer-generated holograms to replicate optical images and thus provide fan-out. A technique for the design of holograms has been developed that allows an arbitrary choice of positions and relative intensities for the output images.[3] Fourier-plane holograms were used in the system described here, but Fresnel devices incorporating the functions of the collimating and focussing lenses have also been fabricated, and these will lead to more compact systems.

The inputs to the neural network were connected to individual devices in a modulator array. The array was illuminated by splitting the collimated output of a DFB laser with a hologram and focussing the resulting array of spots onto the modulators. The modulator outputs were then replicated onto the weight-matrix plane by a second hologram (Figs. 1 & 2). Four copies were made for each output with relative intensities of 1: 2: 4: 8, so that 16 weight levels could be set with a binary mask. The image on the weight-matrix plane was demagnified by a lens to fall onto eight of the detectors in 4×4 array of large-area InP photodiodes. The output signals were amplified and connected to comparators to generate the neuron outputs. The network was configured in such a way that, with minimal overhead (one extra output and two extra inputs), the network could perform general functions requiring bipolar weight values although operating with unipolar optical quantities. With this configuration, the network's behaviour also became independent of modulator and weight-mask contrast and input power level.

An example of the operation of the network with 16 inputs and eight outputs at 8.448 Mbit/s is shown in Fig. 3. For this experiment, the network was configured as a two-layer perceptron by feeding back the first layer outputs to spare inputs and setting inter-layer weight values to zero. The network has now been rebuilt with a 64-input modulator array and results will be presented at the conference.

The practical implementation of optoelectronic neural networks is also being addressed. Modulator arrays have been flip-chip bonded onto glass substrates that have an electrical circuit printed on one face and a Fresnel hologram on the other. Such substrates will serve both as media for optical propagation and also as supports for the electronic circuits, their optoelectronic transducers and the optical components forming the interconnections. Architectures employing these techniques will take systems of the type described in this paper beyond demonstrations on optical tables towards practical implementation.

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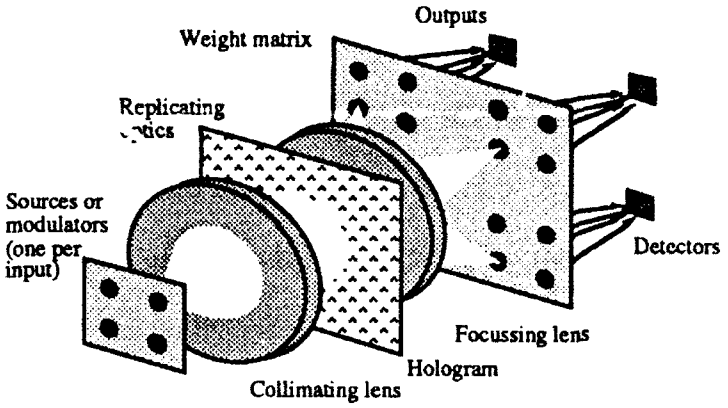


Fig. 1. Optical architecture. Fan-out by replication of the input array onto the weight matrix with a hologram. Fan-in by reduction of replicated image onto a detector array with a lens (not shown). Only four inputs and outputs shown here for clarity. The experimental system has 8 outputs and 16 or 64 inputs.

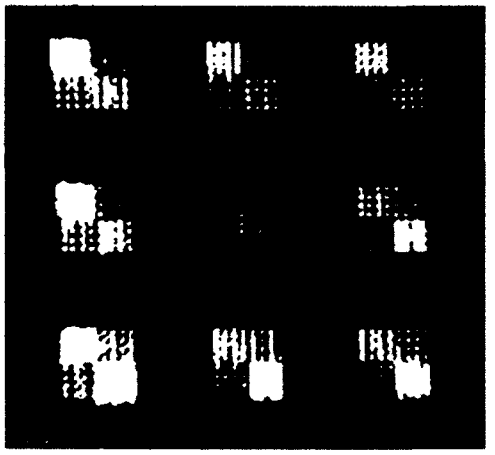


Fig. 2. 16-input array replicated to fan-out to 8 outputs. For each output, 4 copies were made with relative intensities of 1: 2: 4: 8, enabling 16 weight levels to be defined with a binary mask.

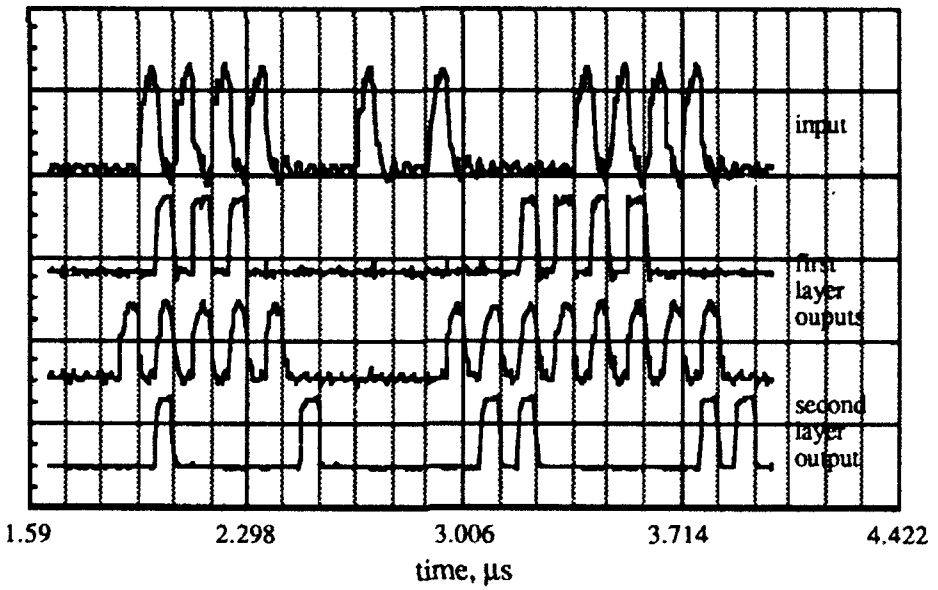


Fig. 3. The 16-input × 8-output network configured as a two-layer perceptron performing a parity check on six of its inputs at 8.448 Mbit/s. Six successive bits from the input signal were presented in parallel to the network by a shift register. The final layer output was true whenever three out of the six input bits were true. Note that there was approximately a 1-bit delay for each layer.

WA4 VLSI/LIQUID CRYSTAL WINNER-TAKE-ALL MODULATORS FOR OPTICAL COMPETITIVE LEARNING

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A winner-take-all (WTA) function is a vector function which evaluates an array of analog inputs to determine which is the largest. Its output is a vector of binary values which are false for all elements but the one that corresponds to the largest input. Essentially all unsupervised learning systems require some form of WTA function for their neuron activations. An optical winner-take-all device which chooses the largest of an array of light intensities would be useful for optical implementations of adaptive resonance and competitive learning systems[1, 2]. This paper discusses an optical WTA device implemented with VLSI/liquid crystal technology, and its use in an optical competitive learning system.

Figure 1 shows a block diagram of an optical competitive learning system that uses a VLSI/liquid crystal winner-take-all modulator. A set of input patterns are applied one at a time to the input SLM. Some of the input light is diffracted by the volume hologram towards the array of LC/VLSI reflective modulators. The modulators are positioned in a fractal pattern which prevents crosstalk through the volume hologram by eliminating Bragg degeneracy. The winner-take-all competition circuit causes the pixel in each competitive patch which is receiving the largest input to switch the liquid crystal above that pixel to reflect the light back through the polarizer, which also blocks light from the losing units. Meanwhile, the undiffracted light that has passed through the volume hologram is reflected by the phase conjugate mirror. The phase conjugate wave interferes with the reflections from the winning pixels in the volume of the photorefractive crystal, strengthening the interconnections between the input pattern and each of the winning pixels. Thus, the optical system implements the competitive learning algorithm, with individual units in the competitive arrays becoming tuned to different clusters of inputs.

Figure 2 shows a schematic cross section of two units in a one-dimensional VLSI/Liquid Crystal WTA array. The VLSI/LC devices are made by flowing a layer of liquid crystals between an integrated circuit (IC) die and a cover glass which is coated with a transparent conductor and an alignment layer. Polarized light passes through the glass and liquid crystal layers and strikes the electrode mirror on the surface of the IC. Light which is not reflected by the metallic electrode is absorbed by a photodetector under the electrode and is converted to a current. This current is input to a competitive circuit[3] which selects the largest of the inputs to all of the units through non-specific global inhibition. The output of the competition circuit is then thresholded and buffered to drive the modulator electrode. The molecules in the liquid crystal layer are oriented by the electric field between the chip and cover glass electrodes to maintain or rotate the polarization of the reflected light.

Figure 3 shows the LC modulator electrode voltage for two units of an eight-unit WTA circuit as the ratio of optical inputs to the units is varied. The light from an LED array is demagnified onto the chip so that each LED is imaged onto a single WTA unit. To produce the data in Fig. 3, units 3–8 received an intensity of $3.7\mu W/cm^2$, unit 2 was set to $11.4\mu W/cm^2$, and unit 1 was varied around unit 2's input value. The 0–5V output voltages generated by the WTA circuit are sufficient to switch the LC mixtures used in current VLSI/FLC devices.

Figures 4(a) and 4(b) are polarizing microscope photographs of a different one-dimensional array demonstrating winner-take-all behavior. In Fig. 4(a), the array is illuminated with uniform light from the microscope's incandescent illuminator. The leftmost unit in the array "wins" in this case because end units receive more photocurrent from the surrounding substrate. Fig. 4(b) shows the result of illuminating the array with an additional stripe of light about one pixel ($50\mu m$) wide. The unit that is illuminated by the stripe switches on, and the unit on the left side is switched off by the electronic competitive circuitry.

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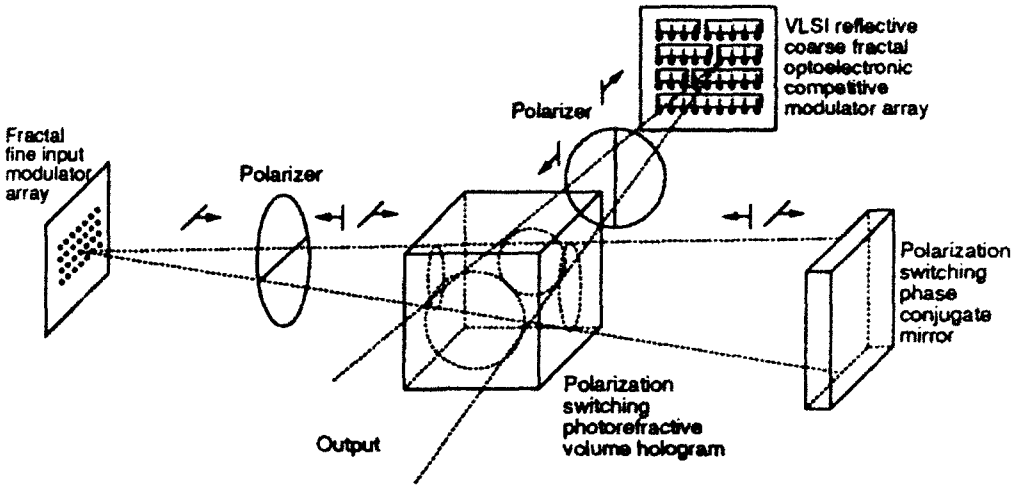


Figure 1: Optical competitive learning system architecture.

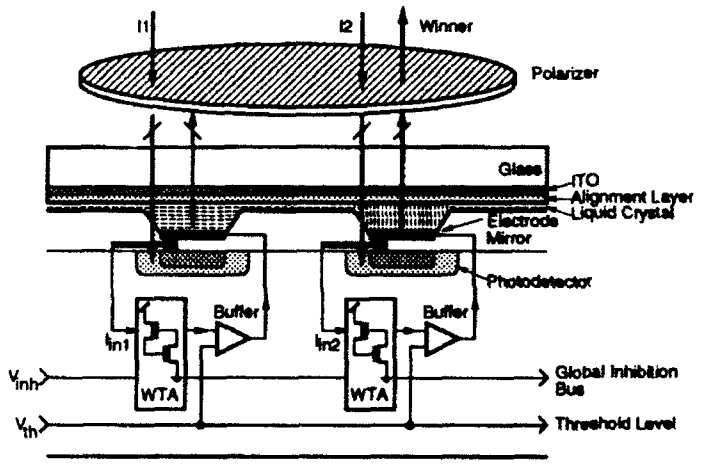


Figure 2: Cross-sectional diagram of two units of a VLSI/LC winner-take-all device.

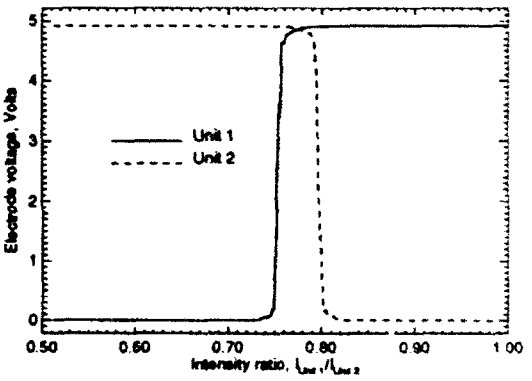
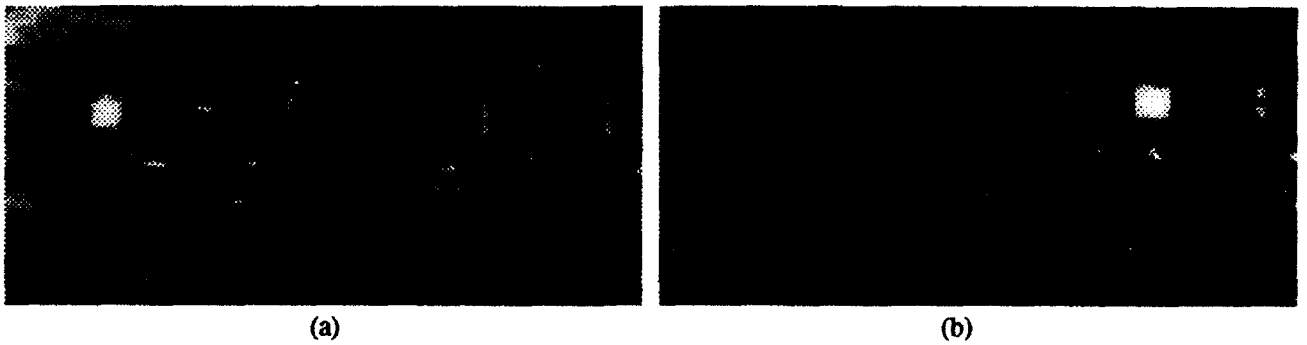


Figure 3: Modulator electrode voltage as the ratio of input intensity is varied on two units of an eight-unit array.



(a) (b)

Figure 4: Photomicrographs of a one-dimensional array showing winner-take-all behavior. (a) Array under uniform illumination; (b) Array with additional illumination on fifth unit.

WB1 RECENT DEVELOPMENTS ON Si/PLZT SMART PIXELS TECHNOLOGIES

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ABSTRACT

Si/PLZT smart pixels technology is critical for optoelectronic computing applications requiring large fan-out (~ 1000) and high-speeds (~ 100MHz). The advances made towards the realization of devices based on this technology will be reviewed.

1. Introduction

It is now widely recognized that free-space optical interconnects can be effectively used for implementing fast parallel computing and communication switching systems only if high speed Smart Pixel Arrays can be brought to the realm of practice. In general, the realization of Smart Pixels requires the intimate coupling of devices and materials with widely different characteristics for the integration of very large scale electronic circuits, with light detectors as inputs and light transmitters as outputs. The output light transmitters can be light sources or light modulators if high density I/O with minimum on-chip power dissipation is required. At UCSD, various device and material integration technologies bringing together logic circuits and light detectors on silicon with light modulators on Lead Lanthanum Zirconate Titanate (PLZT) (for phase modulation), and on III-V Multiple Quantum Wells (MQW) (for absorption modulation) have been investigated towards the realization of Smart Pixels. Although the choice of silicon can be easily understood in terms of the superior characteristics of this material for integrated circuit implementation, the choice of PLZT that possesses a large dielectric constant ($\varepsilon_r = 4700$) as the light modulator material in the 90's is more subtle and merits more discussions. This is especially important when one considers the small dielectric constant ($\varepsilon_r = 13$) of MQW materials. The small dielectric constant of MQW materials result in light modulators with lower switching energies (~ 10 fJ/μm^2) enabling them to be electrically driven at high speeds even when they are densely integrated. The shortcoming of MQW modulators is their small dynamic range and low fan-out related to their absorptive nature. On the other hand, using light modulators with a transverse geometry, one can significantly reduce the disadvantages of PLZT in terms of switching energy and take advantage of its large Kerr electro-optic coefficients and its low absorption. In the following, we will analyze the merits of PLZT for light modulation with respect to MQW materials taking into consideration the technological advances made in the integration technologies for Si/PLZT Smart Pixels.

2. Si/PLZT Smart Pixels Integration and Application Potentials

Over the past years, several technologies for hybrid as well as monolithic integration of silicon and PLZT have been investigated extensively at UCSD. These are based on flip-chip bonding of silicon and PLZT chips [1,2], laser recrystallization of silicon on PLZT[3] and thin film deposition of PLZT on silicon-on-sapphire.[4]

2.1 Flip-chip bonded Si/PLZT Smart Pixels

Flip-chip bonding is a mature and well-developed technique widely used in the silicon industry for multi-chip module assembly. It has lately emerged as a practical approach for the integration of devices of dissimilar materials. In the past, we have reported one-dimensional Si/PLZT spatial light modulator arrays that were fabricated by flip-chip bonding an array of light modulators on a PLZT chip with silicon phototransistors on a silicon chip.[1] More recently, we have been working on a Si/PLZT smart pixels module shown in Fig.1 where several silcon chips with pre-fabricated integrated circuits are flip-chip bonded using indium bumps on a PLZT wafer that supports the light modulators.[2]

Presently, the flip-chip bonding technique exhibits a bond capacitance of ~0.1pF/bond and does not limit the performance of light modulators (with 100 μm^2 aperture) with a capacitance of ~0.5pF fabricated on ceramic bulk PLZT wafers. It should be noted that with present indium bump technology, the capacitance of flip-chip bonded MQW modulators of similar dimensions would be governed by this bonding capacitance reducing significantly the energy advantage of these modulators. However, due to the larger half-wave voltage of the reflective bulk PLZT modulators (35V), asymmetric Fabry-Perot MQW modulators flip-chip-bonded to silicon chips can still offer a considerable advantage in terms of switching energy.

Recently, we have started investigating Self-Tuned Fabry-Perot modulator structures that should enable us to reduce the required modulation voltage of bulk PLZT modulators by at least a factor of five. A general Fabry-Perot etalon consists of a spacer material with high reflectance coatings on both sides. Constructive interference occurs at the output of the etalon when the incident light satisfies

$$m\lambda = 2nd\cos(\phi) + \delta_1 + \delta_2 \qquad (2\text{-}1)$$

where m is an integer, l is the wavelength, n is the index of the spacer, d is the thickness of the spacer, f is the incident angle d_1 and d_2 are the phase changes of each reflective coating. In a typical Fabry-Perot modulator, m, l, d, f, d_1 and d_2 are held constant and by the application of the electric field the index n is varied producing constructive or destructive interference at the output. A problem with this structure is that for a given wavelength the output intensity of each etalon in an array will vary significantly if the optical thickness nd is not uniform over the array. The precision with which this thickness must be controlled is very high and difficult to achieve for a large array of Fabry-Perot modulators in Smart Pixels. The self tuned Fabry-Perot structure that we are investigating uses an optically recorded volume hologram as one of the high reflection coatings. The hologram is recorded in place using the interference between the modulator illumination and the reflected output. The phase angle of the resulting hologram automatically compensates for the optical thickness variations. At each x,y point on the etalon array, the hologram's reflection phase, $d_1(x,y)$ will compensate for the change in substrate thickness:

$$\delta_1(x,y) = 2n(x,y)d(x,y)\cos(\phi) + \delta_{arb} \qquad (2.2)$$

where d_{arb} is an arbitrary constant phase. Note that the hologram also inherently compensates for index variations and changes in the incident angle due to thickness variations. Figure 1 shows the STFP structure when used with flip-chip bonded Si/PLZT smart pixels. Note that rewritable holographic materials offer the possibility of optically addressed tunable devices that will compensate for the wavelength shifts in the laser wavelengths used to power-up the modulators. This technique can also be applied to a large variety of materials and device structures.

While the use of STFP structures can reduce significantly the required modulation voltage, flip-chip bonded Si/PLZT smart pixels, due to their large parasitic capacitances, can be used only in systems operating at medium I/O data rates requiring low transmitter densities (one per mm^2) and large transmitter fan-out (1000). A typical system exhibiting these characteristics is, for example, UCSD's D-STOP neural network system[5] that will be operated with a system clock speed of 10MHz.

2.2. Si/PLZT Smart Pixels Fabricated by Laser Crystallization of Polysilicon

Originally in an attempt to reduce the bond capacitance we had investigated an alternative technique to integrate silicon and PLZT materials, that of laser recrystallization of silicon on PLZT[3]. In this technique, a thin film of polysilicon is deposited on PLZT and then recrystallized with a scanning beam to make it a single crystal where small electronic circuits can be fabricated. Several smart pixel arrays using CMOS integrated circuits on silicon on PLZT were fabricated and tested successfully with this technology. Unfortunately, this technology utilizes unconventional low temperature silicon processing making it expensive to manufacture, without providing any significant performance advantage over flip-chip bonding. It is important to note that before selecting a smart pixel integration technique, it is imperative to fully understand the characteristics of the light modulators that will be employed and efforts should be made to minimize the changes that are required in the silicon processing.

2.3. Si/PLZT Smart Pixels based on Deposited Thin Film PLZT

As pointed out earlier, bulk PLZT light modulators while offering large contrast ratio, suffer from large modulator capacitances (due to large material dielectric constants). To overcome this limitation we have been investigating thin film PLZT modulator structures. Thin film transverse modulators are attractive due to lower device capacitances as the thickness of the material is reduced. However, usage of thin films results in reduced optical interaction lengths and increased operating voltages. A solution to having low modulator drive voltages and modulator capacitance is using films placed between reflective layers in a Fabry-Perot configuration as discussed earlier. The reflective layers increase the optical path of the modulated light and reduce the operating voltage. Through simulation we have shown that for such a modulator operating with a spectral bandwidth of 10nm, it is possible to reduce the operating voltage to less than 15V. Also, the capacitance of such a modulator can be reduced to about 50fF, roughly a factor of ten less than that of bulk PLZT modulators. This corresponds to a required electrical switching energy of 5pJ, a factor of fifty less then the present reflective bulk PLZT modulators.and only slightly more than MQW modulators.

In order to implement Smart Pixels using PLZT thin films, we have investigated the growth conditions of PLZT by magnetron sputtering on various substrates such as silicon GaAs, sapphire, and platinum on sapphire. Although, in our experiments we were unable to grow high quality PLZT films directly on silicon, we have been capable of obtaining very high quality films on the remaining substrates as reported in [4]. These material deposition/growth results open new avenues for Si/PLZT based smart pixels possibly making them attractive for very high speed (> 100Mhz) applications requiring high I/O density (>10 /mm^2).

Two choices exist for Smart Pixels implementation using PLZT thin films. The first one, is based on depositing first platinum followed by thin film PLZT in windows opened in silicon on sapphire. The silicon circuits are fabricated prior to the Pt/PLZT growth using standard SOS fabrication process. Pt is used as one of the reflective mirrors of the Fabry-Perot structure. The top mirror can be a dielectric coating or a thick hologram to implement an STFP structure as discussed in section 2.1. This technology departs however from main-stream bulk silicon technology and uses high cost sapphire wafers as support substrate. It benefits however from low parasitics, a transparent host substrate and offers

the potential for monolithic high performance smart pixels.

An alternative approach using thin film PLZT modulators is based on epitaxial lift-off and direct bonding of thin films. Yablonovitch[6] has shown that GaAs grown on AlAs can be readily lifted-off because of the large etching selectivity of these two materials to a diluted HF solution. This also means that materials that are deposited or grown on GaAs can be lifted-off with an underlying layer of AlAs if they satisfy certain critical conditions including resistance to the diluted HF etching solution. In our context, the main advantage of the lift-off technique is that it allows thin film PLZT to be grown on a "lattice matched" substrate, such as GaAs, and later transferred to arbitrary substrates, including silicon processed wafers. This allows the direct bonding of thin film PLZT on dielectric mirrors deposited on substrates such as silicon. This provides significant flexibility in the implementation of Fabry-Perot etalons and enables significant cost reduction associated with electronic circuit fabrication and support substrate.

3. Conclusions

In this paper, we have reviewed the status of Si/PLZT integration technologies and discuss some of their benefits. It is our strong belief that with novel techniques such as the STFP structures and the epitaxial lift-off of PLZT thin films it is possible to bring the Si/PLZT smart pixels to the realm of practice where they can be competitively used towards the realization of free-space interconnected computing and communication systems.

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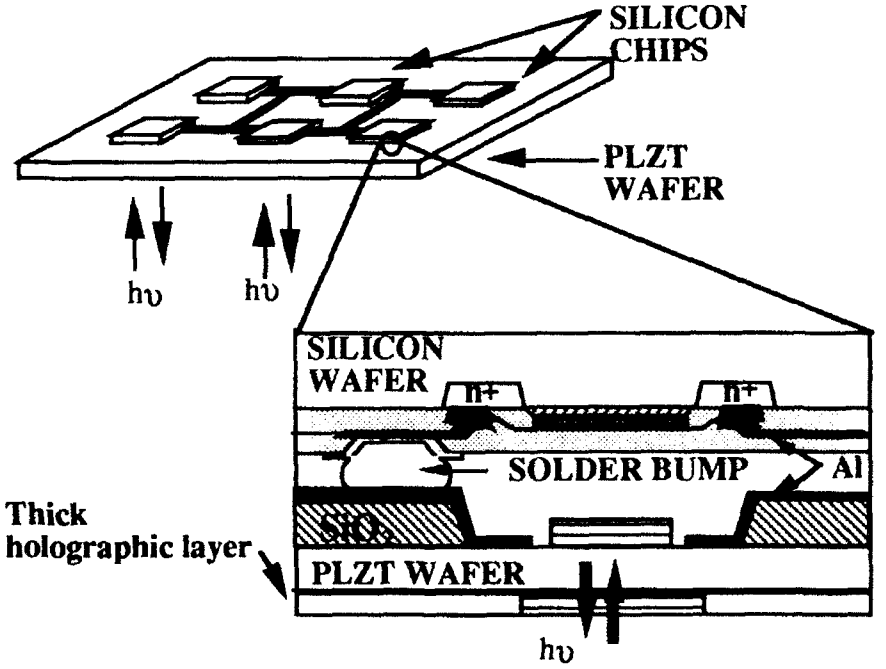


Fig.1: Si/PLZT smart pixel module realized by flip-chip bonding using indium bumps.

WB2 HIGH-SPEED DESIGN OF ASYMMETRIC FABRY-PEROT MODULATORS

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Summary—Because of their low insertion loss, high contrast ratio, and low voltage swing, as well as their surface-normal configuration and polarization independence, asymmetric multiple-quantum-well (MQW) Fabry-Perot modulators (AFPMs) have attracted a great deal of attention as possible elements of smart-pixel arrays. In particular, since electrical bandwidths in excess of 20 GHz have been demonstrated,[1] the AFPM should prove an attractive option for high-speed optical switching applications. Several authors have addressed the complexities of designing AFPMs for optimal DC performance;[2,3,4,5] here we extend the list of design criteria to encompass the modulation speed of the device, as well as its contrast ratio, insertion loss, and operating voltage swing.

The asymmetric Fabry-Perot modulator consists of a MQW *p-i-n* diode sandwiched between mismatched quarter-wave stack mirrors (see Fig. 1). In the zero-bias, low-absorption state, the reflectivity is high (typically > 50%). Applying an electric field across the *p-i-n* diode increases the cavity absorption via the quantum-confined Stark effect, effectively decreasing the back mirror reflectivity to balance that of the front mirror and null out the reflected signal. The device design parameters include the front mirror reflectivity, the number of quantum wells, the quantum well and barrier thicknesses and compositions, thickness of the contact regions, operating voltage swing and the operating wavelength. Since the quantum-confined Stark effect is inherently an almost instantaneous process, the modulation speed is practically limited only by the speed with which the field applied across the MQW region can be modulated.[6]

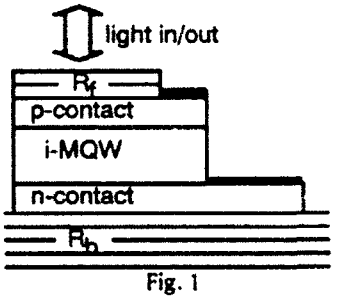


Fig. 1

We will restrict our consideration of the high-speed performance of AFPMs to the situation in which the space charge built up in the quantum wells is insufficient to impact negatively the device performance, either by saturating the exciton or by reducing the effective voltage applied across the MQW region. This amounts to limiting the peak incident optical intensity to relatively low levels (less than, perhaps, 1 kW/cm^2 or ≈0.15 mW on a 10 μm-diameter device). Subject to this constraint, the device's speed is limited only by the *RC* time constant associated with the diode capacitance and series resistance, and the system impedance and parasitic capacitances, and not by any transit-time considerations, as it would be in a photodetector. We can ignore, then, for this analysis, the problems of carrier trapping in and escape from the quantum wells which become important at higher optical powers.[7]

To design a high-speed AFPM, we begin by calculating the absorption–thickness products $(\alpha l_w)_{on}$ and $(\alpha l_w)_{off}$ required in order to give the desired on- and off-state reflectivities (or, equivalently, the desired insertion loss and contrast ratio). The reflectivity at resonance is given by

$$R_o = R_f\left(1-\frac{R_a}{R_f}\right)^2(1-R_a)^2,\ R_a = \sqrt{R_f R_b}\,e^{-\alpha l_w}$$

where R_f is the front mirror reflectivity and R_b the back mirror reflectivity. It is useful to consider the ratio of $(\alpha l_w)_{off}$ to $(\alpha l_w)_{on}$, since in general the more demanding the device design parameters, the higher this ratio will have to be. We can derive experimental values of this absorption ratio from measured electroabsorption curves (Fig. 2). The most efficient designs will then correspond to the peaks in the absorption-ratio curves, or the points of maximum absorption ratio for a given field change ΔE and DC bias. From a plot of this maximum absorption ratio versus the corresponding α_{off} for various values of ΔE we can find the combined thickness of quantum wells l_w, which, for a given ΔE, yields the required $(\alpha l_w)_{off}$ and $(\alpha l_w)_{on}$. The total thickness of the MQW intrinsic region is then $l_{MQW} = l_w + l_b$ (where l_b is the combined thickness of the quantum well barriers), and the operating voltage swing required is $\Delta V = l_{MQW}\Delta E$.

A plot of l_{MQW} versus ΔV (Fig. 3a) derived from electroabsorption data for a certain MQW structure (e.g. the 100Å GaAs well/ 45Å $Al_{0.3}Ga_{0.7}As$ barrier material of Fig. 2) constitutes a general design constraint which an AFPM design employing that MQW material must satisfy in order to give the desired contrast and insertion loss. From this curve, then, given the physical structure of the modulator (i.e. its area A, series resistance R_s, and associated pad capacitance C_{pad}), we can plot the predicted electrical bandwidth of the device (Fig. 3b):

$$f_{3dB} = \left[2\pi\left(R_s + Z_o\left(\frac{\varepsilon A}{l_{MQW}}\right) + Z_o C_{pad}\right)\right]^{-1}$$

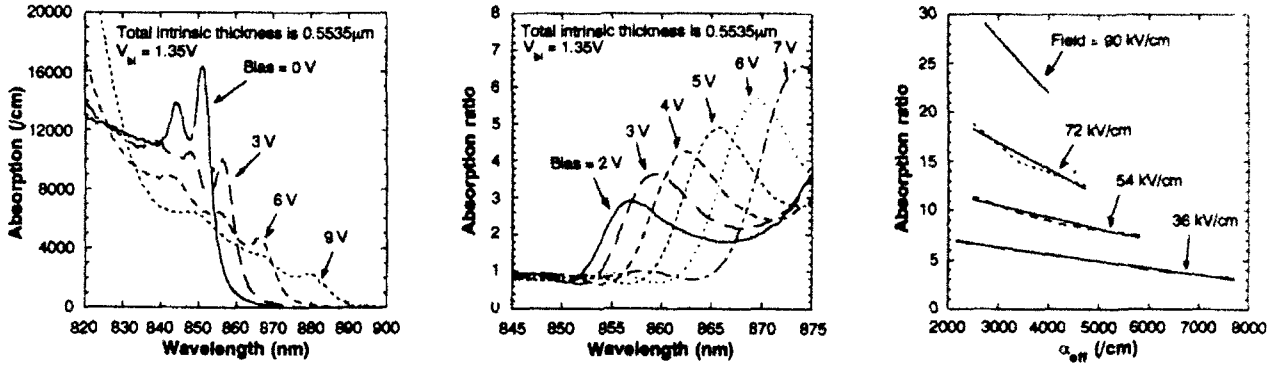


Fig. 2. a) Electroabsorption derived from photocurrent spectroscopy of 100Å GaAs QWs with 45Å $Al_{0.3}Ga_{0.7}As$ barriers. b) Maximum absorption ratios vs. wavelength for 36 kV/cm^2 field change across the structure measured in a) at various DC biases. c) Maximum absorption ratios and the corresponding values of α_{off} for the same structure. Solid curves are linear curve fits.

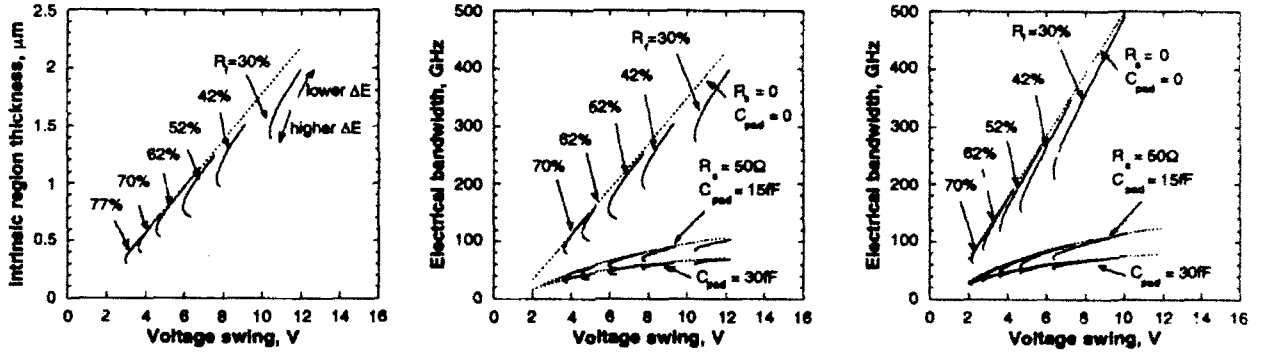


Fig. 3. a) Intrinsic (MQW) layer thickness versus voltage swing for an AFPM layer structure designed to give 20dB contrast and 1.5dB insertion loss using the MQW material in Fig. 2 with various numbers of front quarter-wave-stack periods. The dotted line shows that the most efficient designs (those for lower ΔE, longer λ, and higher bias) fall on a straight line. b) Electrical bandwidth of a 10 μm x 14 μm diode with the same layer structure as in a), and various values of R_s and C_{pad}. c) Electrical bandwidth for a 10 μm x 14 μm diode designed to give 15dB contrast with 2dB insertion loss. Note that higher speeds can be achieved for the same voltage swing if more insertion loss or lower contrast can be tolerated.

As these plots demonstrate, asymmetric Fabry-Perot modulators do indeed offer high speed, as well as the winning combination of high contrast, low insertion loss, and low operating voltage swings which would be required for high-speed optical switching arrays. Current devices, such as our recent 21 GHz device[1], are limited by series resistance and pad capacitance; engineering the diode's contacts and the pad design should yield substantial speed improvements for essentially the same modulator structure. Further, design curves such as these facilitate optimizing the material structure itself for high-speed operation.

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WB3

DIFFERENTIAL SELF-LINEARIZED SEEDs: NOVEL ANALOG SMART PIXELS

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Quantum well self-electrooptic-effect devices (SEEDs) [1] have been extensively investigated for digital systems. The symmetric SEED (S-SEED) [2] has been particularly useful for systems experiments, in part because of many features of operating with differential pairs of light beams. Here we propose new analog SEED circuits that also operate with differential pairs of light beams, and that in many cases can be made using the same technology as has been used successfully to make large arrays of S-SEEDs. The use of differential pairs of beams allows both positive and negative analog values to be represented. The flexibility of the SEED fabrication process allows many different sophisticated analog functions to be performed, including addition, subtraction, and differentiation of images, correlation, and optically controlled bipolar matrix-vector multiplication (e.g., for optical neural nets). The use of SEED technology should allow large arrays of high-speed devices.

Unlike the bistable, positive-feedback switching mode of SEED operation, these devices are based on negative feedback. This mode occurs when the optical absorption increases with increasing reverse bias on a quantum well diode, as happens for photon energies just below the optical bandgap energy. It has been investigated before for "single-ended" devices (i.e., devices designed to modulate one light beam) [3]. One feature of this mode is that it can make a "self-linearized" modulator. When a quantum well diode is driven (in reverse bias) from a current source in this mode, the voltage across the diode adjusts itself so that the generated photocurrent exactly equals the drive current. Since we typically get one electron of photocurrent for every absorbed photon in such diodes, the result is that the absorbed power is linearly proportional to the bias current. One simple way of making a current source is to reverse bias a conventional photodiode, which will typically give a current proportional to the control light power shining on it, independent of voltage over a usable range. This allows optically controlled linear optical modulation.

The present class of devices is based on the extension of the self-linearized modulator to pairs of conventional diodes and pairs of quantum well diodes. The basic circuit is shown in Fig. 1.

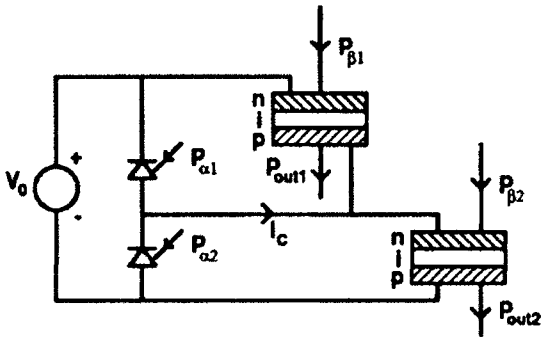


Fig. 1. Self-linearized differential modulator.

In Fig. 1, a current I_C flows out of the center point of the two conventional input photodiodes. This current is simply proportional to the *difference* in the absorbed powers in the two diodes. If the power $P_{\alpha 1}$ is larger than the power $P_{\alpha 2}$, a net positive current flows out of the center point. By conservation of current, in the steady state the difference in the photocurrents in the two quantum well diodes must also equal I_C. Hence the difference in absorbed powers in the two quantum well diodes equals the difference in the incident powers on the two conventional diodes. If we use equal "power supply" beams $P_{\beta 1}$ and $P_{\beta 2}$, then the difference in the output powers P_{out1} and P_{out2} equals the difference in input powers $P_{\alpha 1}$ and $P_{\alpha 2}$. We could call this cir-

cuit a self-linearized differential modulator. It is also possible to make these circuits using only quantum well diodes, with some performance compromises and supply voltage changes.

This unusual circuit has several potential uses. We could, for example, use an array of such devices to find the difference between two images. For example, if $P_{\alpha 1}$ is a pixel from one image and $P_{\alpha 2}$ is from a second image, the output power difference will give the true difference between the incident images, with the absolute power level suppressed, and looking at any one set of output beams (e.g., $P_{out\,ij}$) will give the difference against a constant background.

The use of the differential pair of light beams allows us to represent both positive and negative values, such as the difference between two images. By shining two (or more) sets of input beam pairs on the input photodiodes, we can use this circuit to add or subtract such differential values (optically interchanging the beams in a pair will give subtraction, as will interchanging the wiring of the two photodiodes). Simple variations on this circuit allow conversion between "single-ended" and differential representations of images. The use of differential pairs also means that the overall variations of "power supply" beams over an array are not important, as long as adjacent beams are similar.

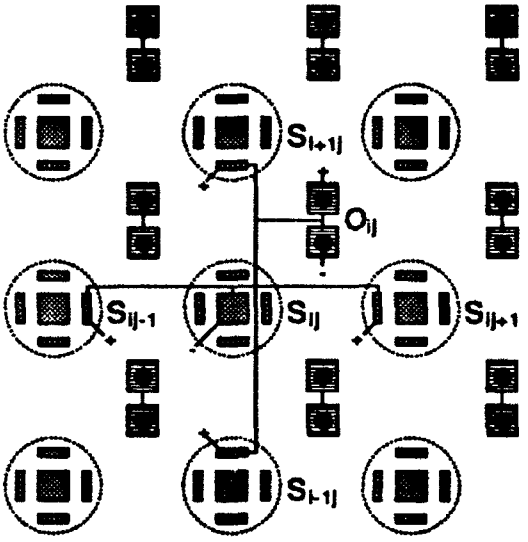


Fig. 2. Diode layout interleaving diodes from adjacent elements in an array for evaluating the Laplacian. The input image is shone onto the entire array through a mask with circular holes (dashed circles S_{ij}). The grey areas are the input conventional photodiodes, with areas chosen to give the necessary input weights for the Laplacian. The outputs are taken from the output quantum well diodes O_{ij}, shown with equal power beam (black circles) incident on them The electrical connections are shown onlyfor one set of diodes for clarity.

One potential application of such a circuit is to optical neural systems, where we can have both inhibitory and excitatory inputs to a neural node, and can use fully bipolar values and bipolar weights in the neural net. The output of the circuit also saturates in an approximately sigmoidal fashion, as desired for many neural nets, since there are limits to the minimum and maximum absorption of the quantum well diodes.An extension of this circuit also allows an optically controlled bipolar weight for neural nets or bipolar optical analog matrix multiplication. Hence we have techniques with this circuit for full arithmetic operations on bipolar values.

Another class of applications of this circuit is to evaluate spatial derivatives of images. The example in Fig. 2 gives an approximation to the Laplacian, as frequently used in early vision processing. The outputs are given for each point in the array as the differential beam pair from the quantum well diodes. A circuit such as that in Fig. 2 is actually a specific example of a convolution or correlation (in real space), and by the use of other diode layouts we can extend this to other applications such as pattern recognition.

In summary, with this class of proposed circuits, it should be possible to extend the use of SEED technology to sophisticated analog optical array processing functions.

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WB4 COMPARATIVE STUDY OF SMART PIXEL SCHEMES USING OPTOELECTRONIC OR S-SEED BASED LOGIC

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The recent interest in photonic switching technology has lead to rapid development of smart pixels which can perform multiple optical logic functions and can be potentially integrated into two-demensional arrays. Various schemes for realizing smart pixels have been proposed and actively pursued. However little work has been done in comparing the fundamental limitations that different approaches would impose on a photonic switching system.

Characteristics that can be used to determine the performance of a photonic switching system include bandwidth, power dissipation, pixel packing density, thermal stability, and overall efficiency. In a photonic switching system the essential process is the modulation of light which is the carrier of information. To modulate a light source, either direct current modulation or external (intensity) modulation can be employed. The former is represented by laser diode-based integrated optoelectronic circuits in which the output of the laser diode is directly modulated by current[1]. The latter uses external modulators to vary the intensity of input light. One of the most thoroughly investigated external modulators for these applications is self-electro-optic effect device (SEED)[2]. Since any logic function can be synthesized by using only NOR gates, we base our comparative study on two schematic optical NOR gates using a laser diode/HBT/detector circuit, or a symmetric SEED (S-SEED), as illustrated by Fig. 1 (a) and (b).

In Fig. 1 (a) the laser diode is biased above its threshold current without any light incident on either of the two p-i-n photodetectors so that the output of the laser diode is in the logical "1" state. When either or both of the p-i-n diodes are illuminated, the photocurrent drives the HBT from cutoff into saturation, so that the laser output will be switched off into the logical "0" state. The bandwidth of the logic gate is limited by the slower of the laser diode and the photoreceiver. The relaxation oscillation frequency f_r sets the upper limit to the laser's modulation response which is in the range of 10-20 GHz for InGaAaP lasers with 1.3-1.55 μm wavelength. On the receiver side, InGaAs/InP p-i-n photodiodes have demonstrated bandwidth of 10-40 GHz, and InGaAs/InP HBTs have achieved unity gain bandwidth of 165 GHz. We can resonably expect, therefore, that the bandwidth of laser-based optical logic gate can be as high as 1-10 GHz.

Optoelectronic gain is also required for an optical logic gate to compensate losses and achieve fanout. For laser-based NOR gates, gain is determined by the product of the differential quantum efficiency of the laser diode, the quantum efficiency of the p-i-n photodiode,

and the current gain of the HBT. The power dissipation of the NOR gate is determined by the threshold current of the laser diode and the current swing during switching. With a typical bias voltage of 5 V, and assuming a 1 mA laser threshold, power dissipation is about 8 mW to achieve a gain of 10. The temperature dependence of the threshold current will degrade the optoelectronic gain, and thus increase the instability of the logic gate.

For the S-SEED NOR gate shown in Fig. 1 (b), two p-i-n diodes connected in series and under reverse bias work as both detector and modulator[3]. The logical "1" is when the upper diode is more transmitting (or reflecting) than the lower diode, and the logical "0" state is the contrary. The S-SEED functioning as a NOR gate must be preset to the "0" state by initially illuminating the upper diode. During operation, outputs from previous stages will be incident on the S-SEED. The S-SEED will not switch from "0" to "1" unless both S-SEEDs in the previous stage are outputing "0".

The switching time of S-SEED is set by the the time it takes to charge the capacitance of the reverse biased p-i-n diodes. Detailed knowledge of responsivity of the SEED is required to evaluate its switching time. We used recently published measured responsivity data to calculate the switching time for several types of S-SEEDs including conventional, extremely shallow quantum well, and asymmetric Fabry-Perot cavity-based devices. The results show that with an optical power of 500 μW, the bandwidth of S-SEED logic gates is as high as 400 MHz, which is significantly lower than that of laser-based logic gates. The ultimate switching speed of the S-SEED is limited by saturation effects due to the finite carrier sweep-out time in the mutiple quantum well region of the diode. Also, the "time sequential gain" is limited by the saturation effect. On the other hand, the power dissipation of an S-SEED logic gate is one order of magnitude lower than that of the laser-based logic gate. The temperature dependence of band gap will make the contrast ratio of the S-SEED vulnerable to temperature fluctuations due to the narrow absorption peak of the quantum confined Stark effect (QCSE). This undesirable sensitivity is worsened when the Fabry-Perot structure is used.

These comparisons, along with ease of implementation, temperature and wavelength sensitivity, system noise performance, scalability and device geometry will all be quantitatively discussed in this paper.

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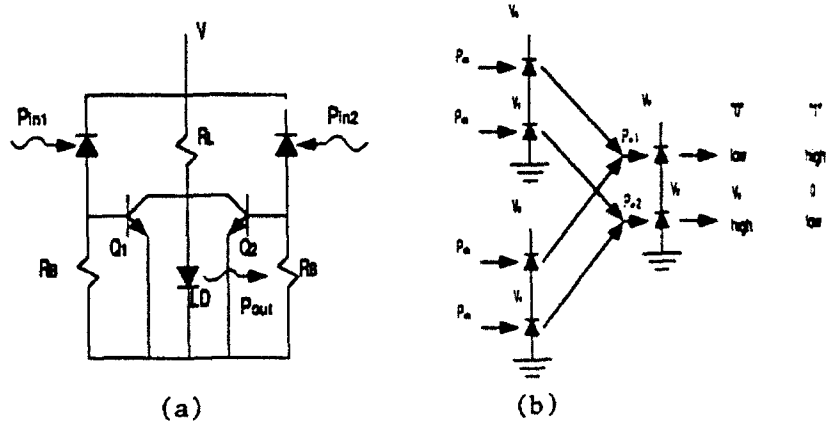


Figure 1

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